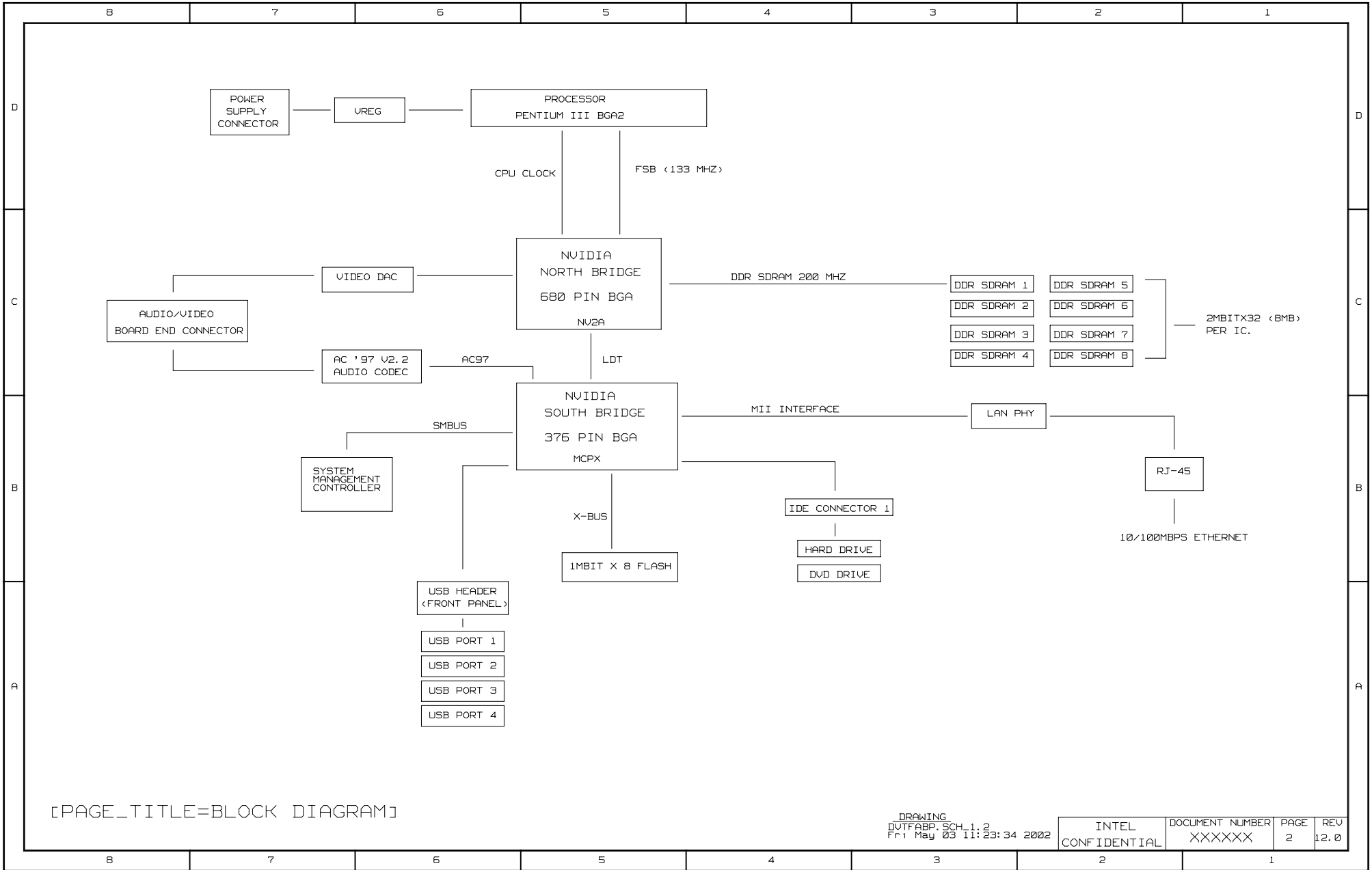


8	7	6	5	4	3	2	1
PAGE		CONTENTS		PAGE		CONTENTS	
[1]	COVER PAGE]	[27]	CPU VREG OUTPUT FILTER]	<div style="text-align: center;"> <p>SCHMATIC REV 12.0</p> <p>PBA NUMBER A88754-300</p> <p>REV 01</p> <p>BOM RELEASE DATE 04/26/02</p> <p>DVT REV 12.0 FAB P</p> <p>STANDARD BOM: MICRON DDR SEE PAGE 13 FOR SAMSUNG ALT</p> <p>XBLADE</p> </div>			
[2]	BLOCK DIAGRAM]	[28]	1.5V SWITCHING REGULATOR]				
[3]	RESET MAP]	[29]	CLOCK GENERATOR]				
[4]	GPIO/IDSEL TABLE]	[30]	1.25V LINEAR REGULATOR]				
[5]	PENTIUM III BGA2 PART 1 OF 4]	[31]	LINEAR_REGULATORS_1.5_2.5]				
[6]	PENTIUM III BGA2 PART 2 OF 4]	[32]	DVT POWER CONNECTOR]				
[7]	PENTIUM III BGA2 PARTS 3 & 4]	[33]	BULK DECOUPLING]				
[8]	CPU VCORE DECOUPLING]	[34]	SUPERCAP VBAT REGULATOR]				
[9]	CPU VTT DECOUPLING]	[35]	LAN ICS1893]				
[10]	ITP TERMINATION]	[36]	LAN JACK/THERMAL SENSE/EEPROM]				
[11]	NV2A 1 OF 2(NORTH BRIDGE)]	[37]	IDE]				
[12]	NV2A 2 OF 2(NORTH BRIDGE)]	[38]	AUDIO CODEC]				
[13]	NV2A STRAPPING]	[39]	AUDIO AMPLIFIER]				
[14]	DDR SDRAM (PARTITION A)]	[40]	AUDIO VREG AND BIAS]				
[15]	DDR SDRAM (PARTITION B)]	[41]	CX25871\SAN ANTONIO VIDEO-ENCODER]				
[16]	DDR SDRAM (PARTITION C)]	[42]	CX25874 VIDEO DAC AND TV ENCODER]				
[17]	DDR SDRAM (PARTITION D)]	[43]	VIDEO DAC AND TV ENCODER]				
[18]	DDR PARALLEL TERM DATA A/B]	[44]	AV CONNECTOR]				
[19]	DDR PARALLEL TERM DATA C/D]	[45]	LABELS AND MOUNTING HOLES]				
[20]	VTERM DECOUPLING]	[46]	FLASH]				
[21]	MEMORY DECOUPLING]	[47]	USB FRONT PANEL]				
[22]	NV2A DECOUPLING]	[48]	NV2A FAN/5V DRAIN/BROWN OUT]				
[23]	MCPX 1 OF 2]	[49]	SMC/FAN/DVD PWR/FRONT PANEL]				
[24]	MCPX 2 OF 2]	[50]	MCPX MUXED PIN ASSIGNMENT]				
[25]	MCPX INPUT STRAPS]	[51-56]	INDEX]				
[26]	CPU VOLTAGE REGULATOR]						
<p>NOTES:</p> <ol style="list-style-type: none"> <li>THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLS FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.</li> <li>RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.</li> <li>VCC = +5V UNLESS OTHERWISE SPECIFIED.</li> <li>* SUFFIX INDICATES ACTIVE LOW SIGNAL.</li> <li>\I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.</li> <li>THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.</li> </ol> <p>[PAGE_TITLE=COVER PAGE]</p>							
<p>DRAWING: DUTFABP_SCH_1_1 Fri May 03 11:23:32 2002</p>							
BOM RELEASE DATE		xx/xx/xx	PB NUMBER		XXXXXX-XXX		
SIGNATURE		DATE	intel		3065 BOWERS AVE SANTA CLARA, CA 95051		
DRN BY			TITLE		SCH, PBA, XBLADE		
CHK BY		xxxxxx	XXXXXX				
EPLD			INTEL		DOCUMENT NUMBER	PAGE	REV
APUD			CONFIDENTIAL		XXXXXX	1/56	12.0
APUD							

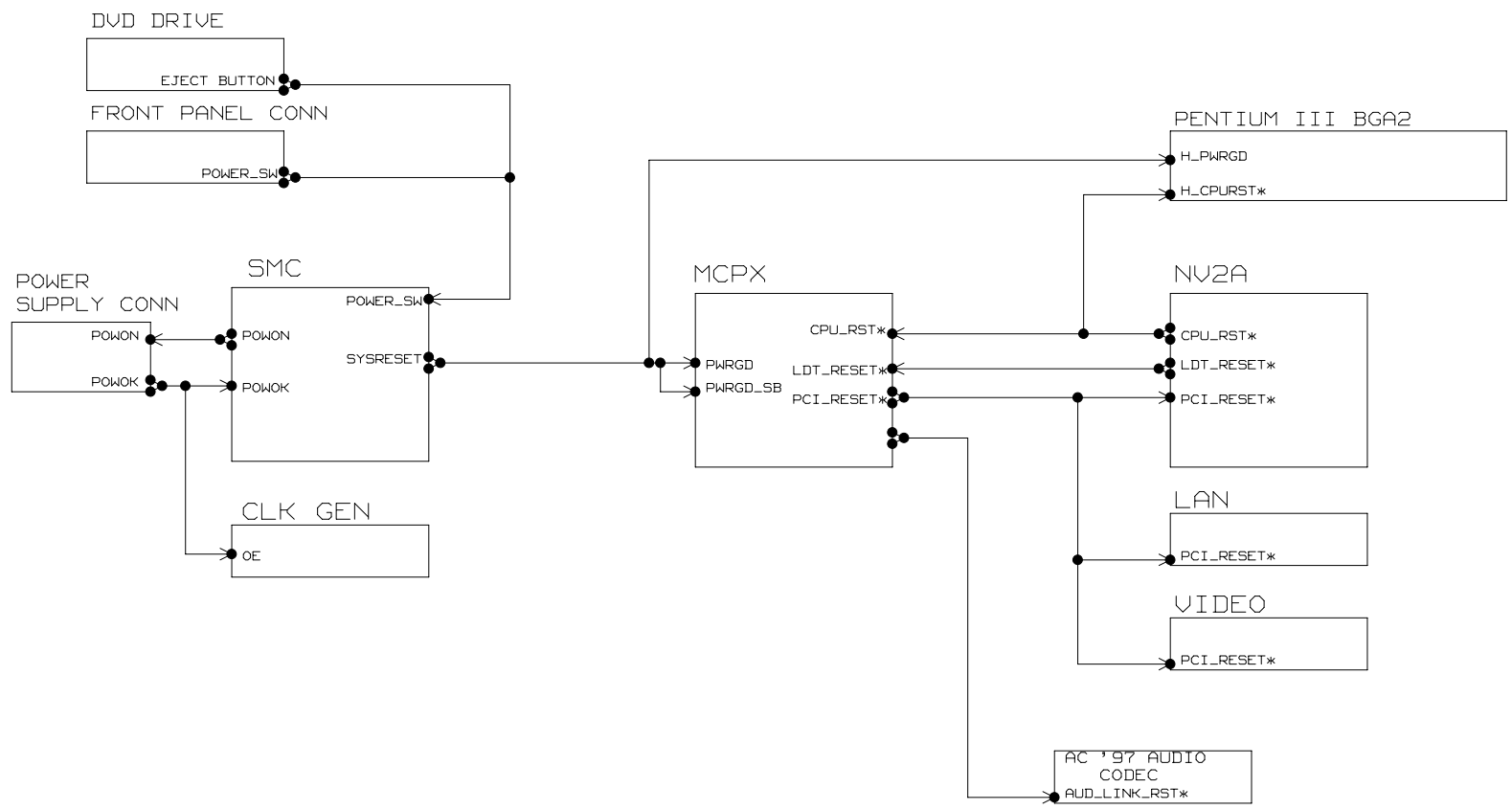


[PAGE\_TITLE=BLOCK DIAGRAM]

DRAWING  
 DUTFABP\_SCH\_1\_2  
 Fri May 03 11:23:34 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 2	REV 12.0
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# RESET & POWER-ON MAP



[PAGE\_TITLE=RESET MAP]

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 DUTFABP\_SCH\_1\_3  
 Fri May 03 11:23:35 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 3	REV 12.0
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### PCI DEVICE MAP

DEVICE	PCI BUS #	DEVICE #	FUNCTION	DEVICE ID	COMMENTS
NV2A					
HOST BRIDGE	00	00	00	02A8	IT IS DIFFERENT FUNCTIONALLY FROM CRUSH12
AGP BRIDGE	00	30	00	01B7	SECONDARY BRIDGE #=1 IN STD ENUMERATION
NV2A	02	00	00	02A0	
MCPX					
APU	00	05	00	01B0	
AUDIO CODEC	00	06	00	01B1	
USB1.1 OHCI A	00	02	00	01C2	
USB1.1 OHCI B	00	03	00	01C2	
MAC	00	04	00	01C3	
IDE	00	09	00	01BC	
SMBUS2	00	01	01	01B4	
SUBTRACTIVE	00	01	00	01B2	INCLUDES LEGACY AND LPC (BIOS)

### GPIO USAGE TABLE

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
MCPX	GPIO0	OUT	UCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO1	OUT	UCC3	H	H	CNFG_SEL1
MCPX	GPIO14	IN	UCC3	Z	Z	CNFG_SEL0
MCPX	GPIO15	OUT	UCC3	Z	Z	TP_DEBUG_GPIO15
MCPX	GPIO16	IN	UCC3	Z	Z	CNFG_SEL2
MCPX	GPIO19	OUT	UCC3	Z	Z	LULCNT1
MCPX	GPIO20	OUT	UCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO21	IN	UCC3	H	H	SMI* INPUT FROM SMC
MCPX	GPIO22	OUT	UCC3	Z	Z	LULCNT0
MCPX	GPIO24		UCC3	Z	Z	TESTPOINT (NOT USED)

### SMBUS ADDRESS MAP

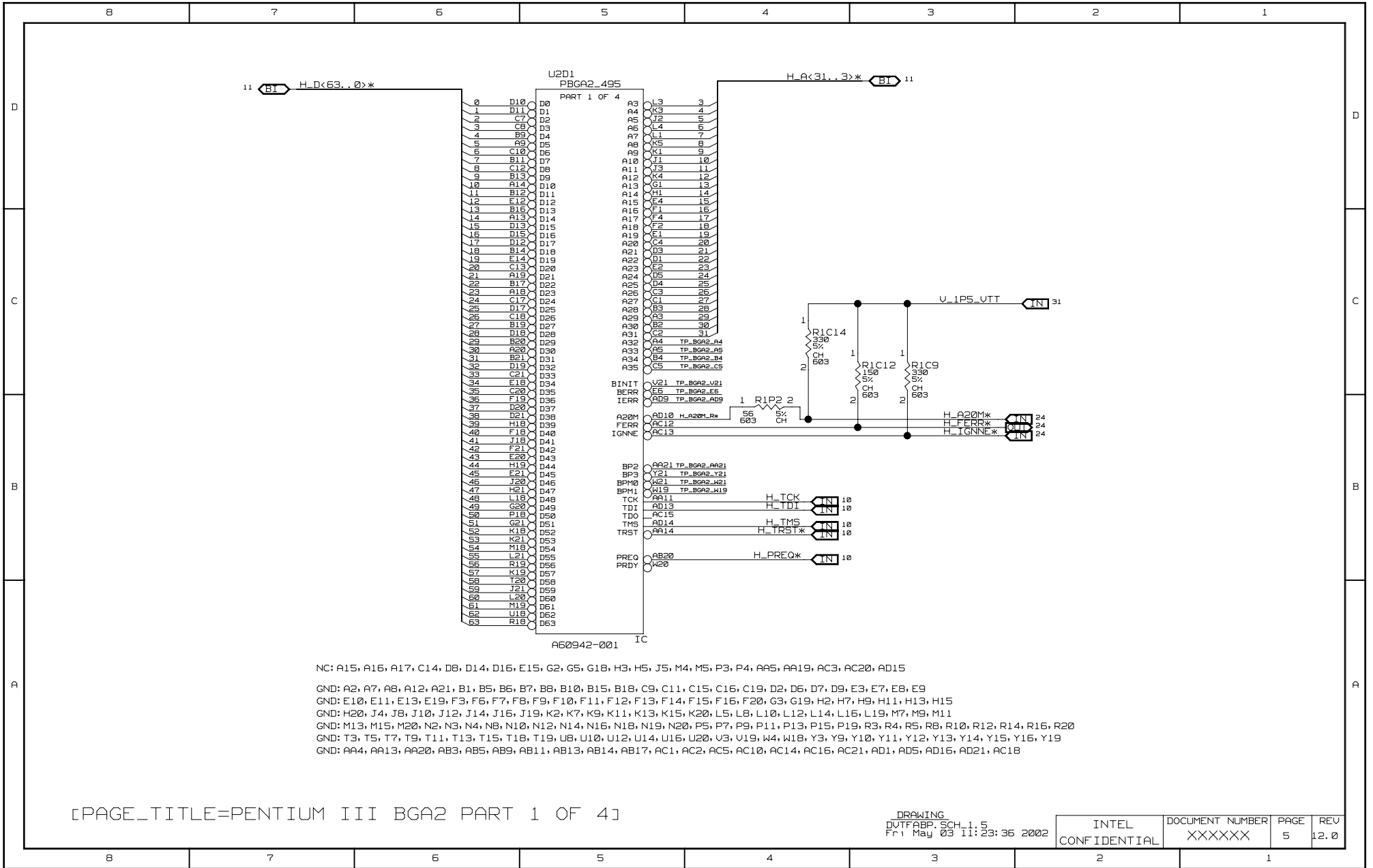
DEVICE	SMBUS #	ADDRESS	EVT	DVT	COMMENTS
CX25B71	1	8A/8B		X	CONNECT ALTADDR (PIN 48) TO 3.3
CNR EEPROM	1	A8/A9	X	X	CONNECT CNR_SMB[2:0]=100 BINARY
MCP1 SMB1	1	10/11	X	X	SMBUS HOST (WRITE/READ)
SMC	1	20/21	X	X	(WRITE/READ)
TEMP(ADM1032)	1	98/99	X	X	(WRITE/READ)
DIMM0	0	A0/A1	X		M_LA_CS[1..0]*
DIMM1	0	A2/A3	X		M_LB_CS[1..0]*
DIMM2	0	A4/A5			M_LB_CS[3..2]*
MCP1 SMB0	0	10/11	X		SMBUS HOST (WRITE/READ)

\*NOTE: DEVICES ON SMBUS 0 DON'T EXIST ON DVT.

[PAGE\_TITLE=GPIO/IDSEL TABLE]

DRAWING  
DVT FAB. SCH 1.4  
Fri May 03 11:23:35 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 4	REV 12.0
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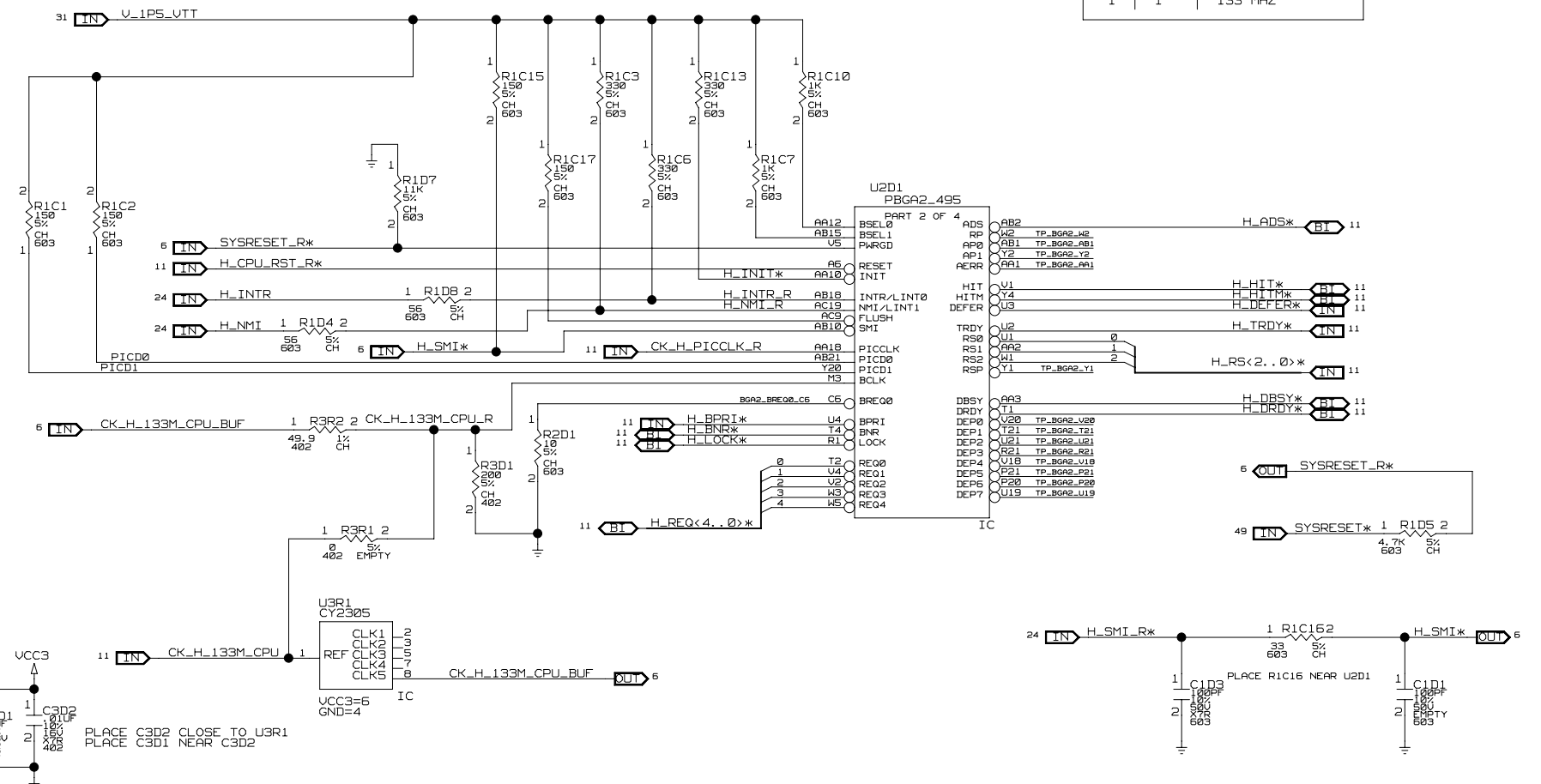


[PAGE\_TITLE=PENTIUM III BGA2 PART 1 OF 4]

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DVT/FABP\_SCH 11:5  
Fri May 03 11:23:36 2002

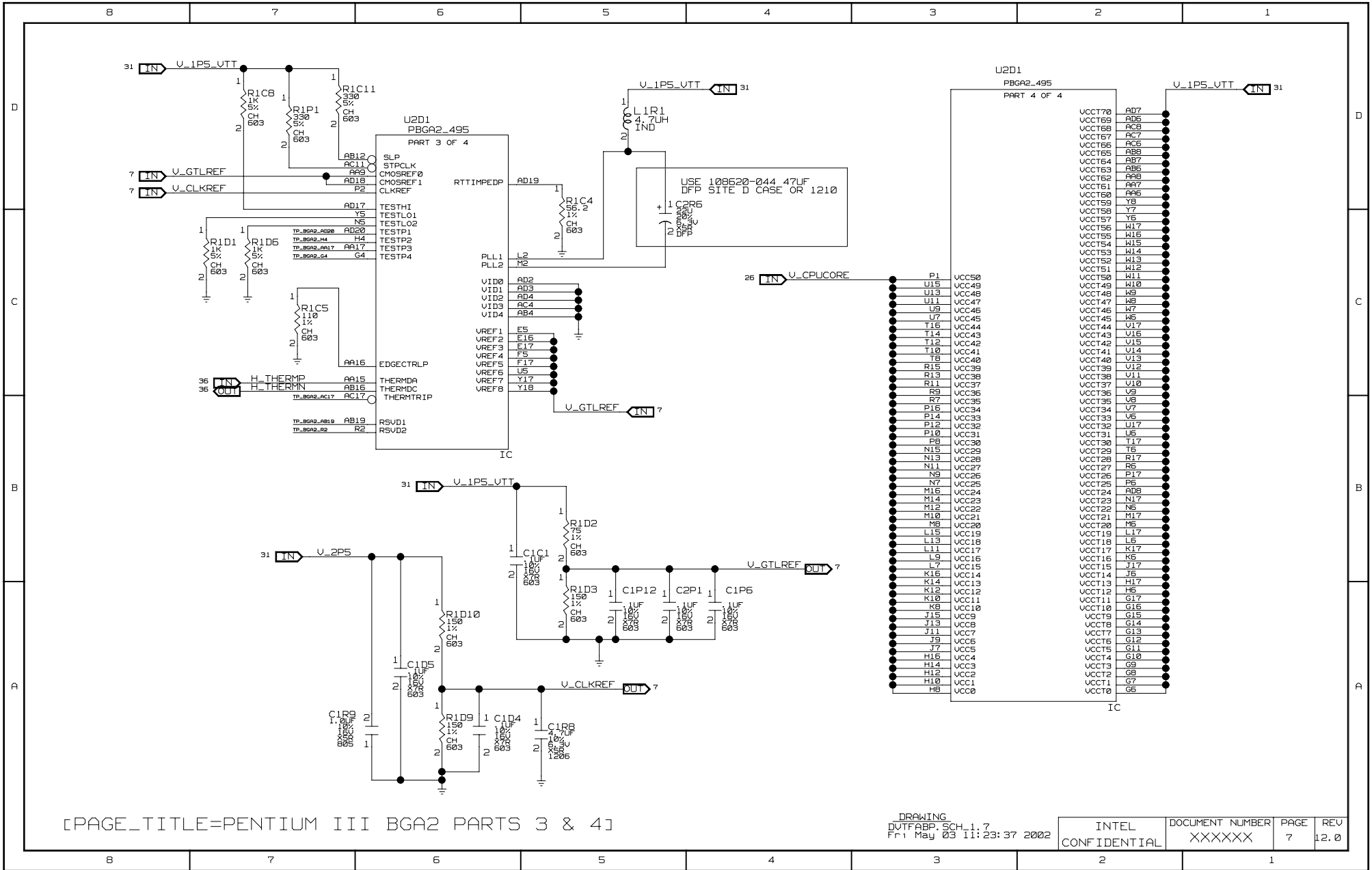
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	5	12.0

BSEL1	BSEL0	SYSTEM BUS FREQUENCY
0	0	RESERVED
0	1	100 MHZ
1	0	RESERVED
1	1	133 MHZ

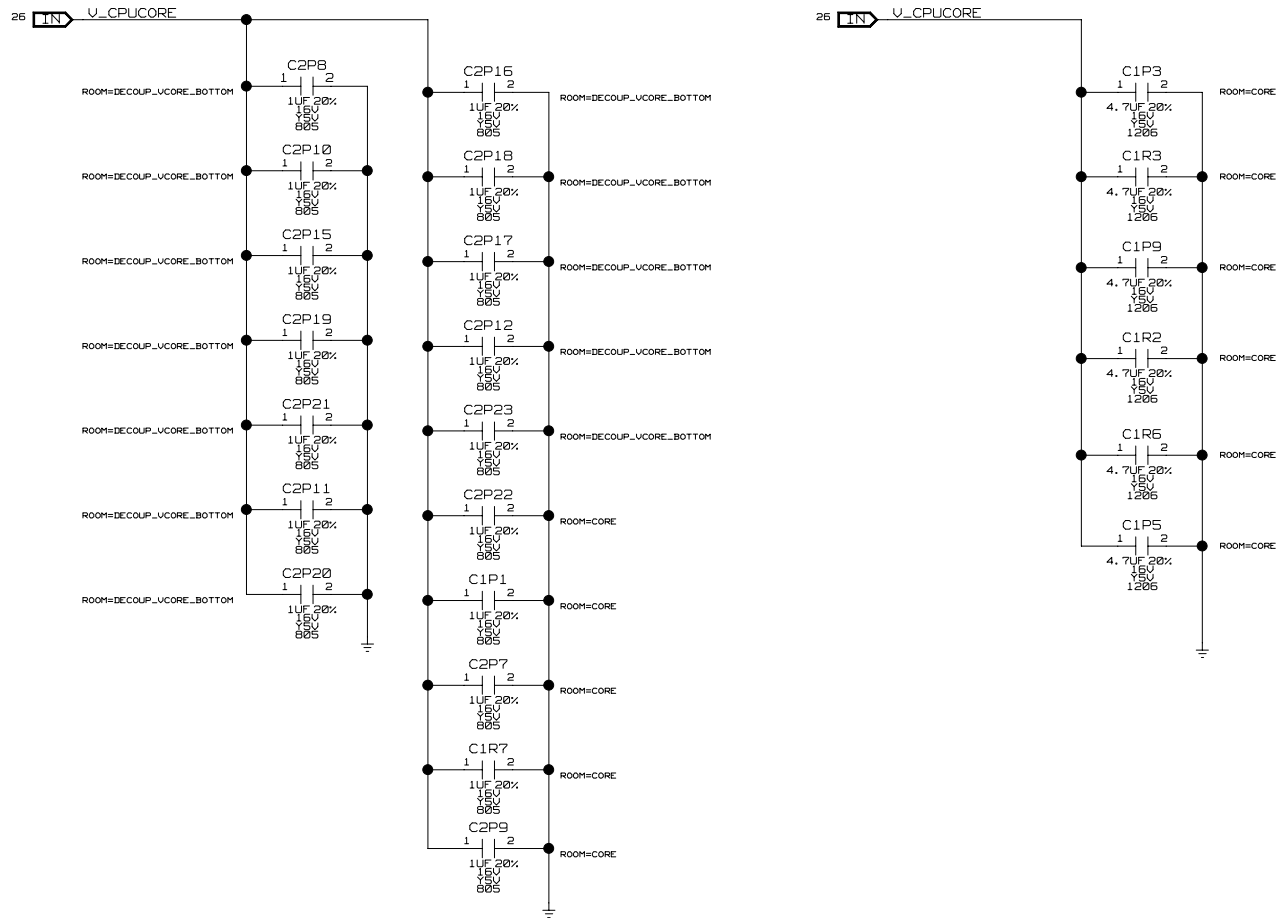


PLACE C3D2 CLOSE TO U3R1  
PLACE C3D1 NEAR C3D2

PLACE R1C16 NEAR U2D1



# CPU VCORE DECOUPLING



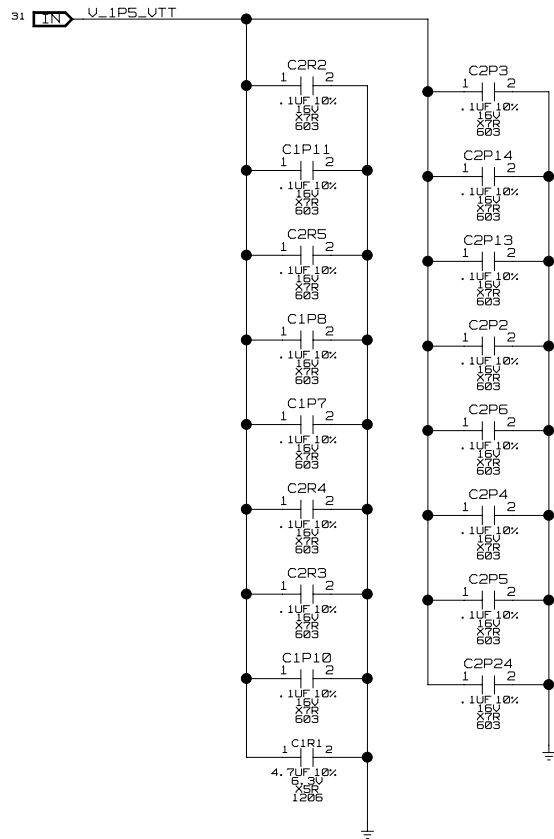
[PAGE\_TITLE=CPU VCORE DECOUPLING]

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 DUTFABP\_SCH\_11\_8  
 Fri May 03 11:23:38 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 8	REV 12.0
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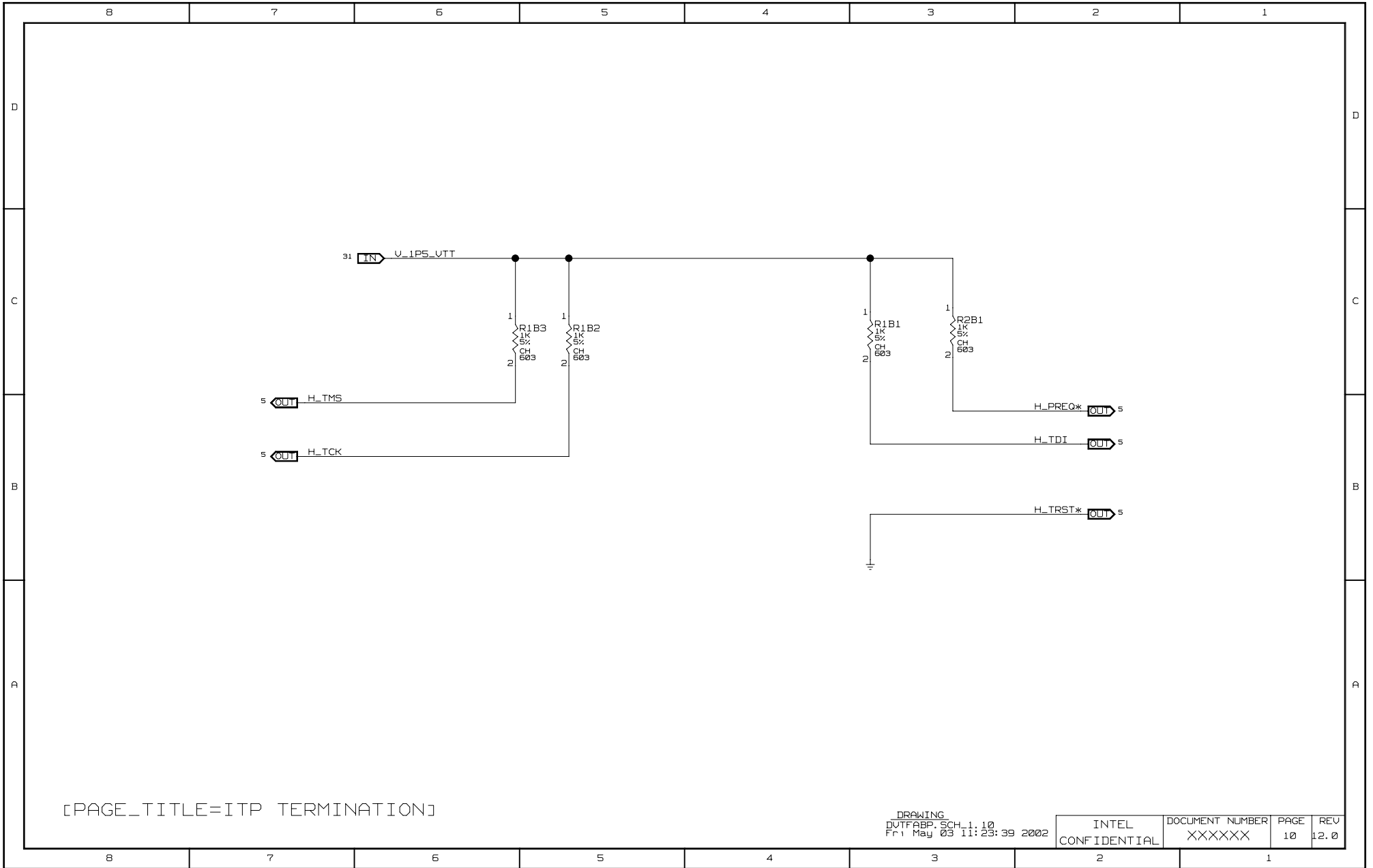
CPU VTT DECOUPLING



[PAGE\_TITLE=CPU VTT DECOUPLING]

DRAWING  
 DUTFABP\_SCH\_11\_9  
 Fri May 03 11:23:39 2002

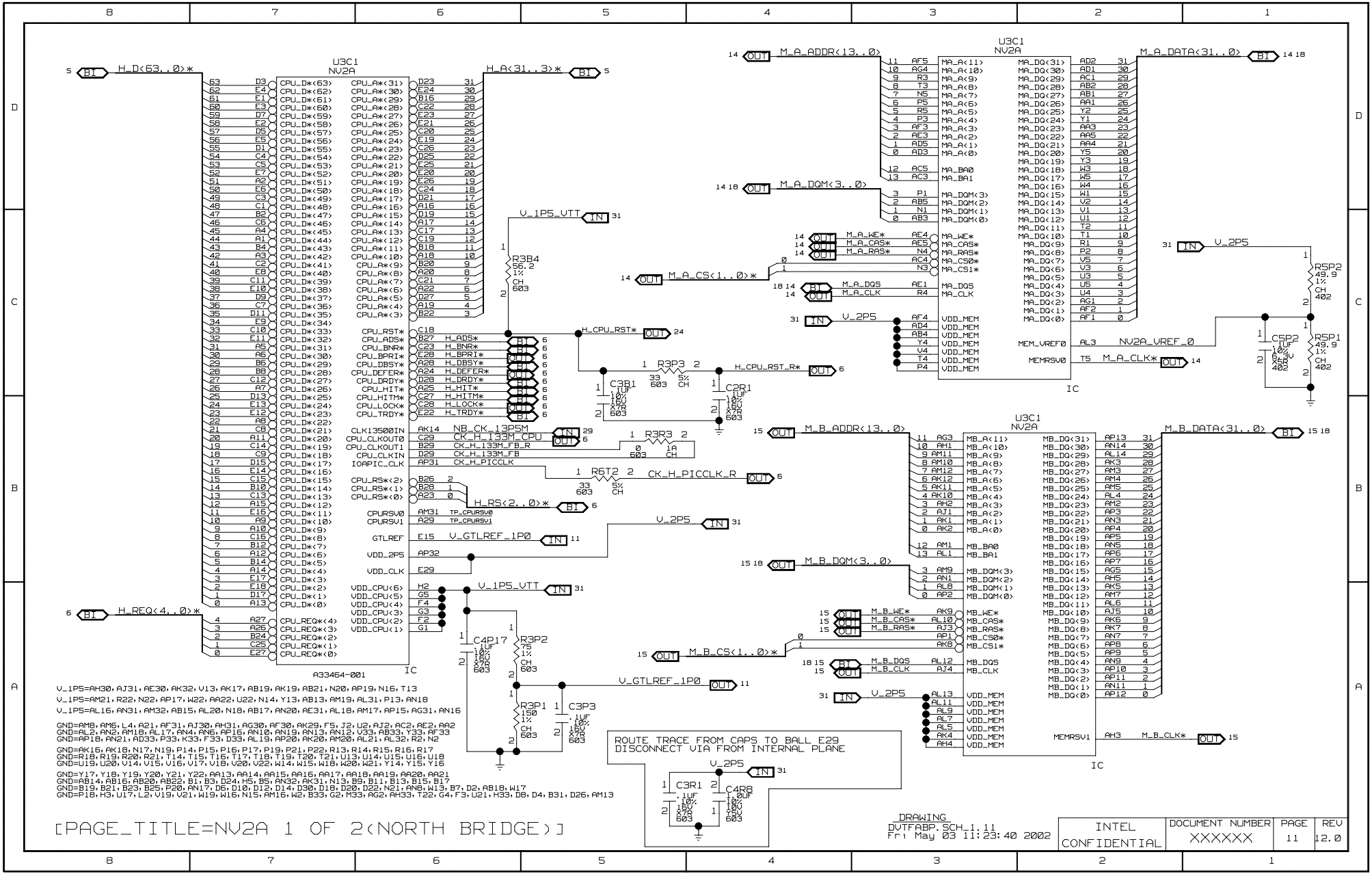
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 9	REV 12.0
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[PAGE\_TITLE=ITP TERMINATION]

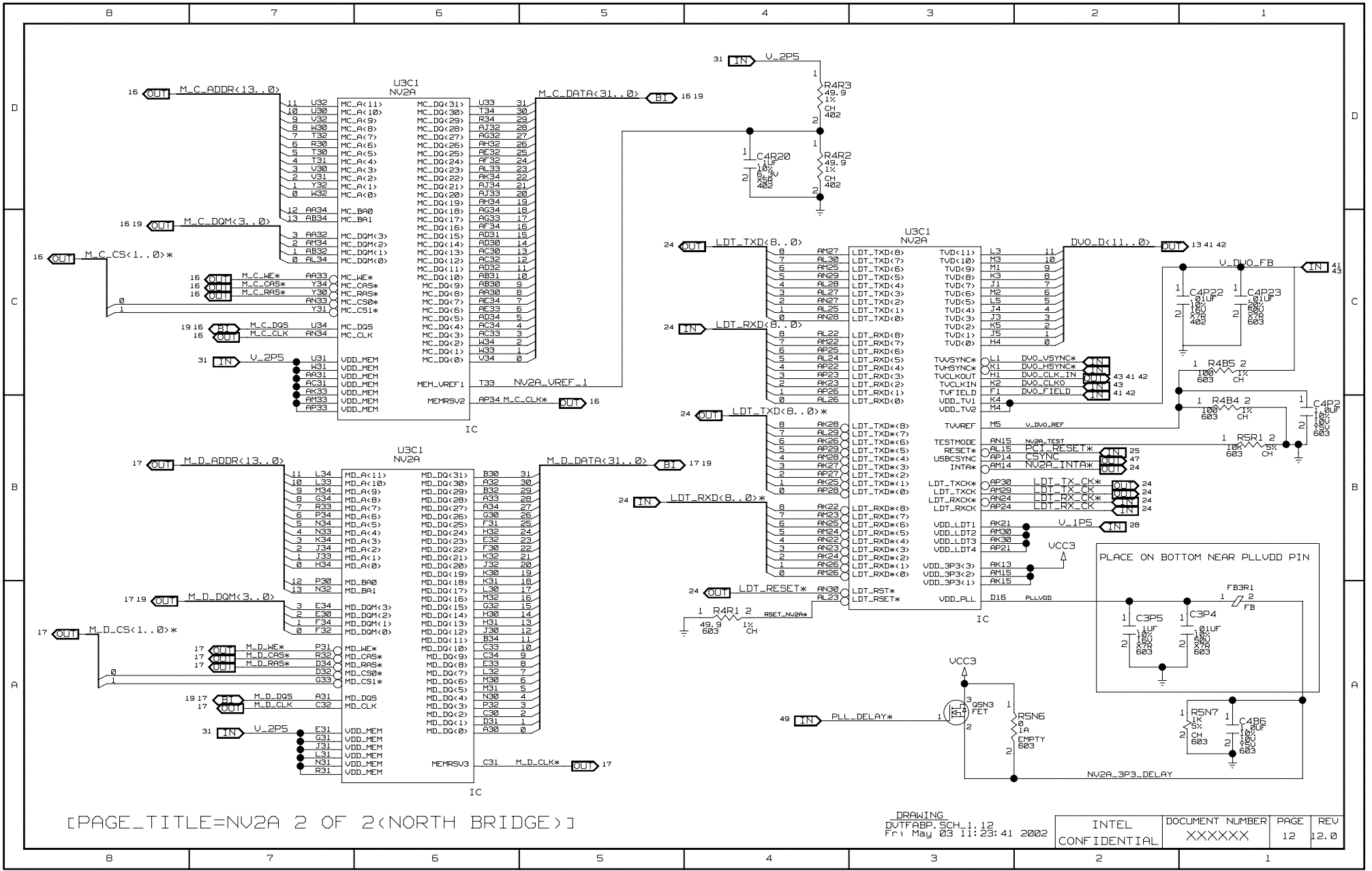
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 Fri May 03 11:23:39 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 10	REV 12.0
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DRAWING  
DVT/ASP\_SCH 11:11  
Fri May 03 11:23:40 2002

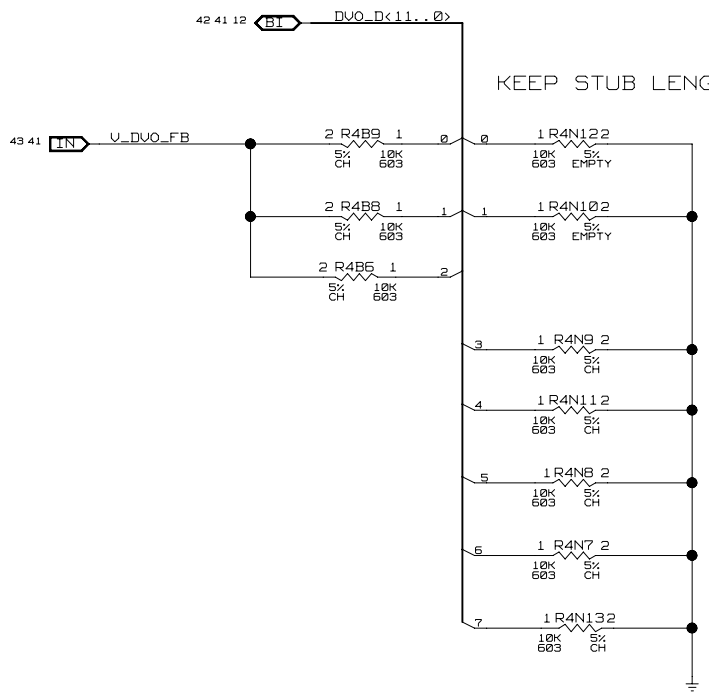
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 11	REV 12.0
-----------------------	---------------------------	------------	-------------



[PAGE\_TITLE=NV2A 2 OF 2<NORTH BRIDGE>]

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DUTFABP\_SCH 11:12  
Fr 1 May 03 11:23:41 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 12	REV 12.0
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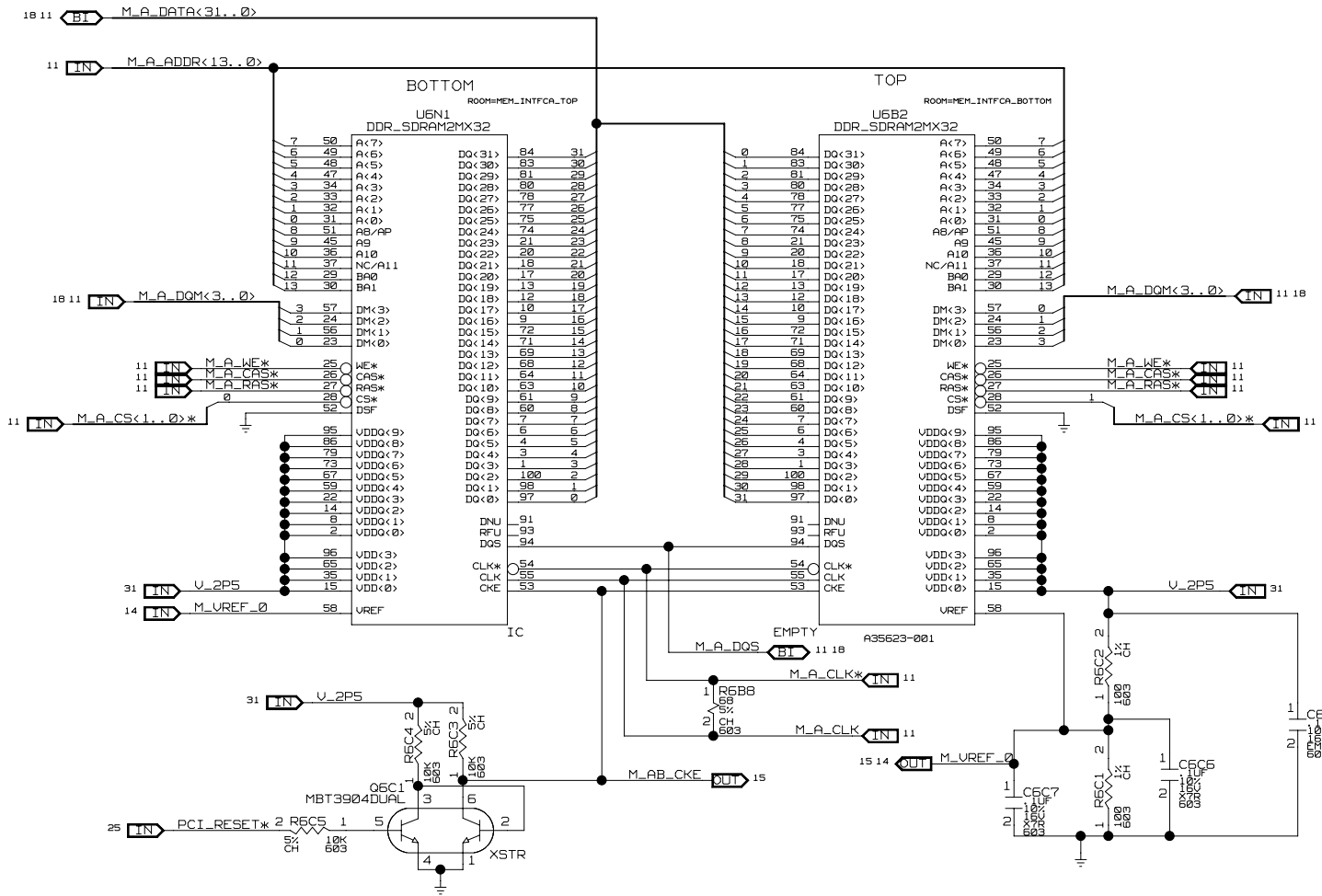


TVD		DEFINITION
[7]	0* 1	ENABLE INTERNAL LDT TERMINATION DISABLE INTERNAL LDT TERMINATION
[6]	0* 1	13.5MHZ OR 16.6MHZ 14.31818MHZ
[5:4]	00* 01 10 11	USE FSB FREQUENCY BASED ON TVD[3:2] USE INTERNAL PROGRAMMED VALUE A USE INTERNAL PROGRAMMED VALUE B FORCE 65MHZ
[3:2]	00 01* 10 11	NA FSB FREQ=133MHZ FOR 16.6MHZ INPUT CLK NA NA
[1:0]	00* 01 10 11	EMRS MICRON MATCHED MODE EMRS [6,1]=[0,1], HALF OF NORMAL DRIVE MODE RESERVED EMRS MATCHED 30% DRIVE MODE<SAMSUNG>

\* = CURRENT SETTING

FOR SAMSUNG DDR:  
EMPTY R4N10 AND R4N12  
STUFF R4B8 AND R4B9

# MEMORY INTERFACE PARTITION A

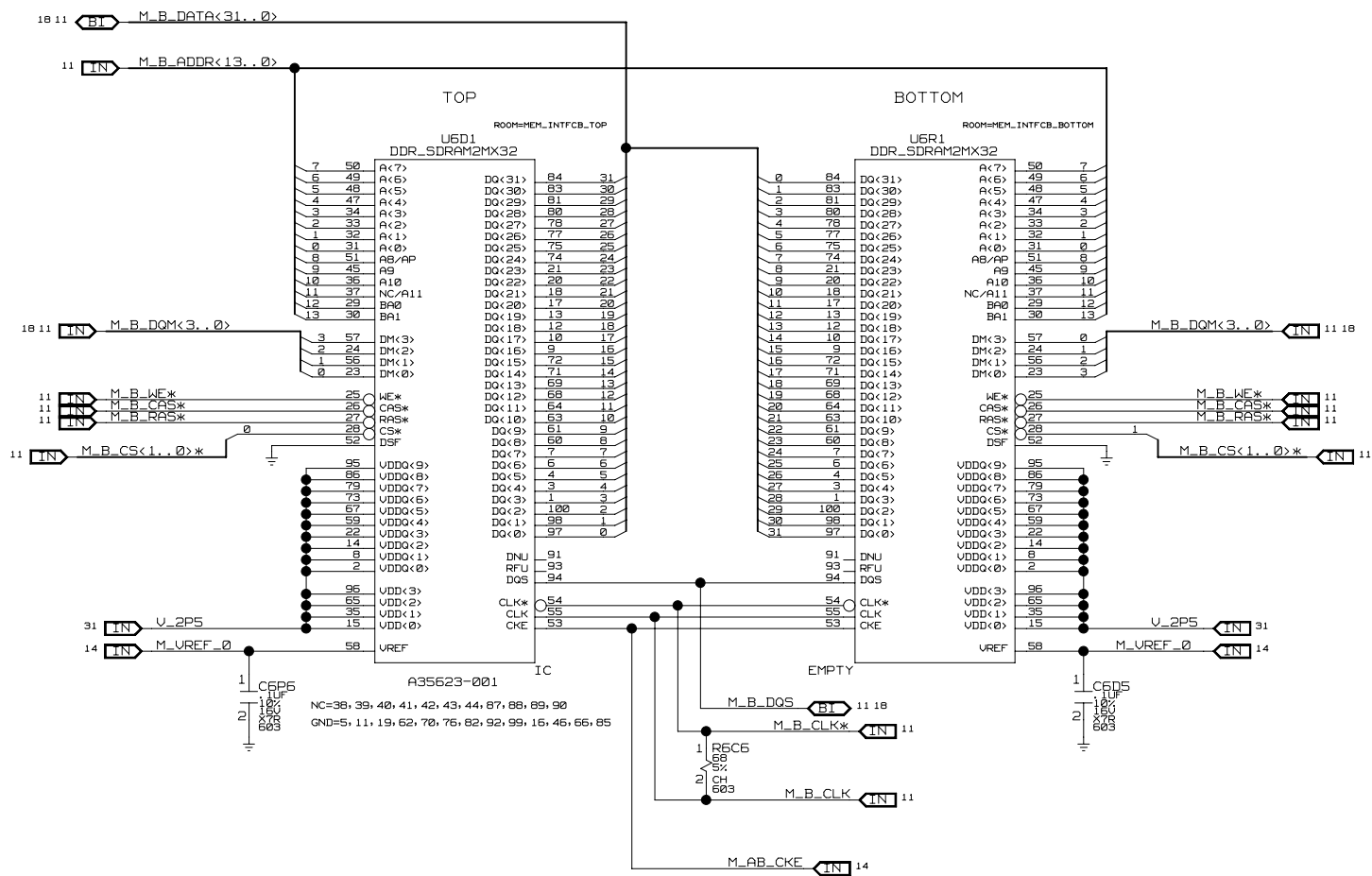


[PAGE\_TITLE=DDR SDRAM (PARTITION A)]

DRAWING  
DVT/FAB SCH 11:14  
Fr 1 May 03 11:23:42 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 14	REV 12.0
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# MEMORY INTERFACE PARTITION B

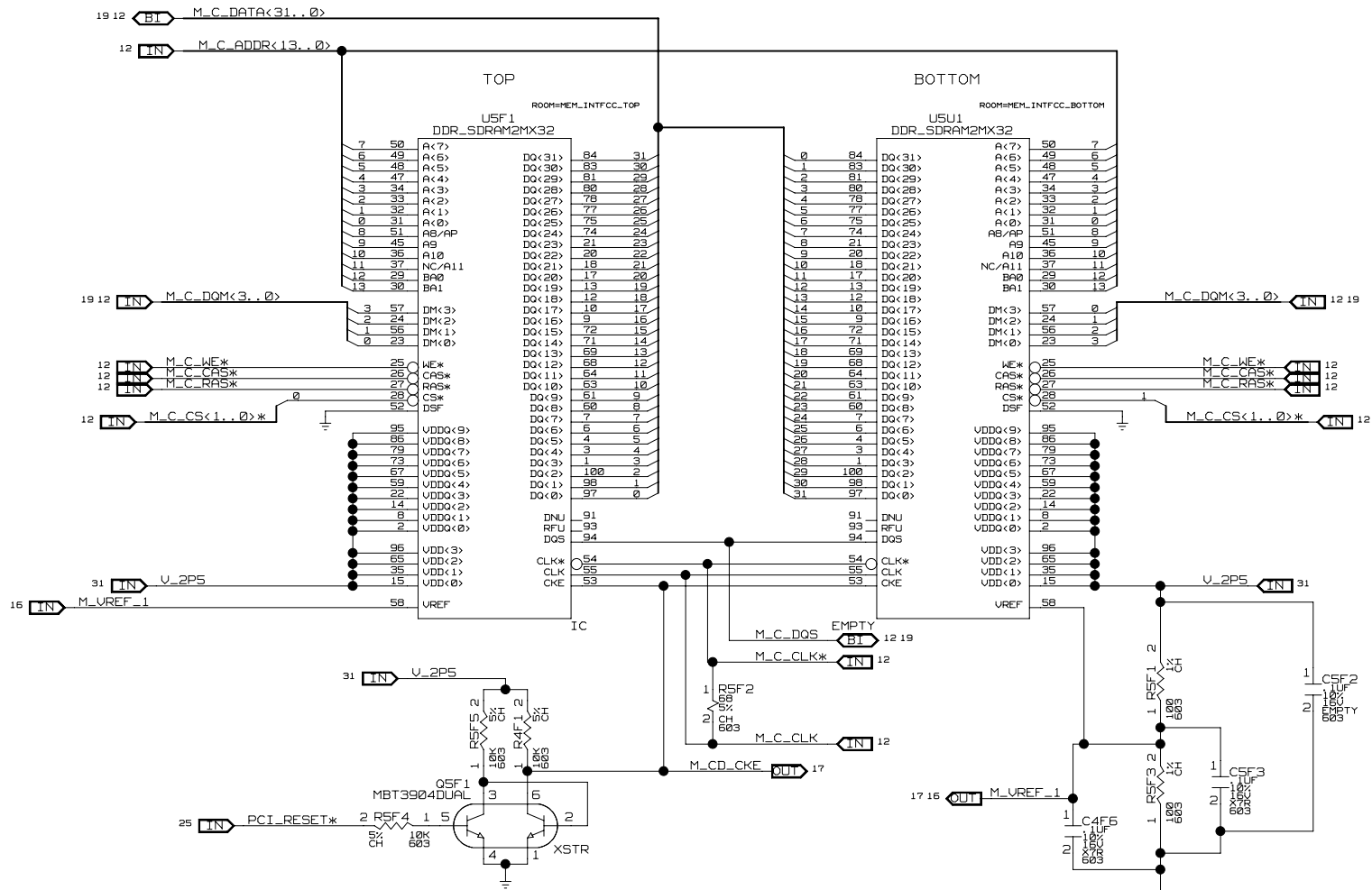


[PAGE\_TITLE=DDR SDRAM (PARTITION B)]

DRAWING  
DVT/FABP\_SCH 11:15  
Fri May 03 11:23:43 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	15	12.0

# MEMORY INTERFACE PARTITION C



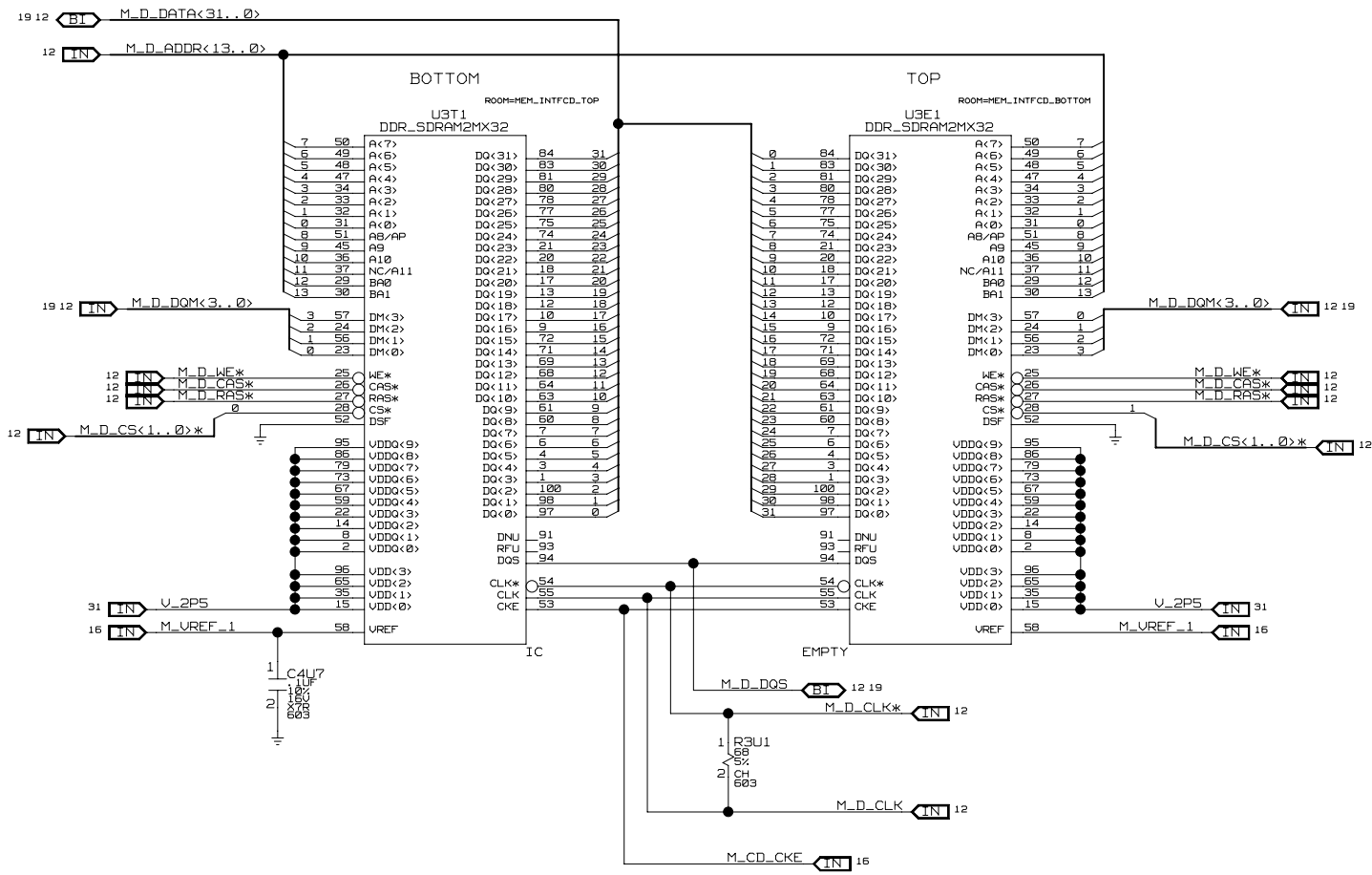
[PAGE\_TITLE=DDR SDRAM (PARTITION C)]

DRAWING  
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Fr 1 May 03 11:23:44 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 16	REV 12.0
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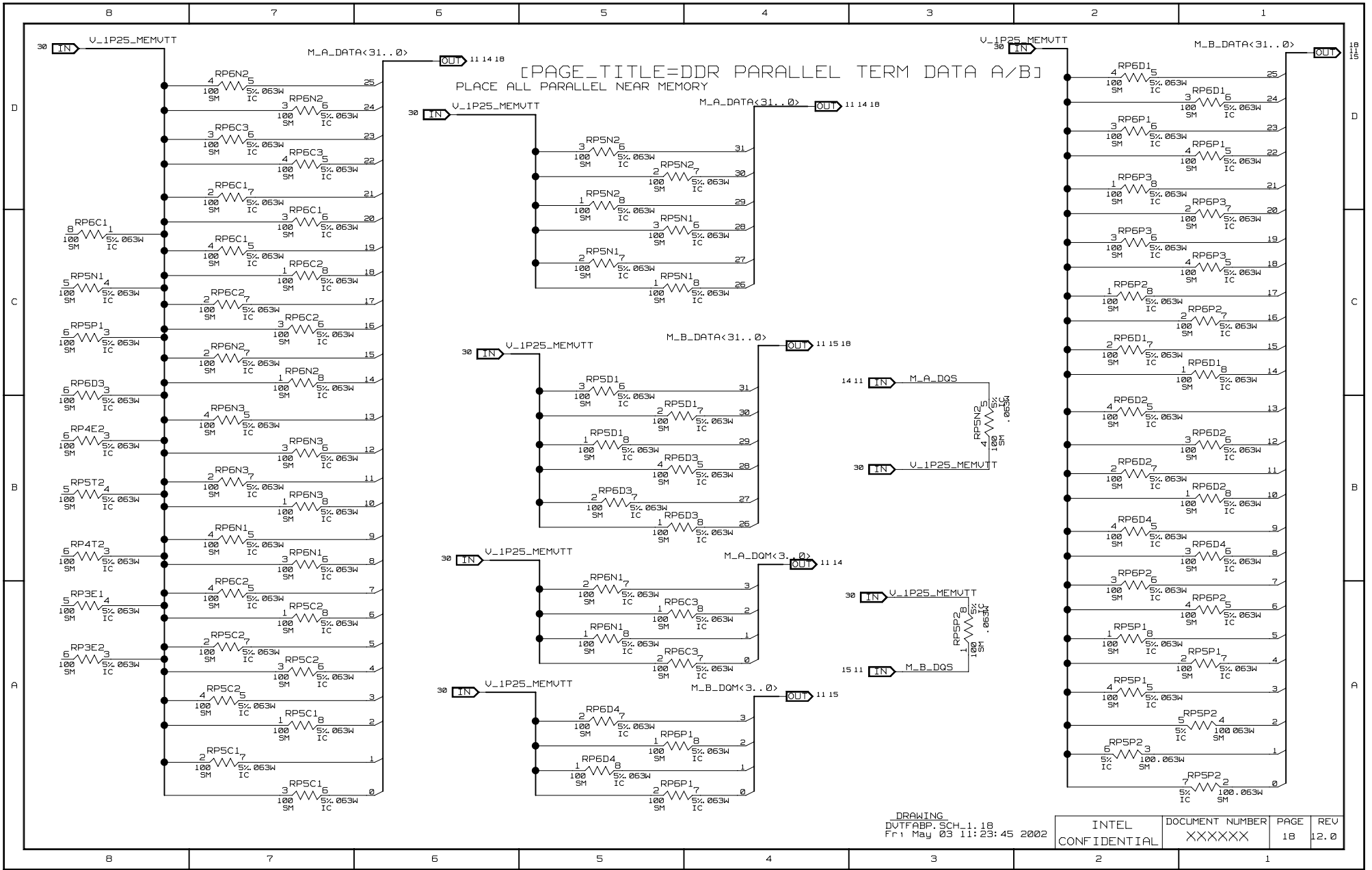
MEMORY INTERFACE PARTITION D



[PAGE\_TITLE=DDR SDRAM (PARTITION D)]

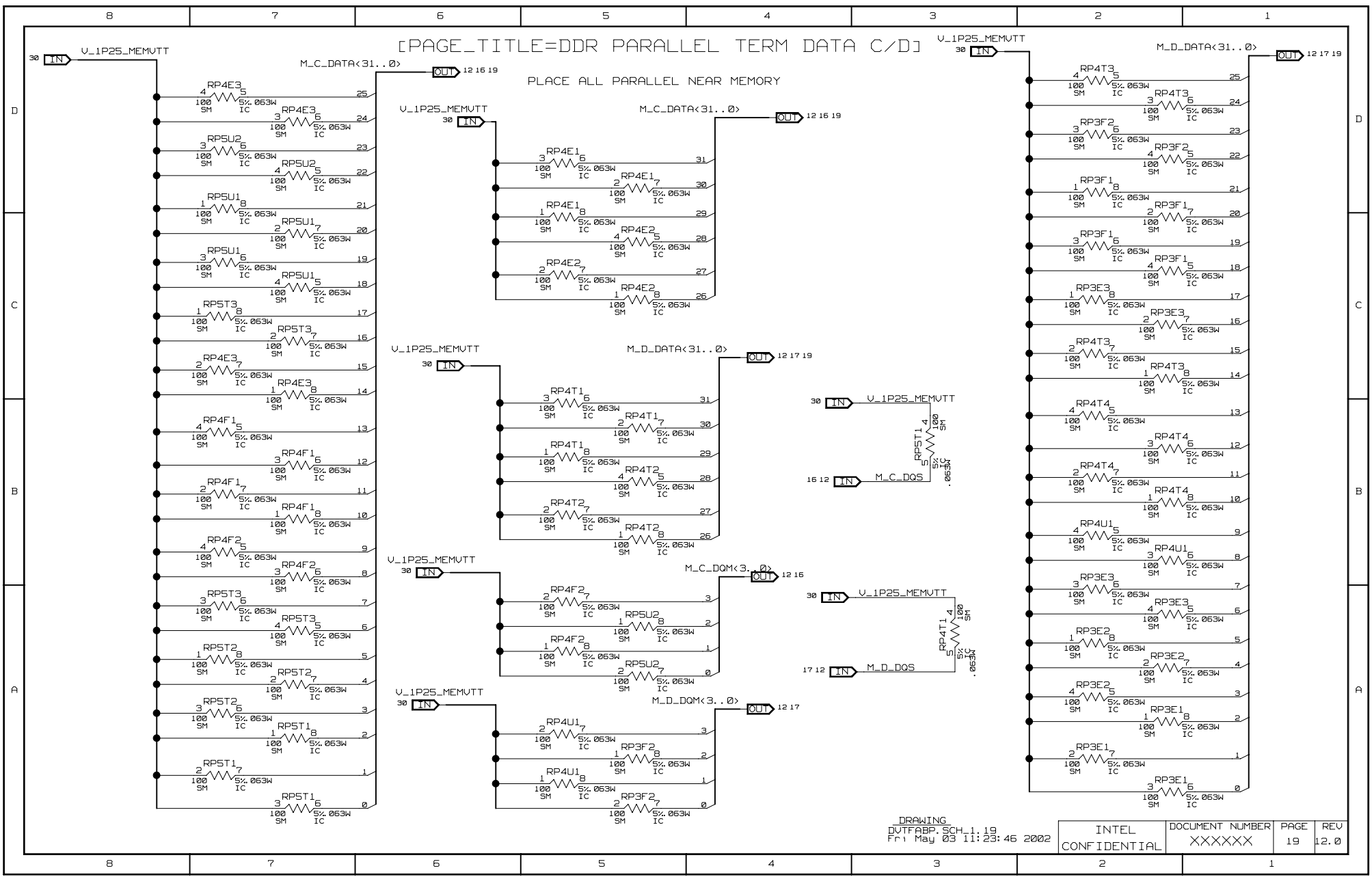
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DVTFABP\_SCH\_117  
Fri May 03 11:23:45 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	17	12.0

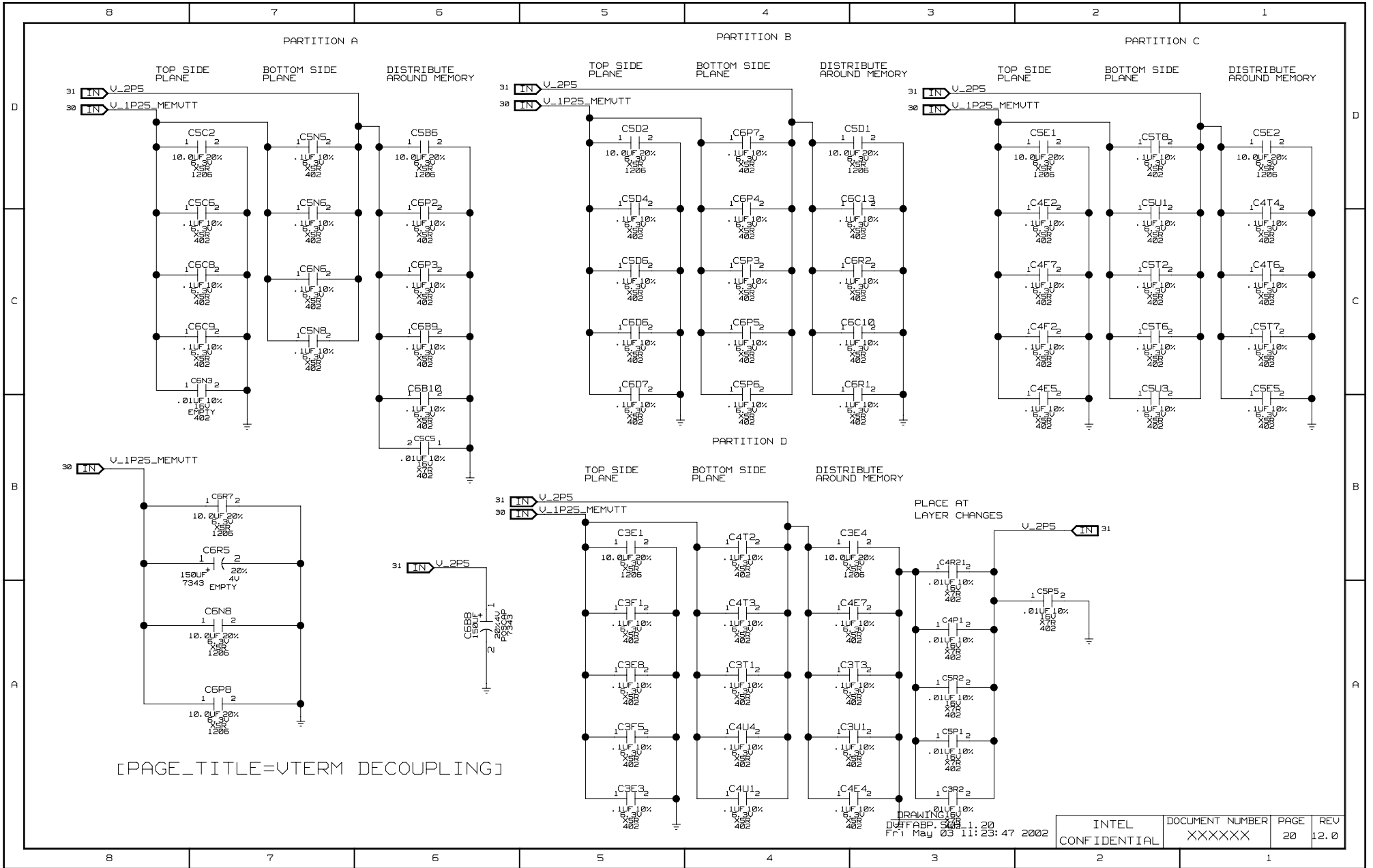


INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 18	REV 12.0
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[PAGE\_TITLE=DDR PARALLEL TERM DATA C/D]



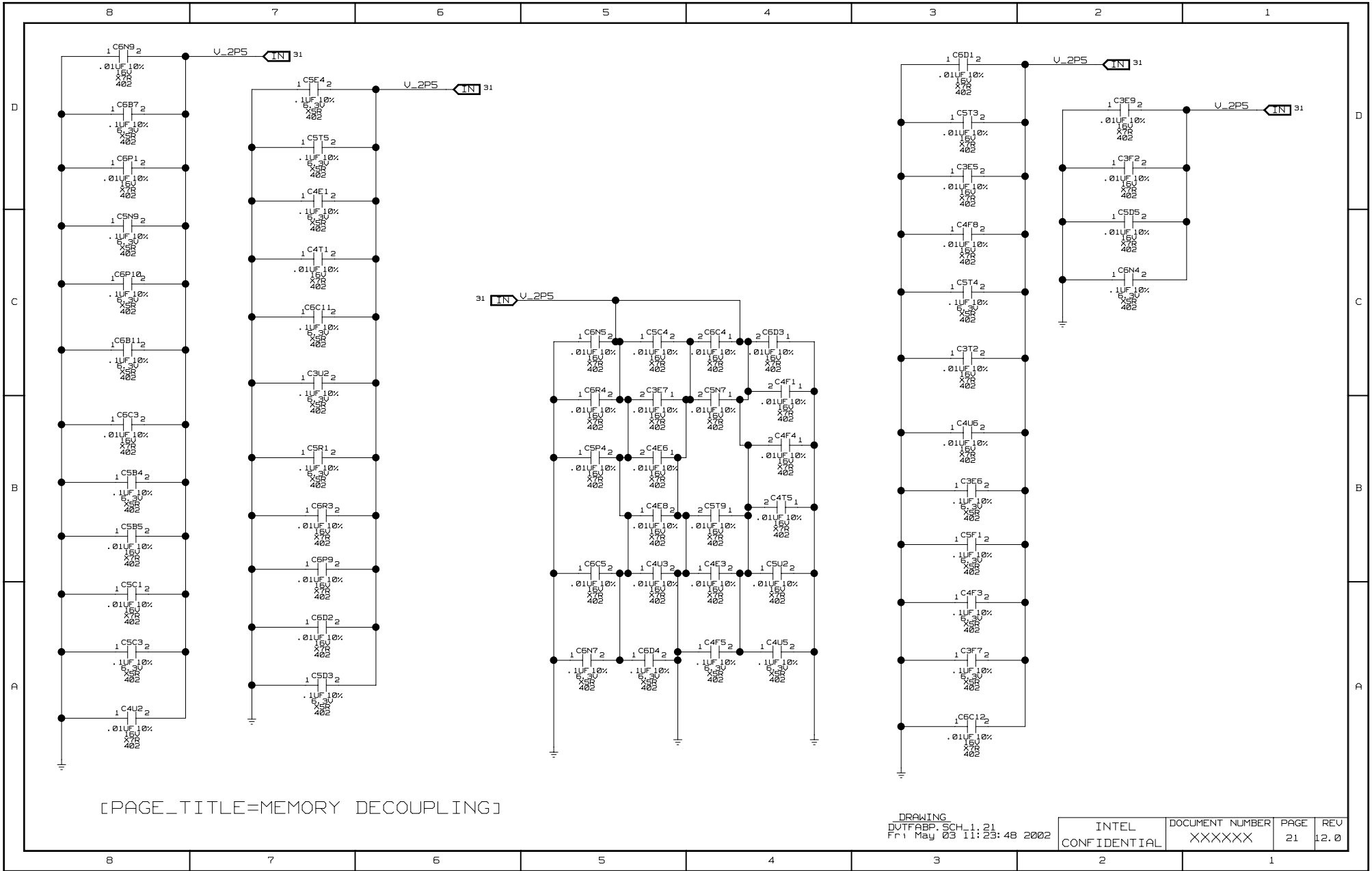
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CONFIDENTIAL	XXXXXX	19	12.0



[PAGE\_TITLE=VTERM DECOUPLING]

DRAWING 153  
 DATE: 05/03/02  
 Fr 11:23:47 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	20	12.0



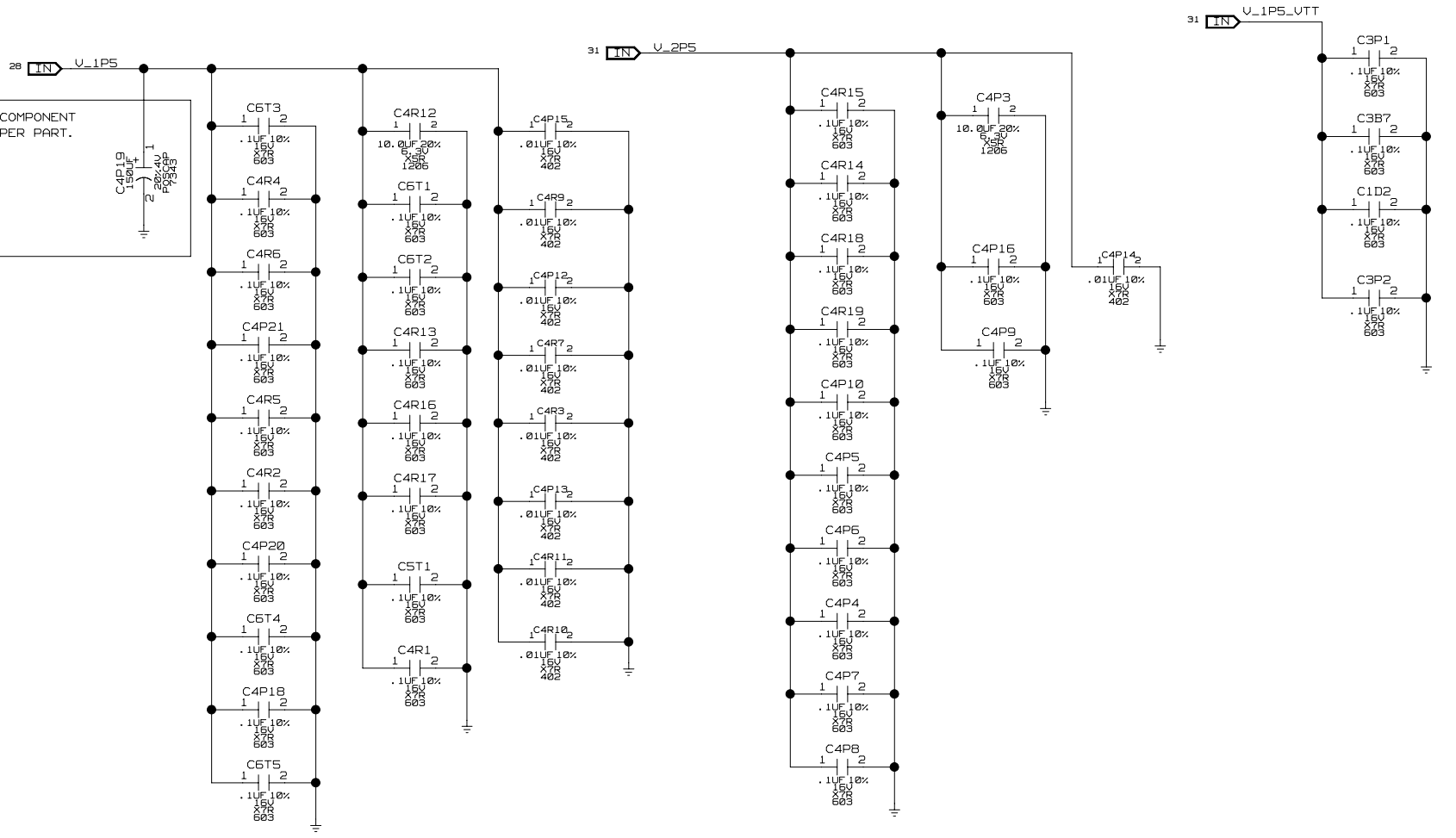
[PAGE\_TITLE=MEMORY DECOUPLING]

DRAWING  
 DUTFABP\_SCH\_11\_21  
 Fri May 03 11:23:48 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	21	12.0

# NV2A DECOUPLING

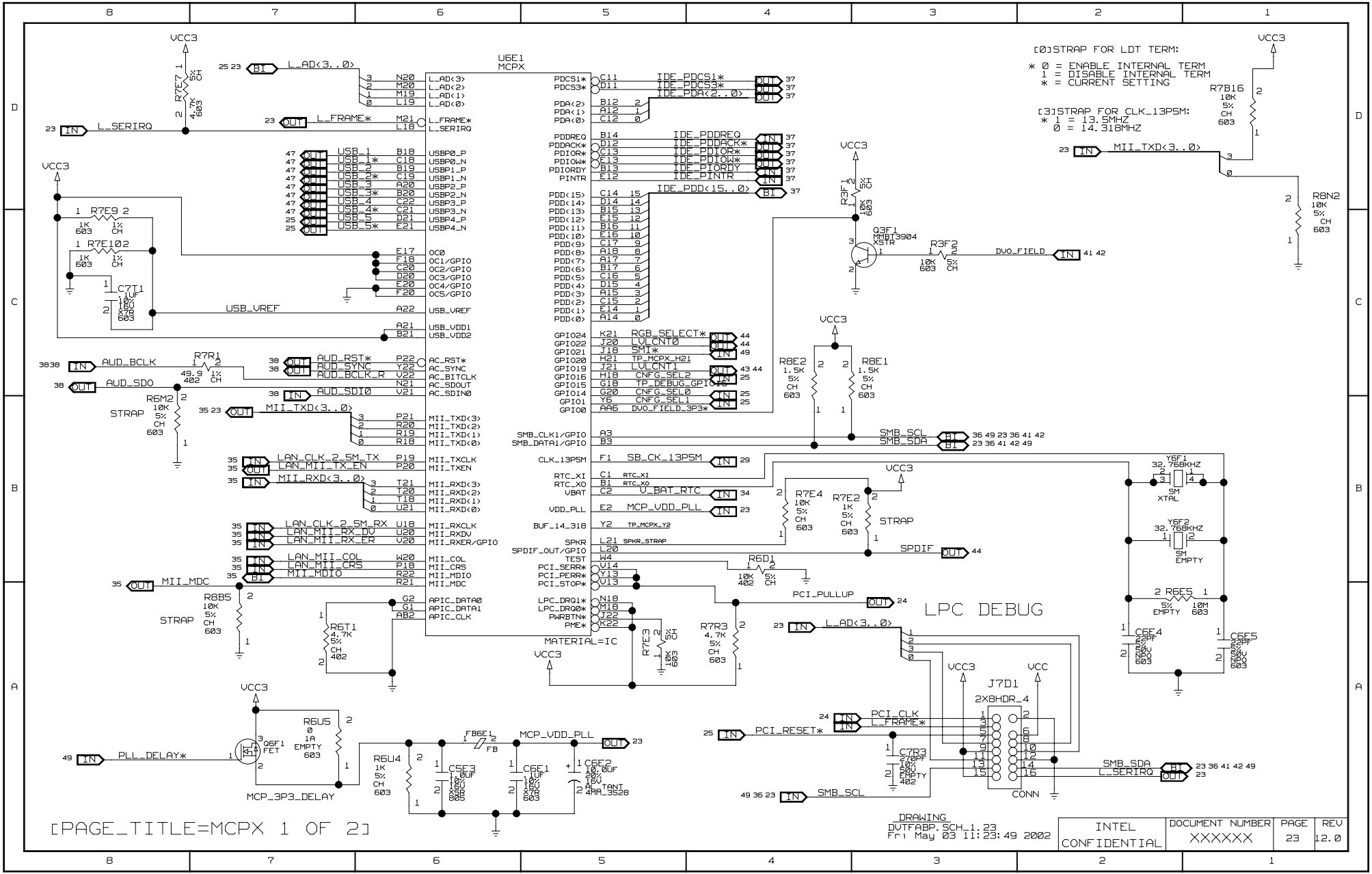
CHANGE COMPONENT  
TO CHEAPER PART.



[PAGE\_TITLE=NV2A DECOUPLING]

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Fri May 03 11:23:49 2002

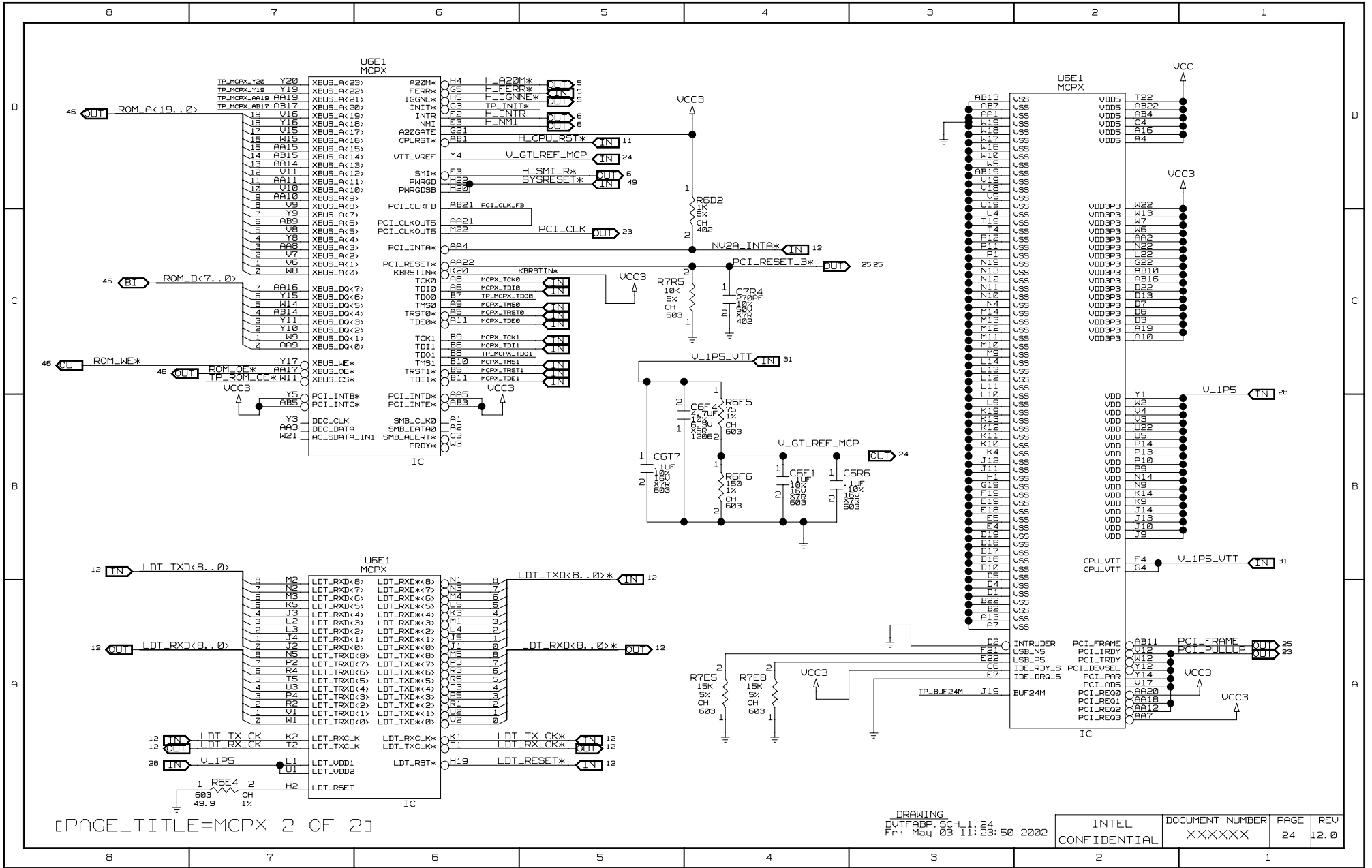
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	22	12.0



[PAGE\_TITLE=MCPX 1 OF 2]

DRAWING  
 DVT/FAB. SCH 11:23  
 Fri May 03 11:23:49 2002

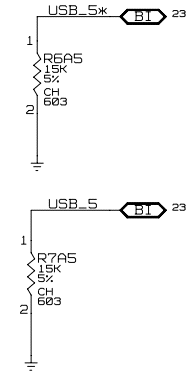
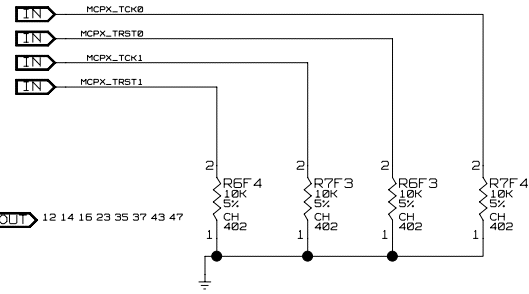
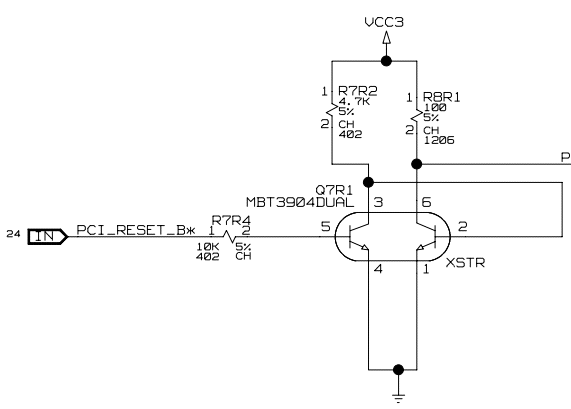
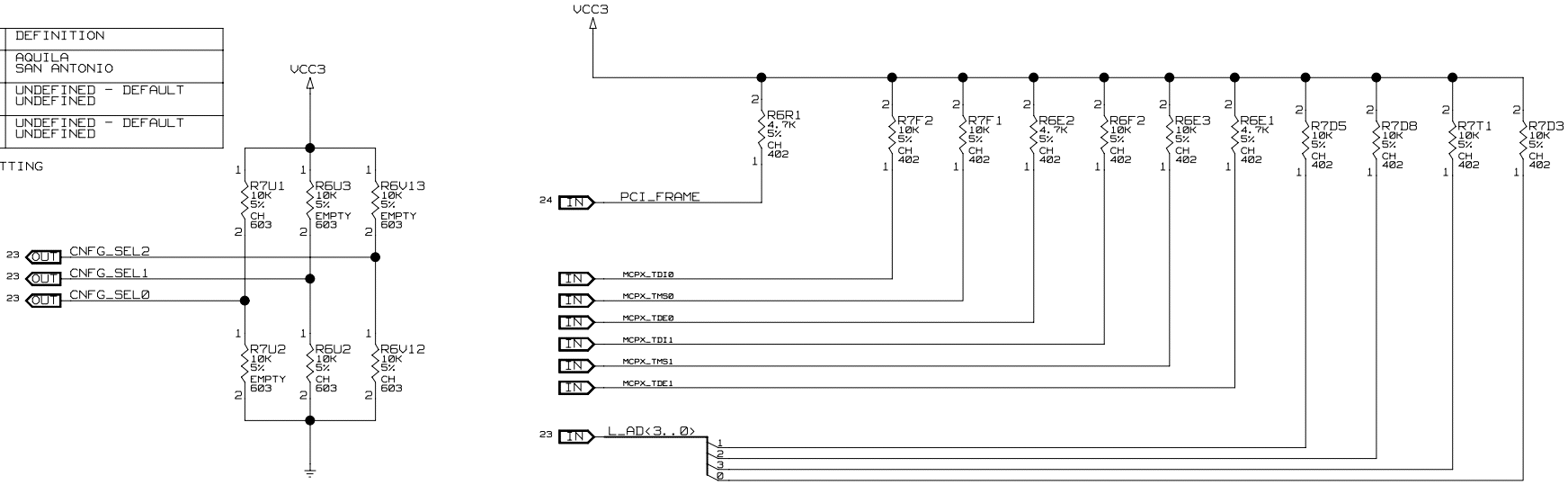
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	23	12.0





CNFG_SEL		DEFINITION
[0]	0 1*	AQUILA SAN ANTONIO
[1]	0* 1	UNDEFINED - DEFAULT UNDEFINED
[2]	0* 1	UNDEFINED - DEFAULT UNDEFINED

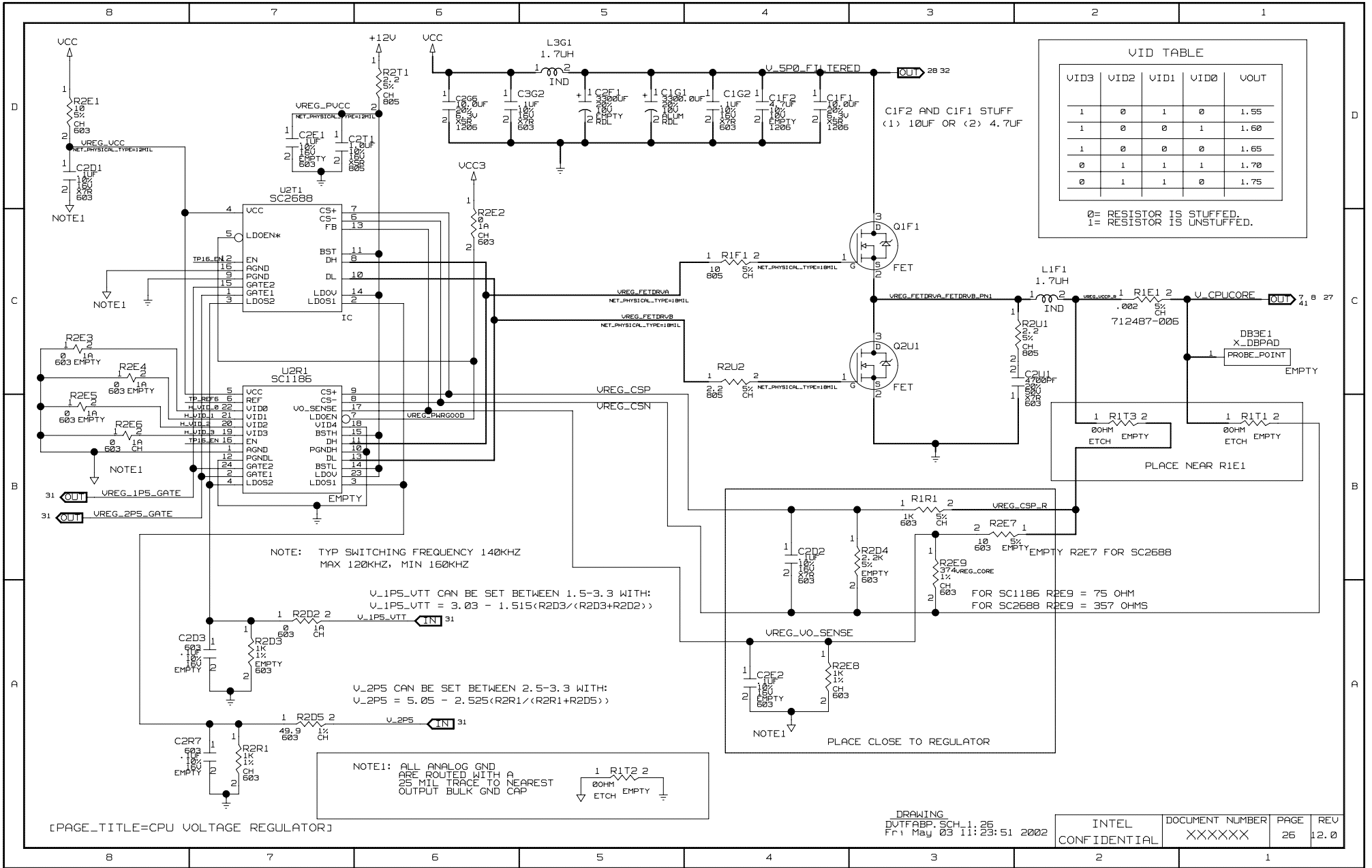
\* = CURRENT SETTING

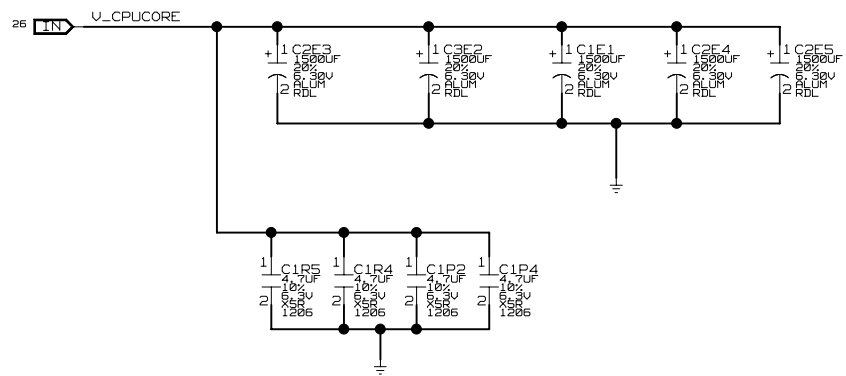


[PAGE\_TITLE=MCPX INPUT STRAPS]

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Fri May 03 11:23:51 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 25	REV 12.0
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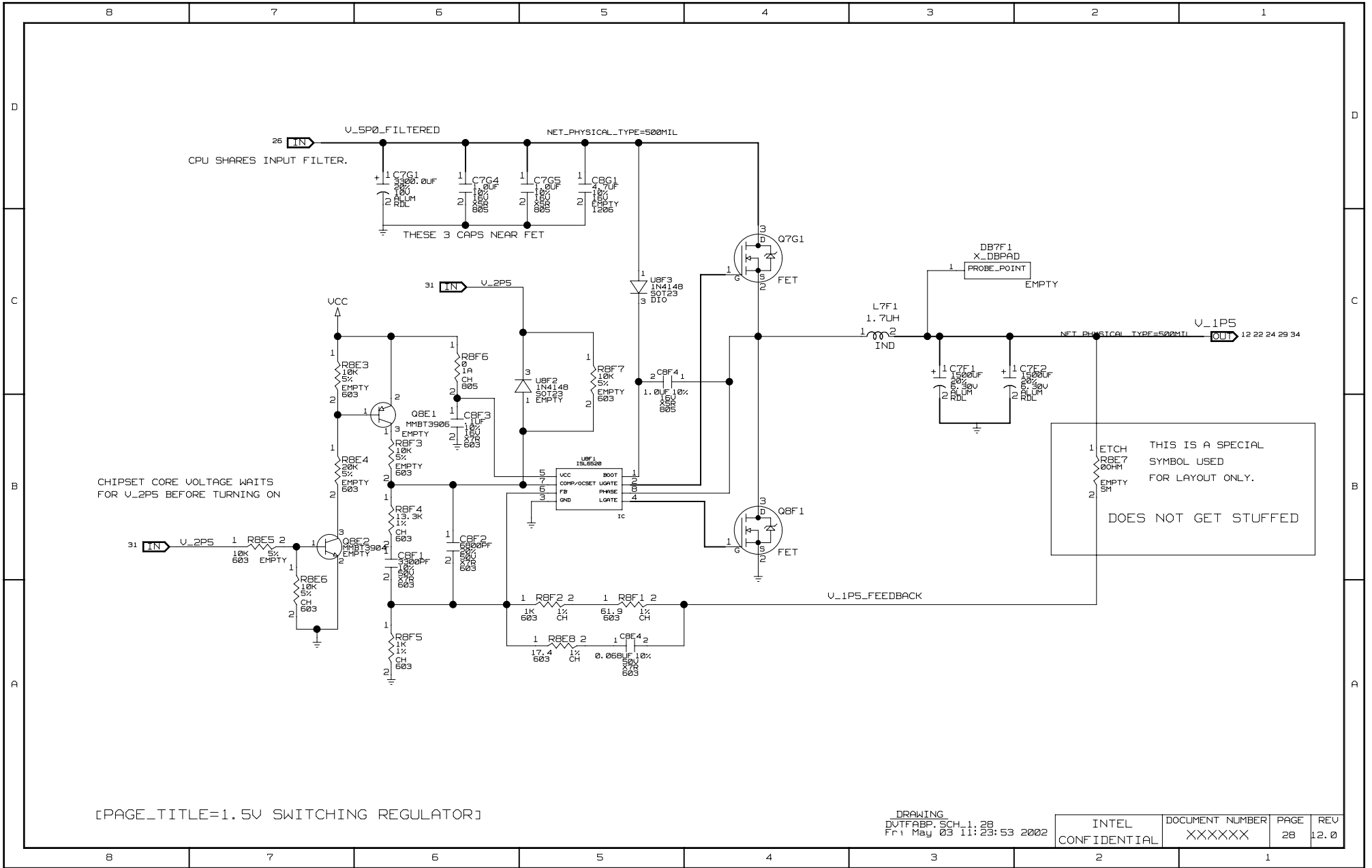


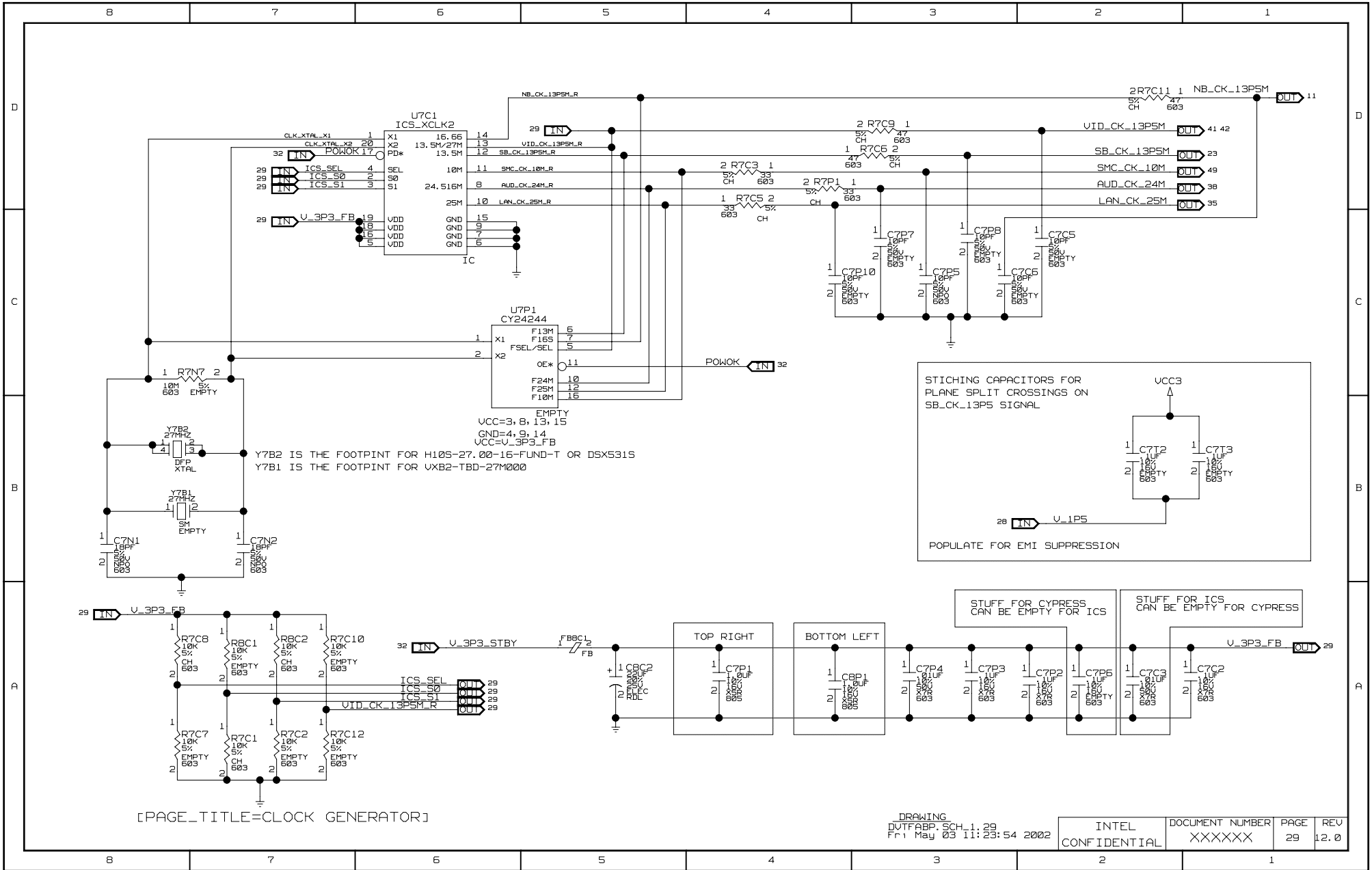


[PAGE\_TITLE=CPU VREG OUTPUT FILTER]

DRAWING  
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Fri May 03 11:23:52 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 27	REV 12.0
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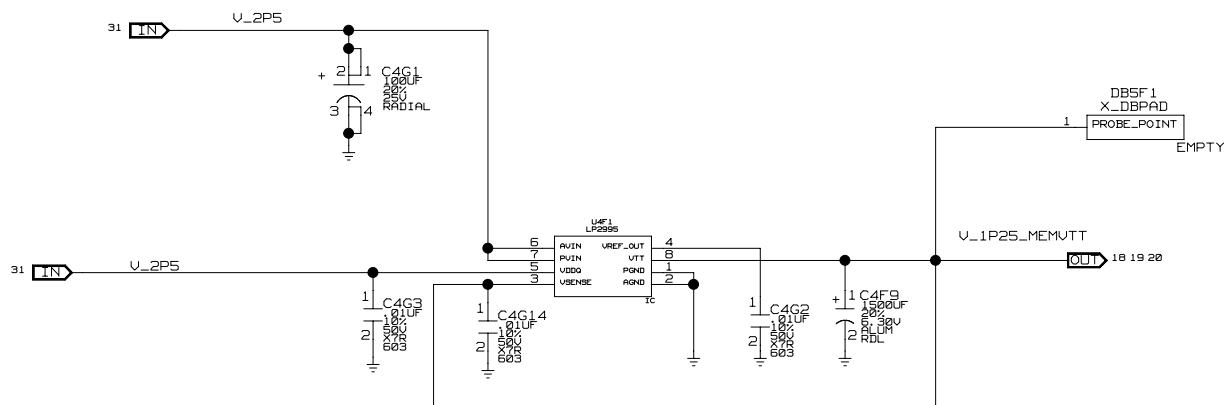


8 7 6 5 4 3 2 1

D

D

STUFF EITHER UCC3 OR UCC RESISTORS FOR DIFFERENT SEQUENCING



PLACE C301, C302, AND C303 NEAR REGULATOR PINS

[PAGE\_TITLE=1.25V LINEAR REGULATOR]

DRAWING  
DUTFABP\_SCH\_1\_30  
Pr: May 03 11:23:54 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 30	REV 12.0
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8 7 6 5 4 3 2 1

A

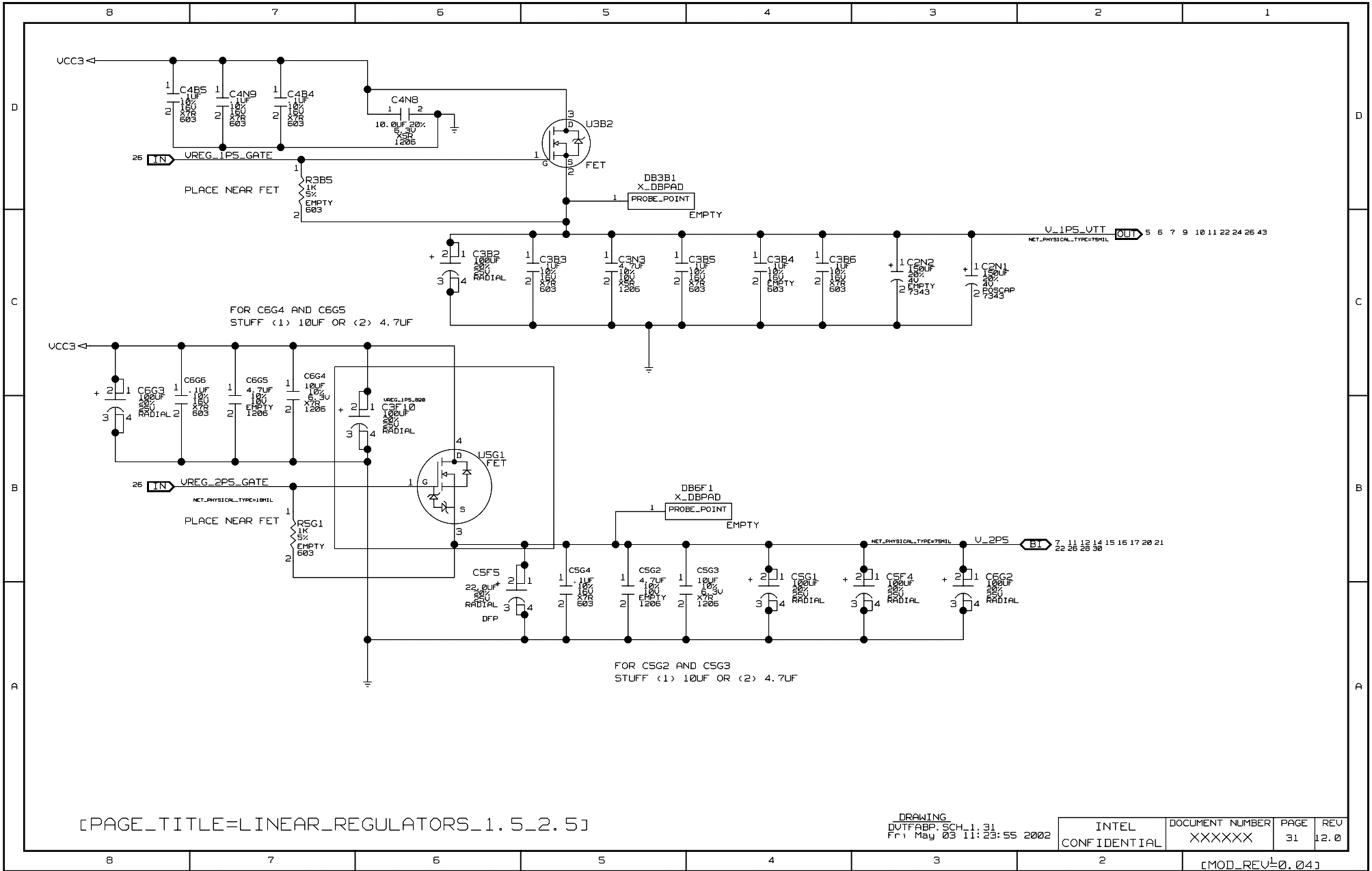
A

C

C

B

B

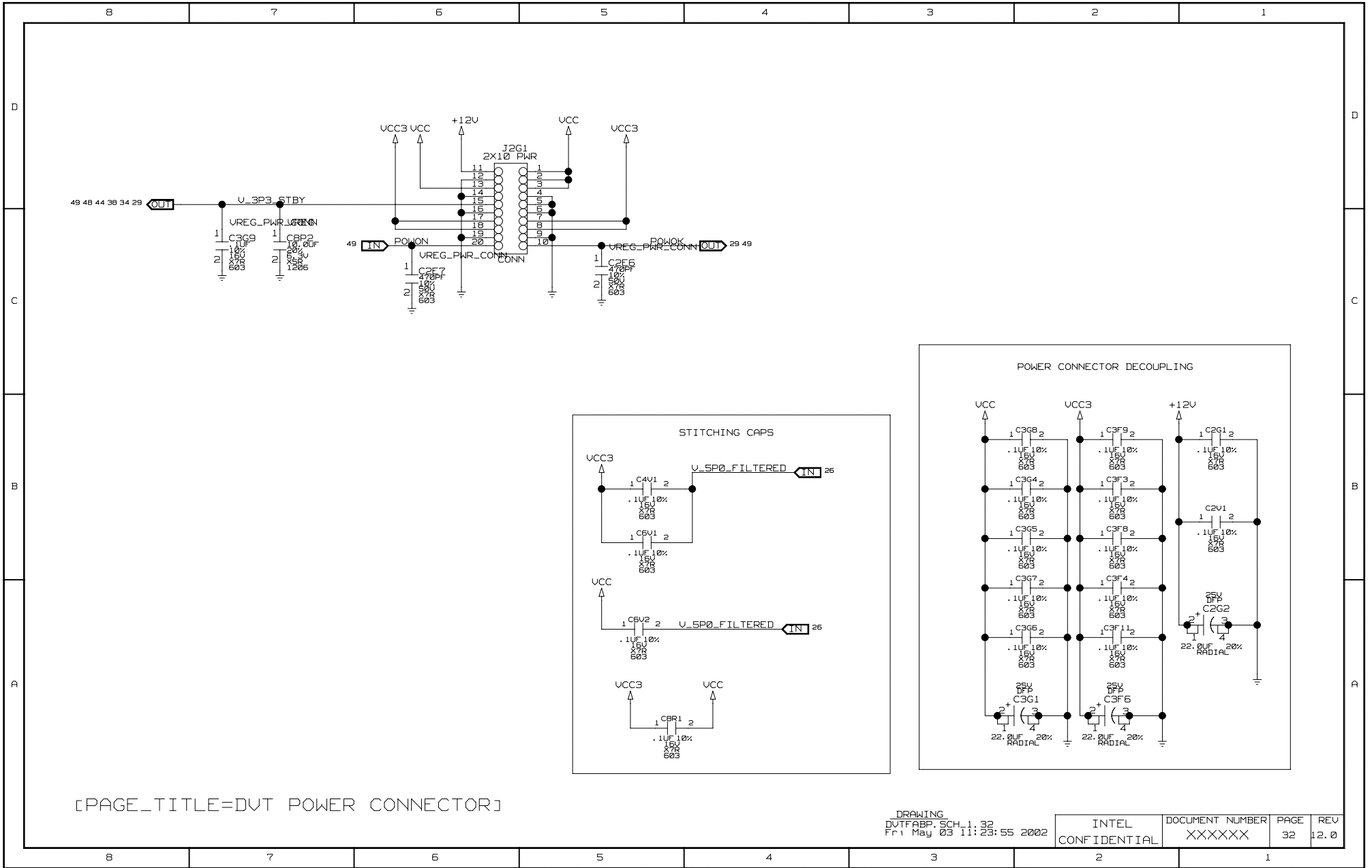


[PAGE\_TITLE=LINER\_REGULATORS\_1.5\_2.5]

DRAWING  
DVTFABP\_SCH\_11:31  
Fr: May 03 11:23:55 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 31	REV 12.0
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[MOD\_REV=0.04]



[PAGE\_TITLE=DVT POWER CONNECTOR]

DRAWING  
 DVTFABP\_SCH\_11:32  
 Fri May 03 11:23:55 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	32	12.0



D

C

B

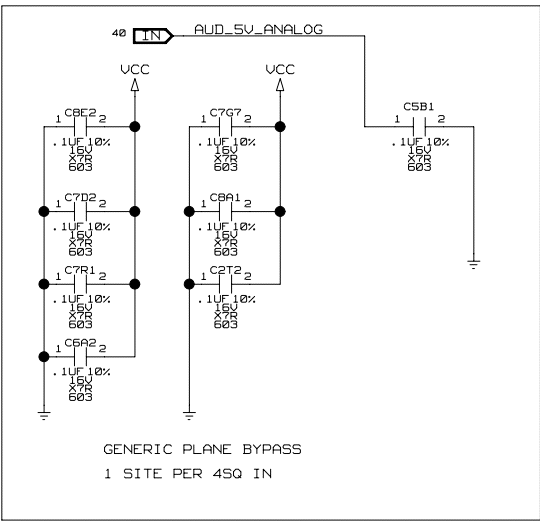
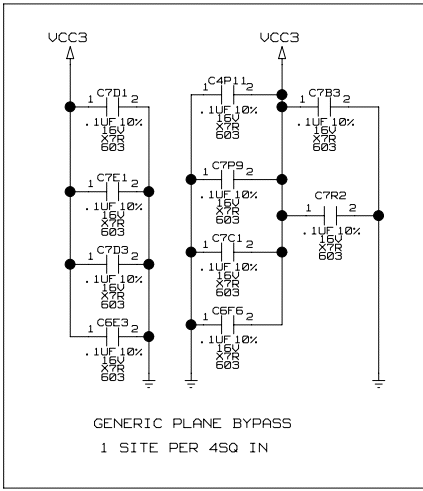
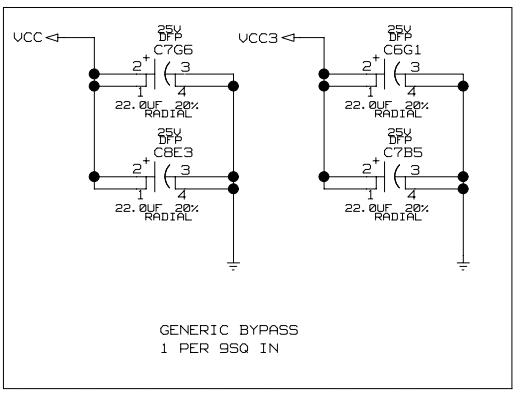
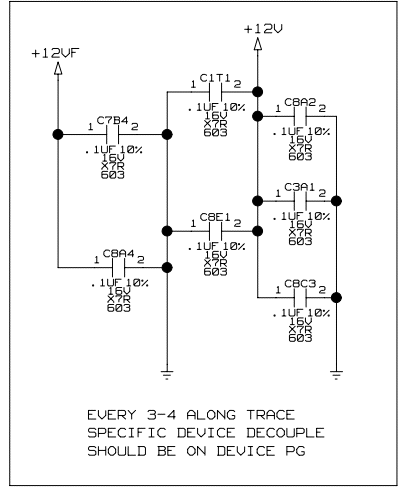
A

D

C

B

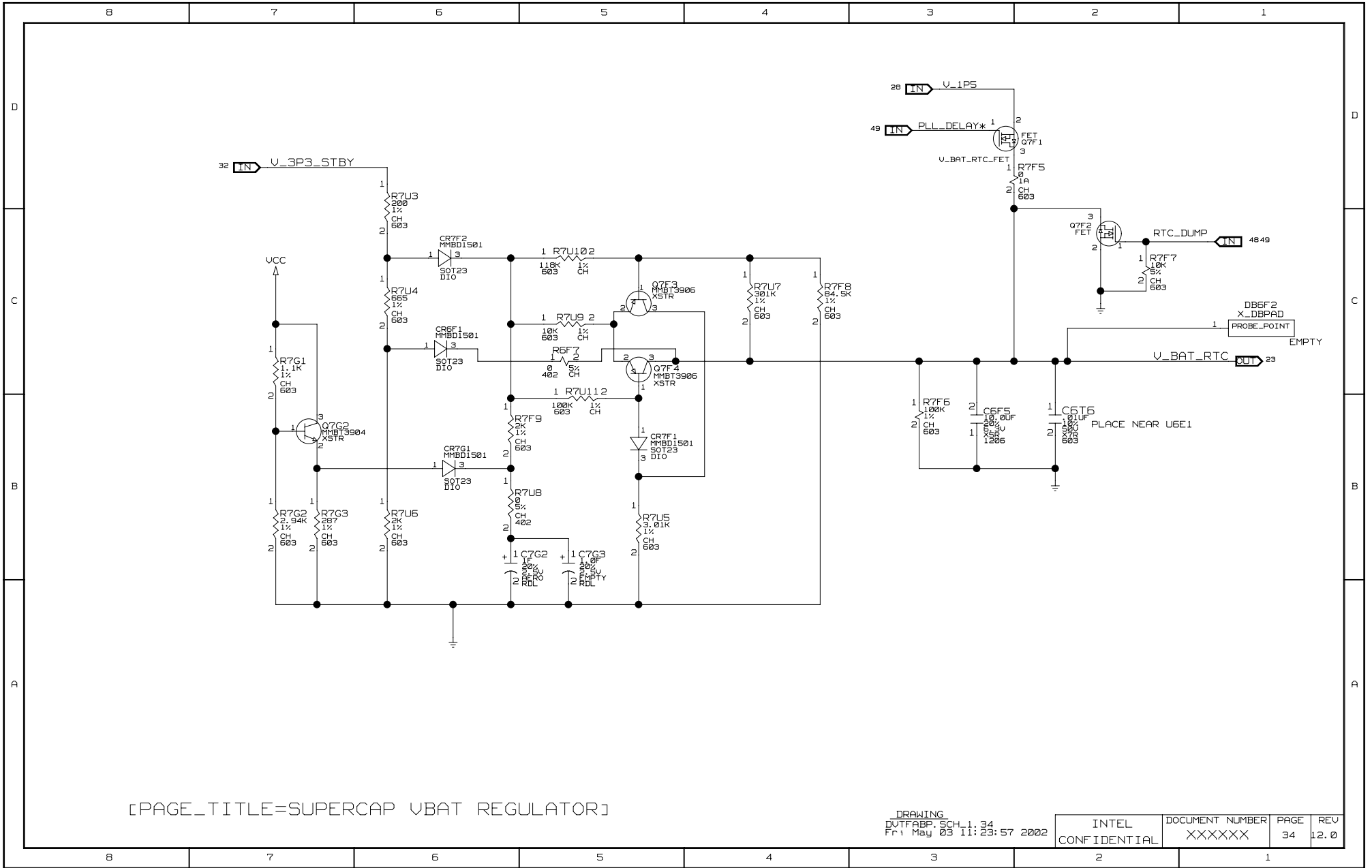
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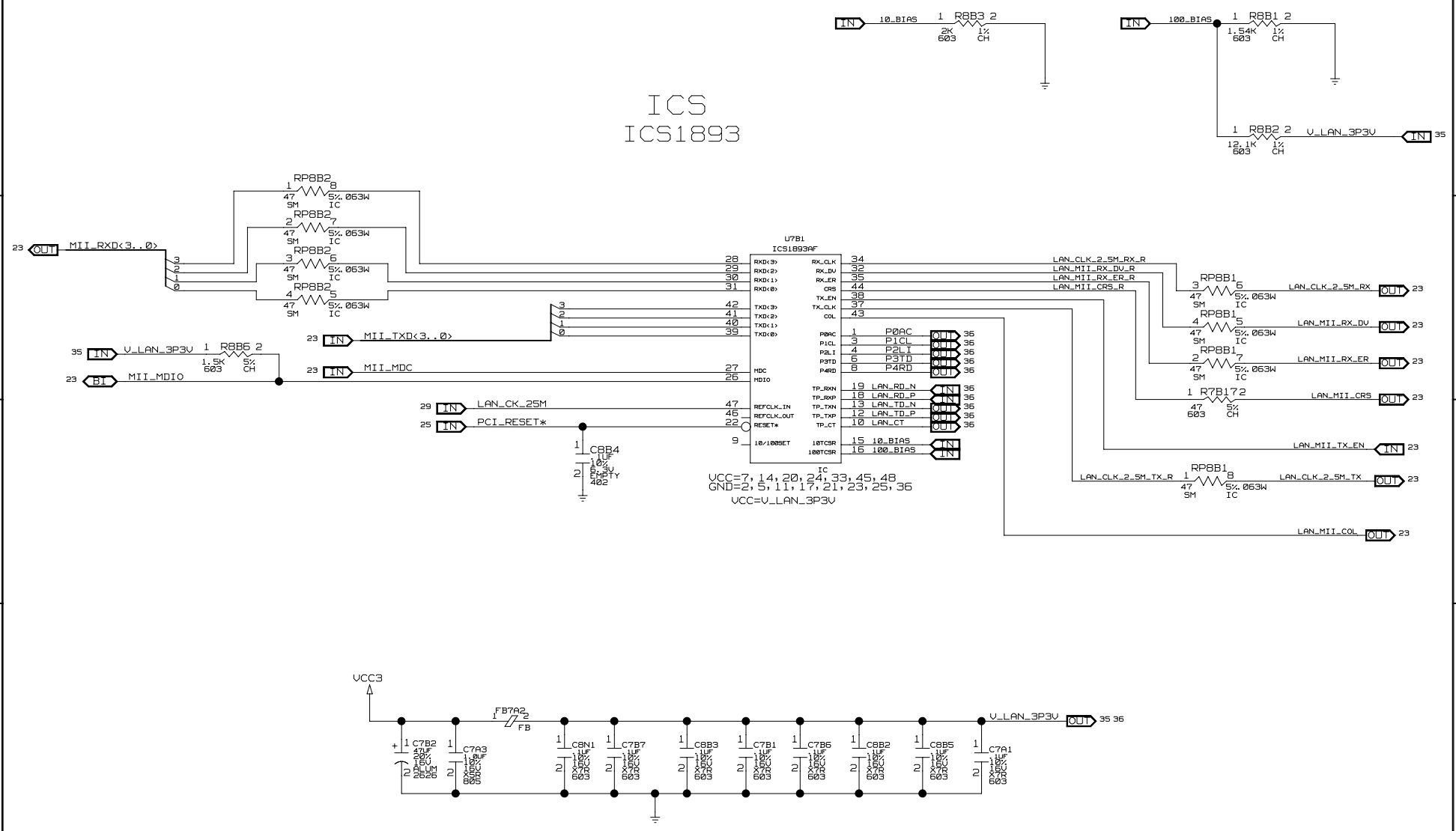
[PAGE\_TITLE=BULK DECOUPLING]

DRAWING  
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INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 33	REV 12.0
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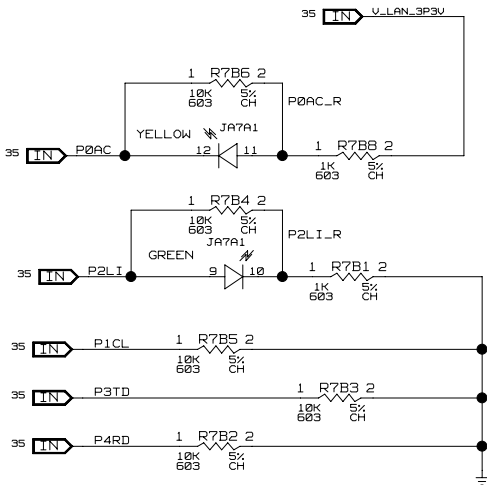
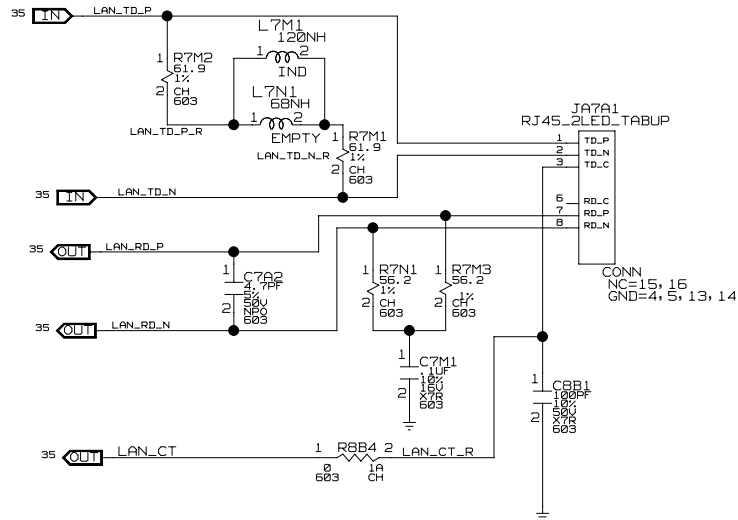


ICS  
ICS1893



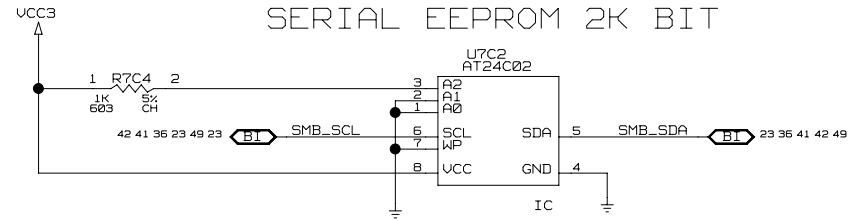
UCC=7, 14, 20, 24, 33, 45, 48  
GND=2, 5, 11, 17, 21, 23, 25, 36  
UCC=V\_LAN\_3P3V

# RJ45 SP JACK

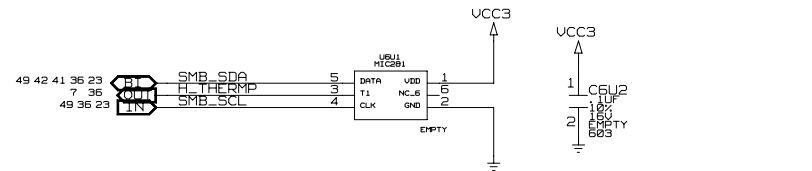
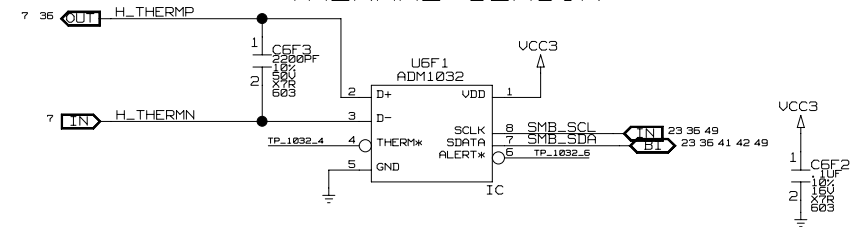


[PAGE\_TITLE=LAN JACK/THERMAL SENSE/EEPROM]

# SERIAL EEPROM 2K BIT



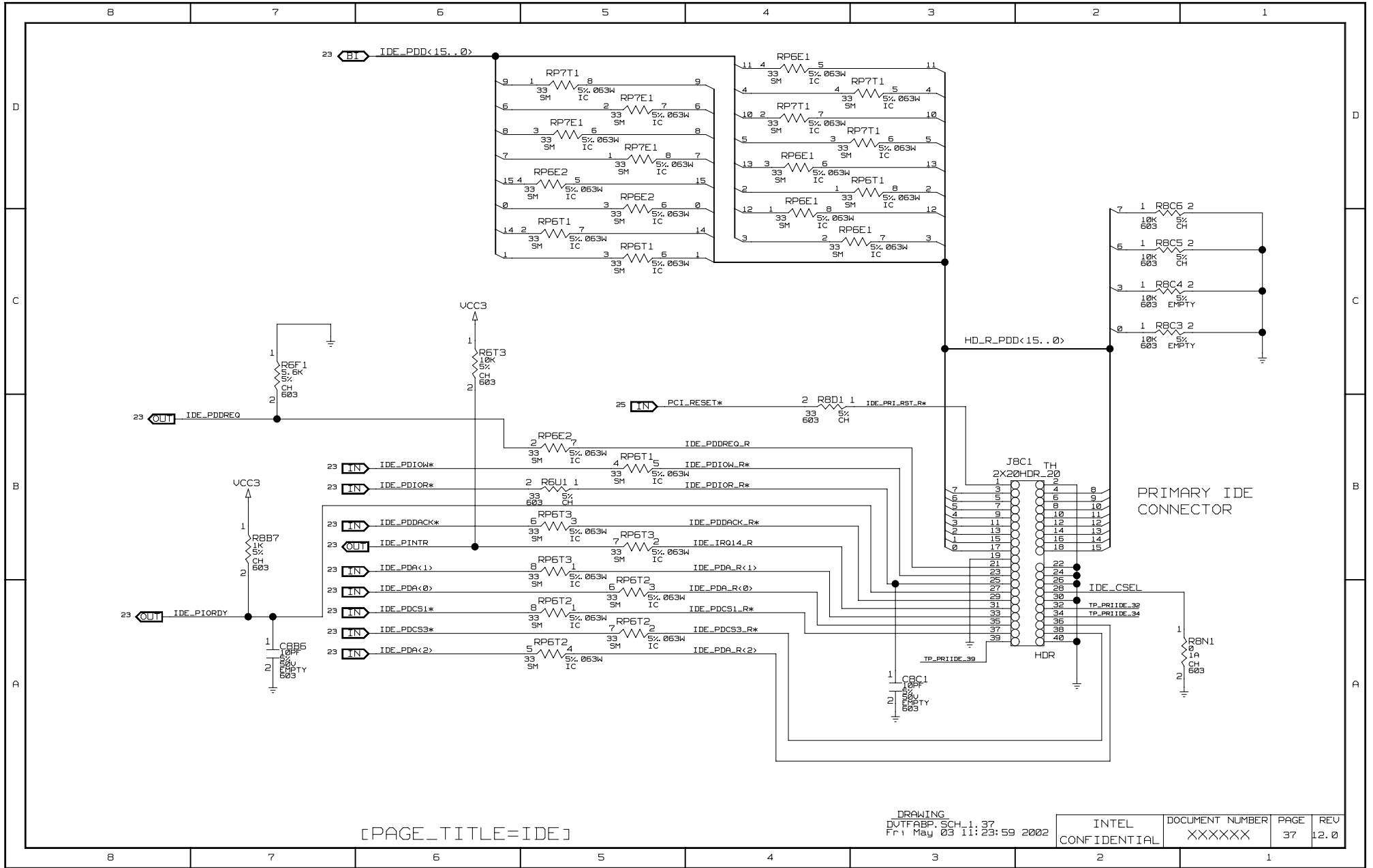
# THERMAL SENSOR



CAD NOTE:  
CONNECT THE GND  
ON CF101 TO PIN 2  
OF U5F100, BEFORE  
VIA TO GND

DRAWING  
DUTFARP\_SCH 1:36  
Fri May 03 11:23:58 2002

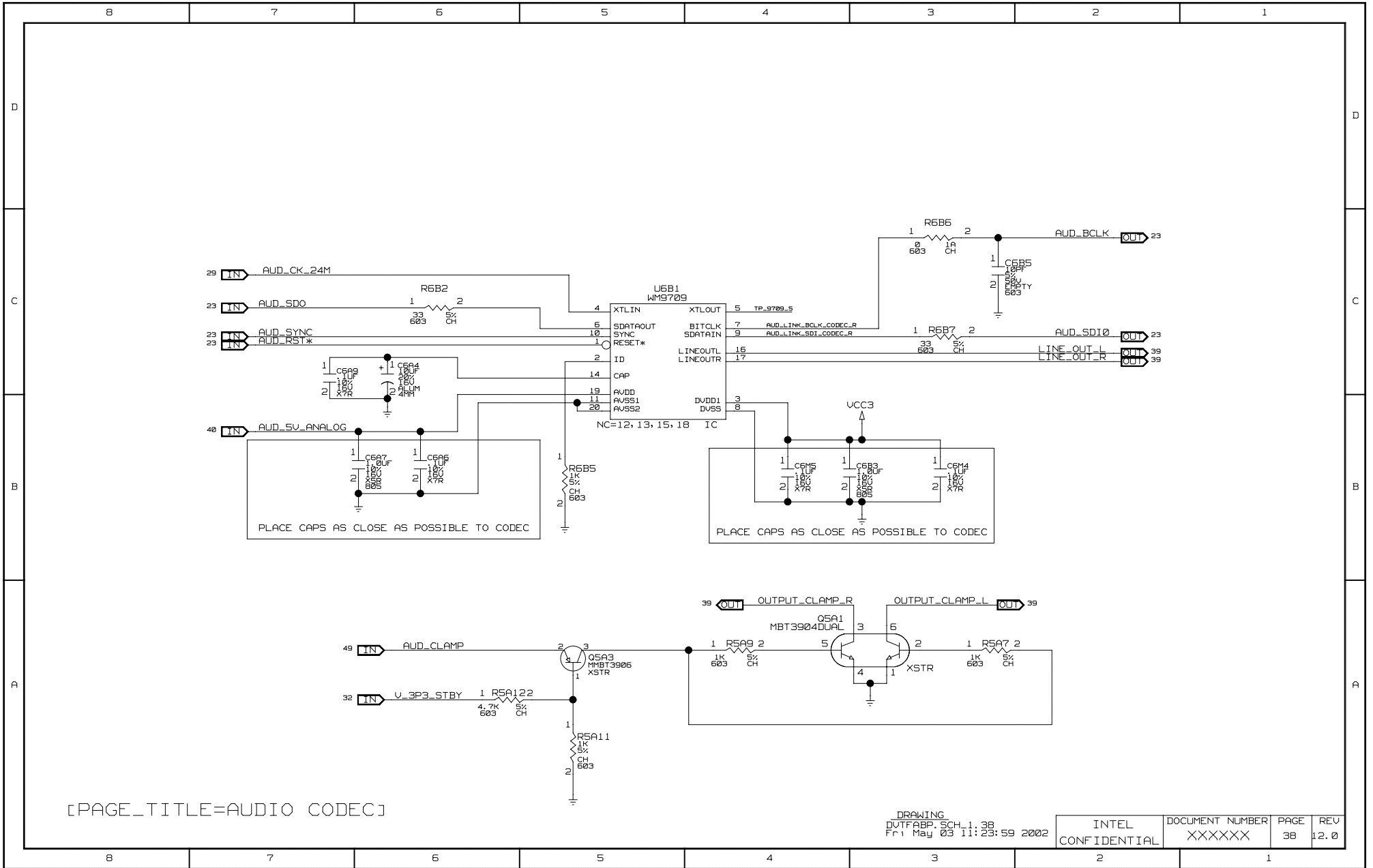
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 36	REV 12.0
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[PAGE\_TITLE=IDE]

DRAWING  
 DVTFABP\_SCH 1:37  
 Fri May 03 11:23:59 2002

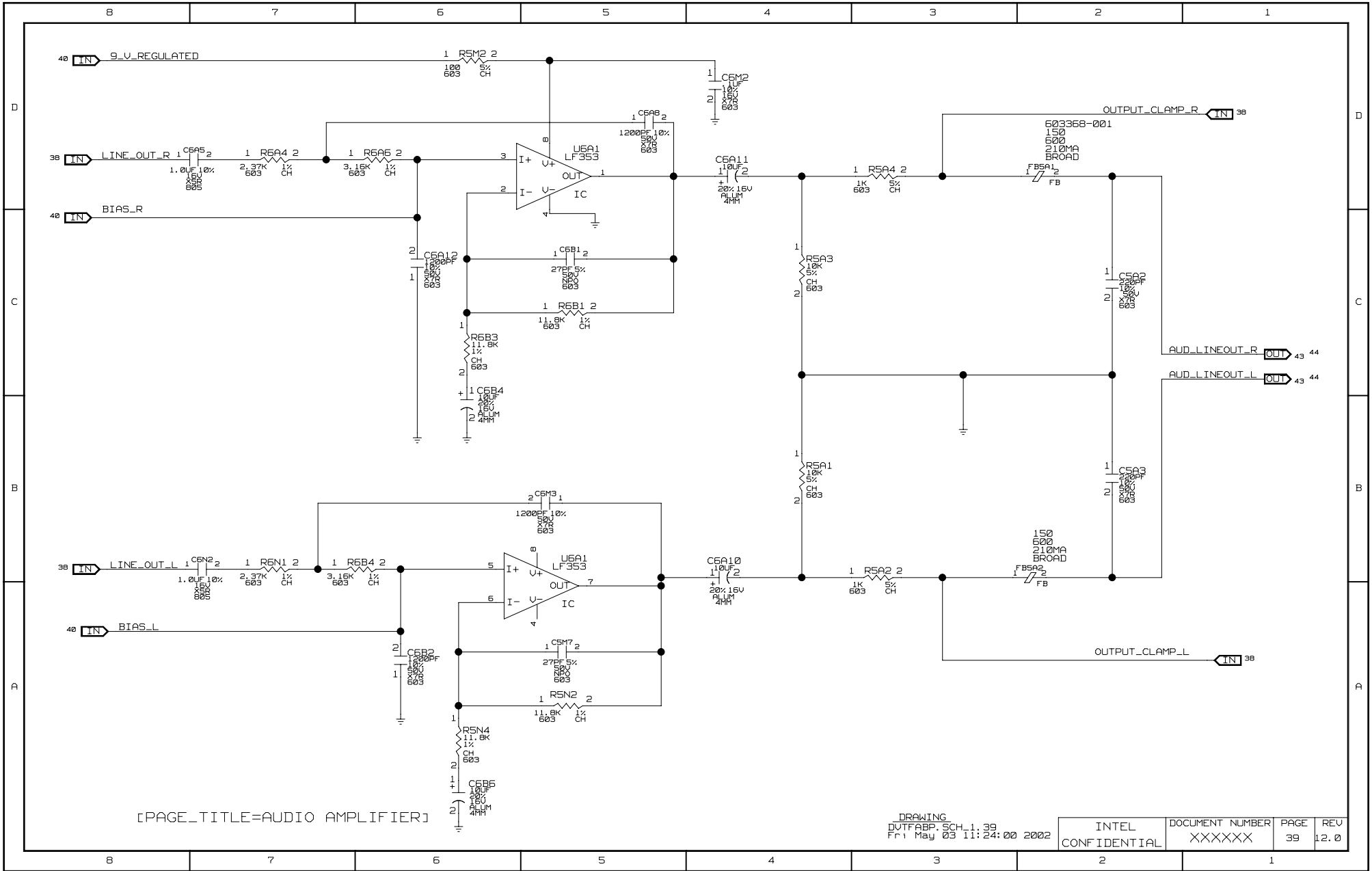
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	37	12.0



[PAGE\_TITLE=AUDIO CODEC]

DRAWING  
 DUTFABP\_SCH\_11:38  
 Fri May 03 11:23:59 2002

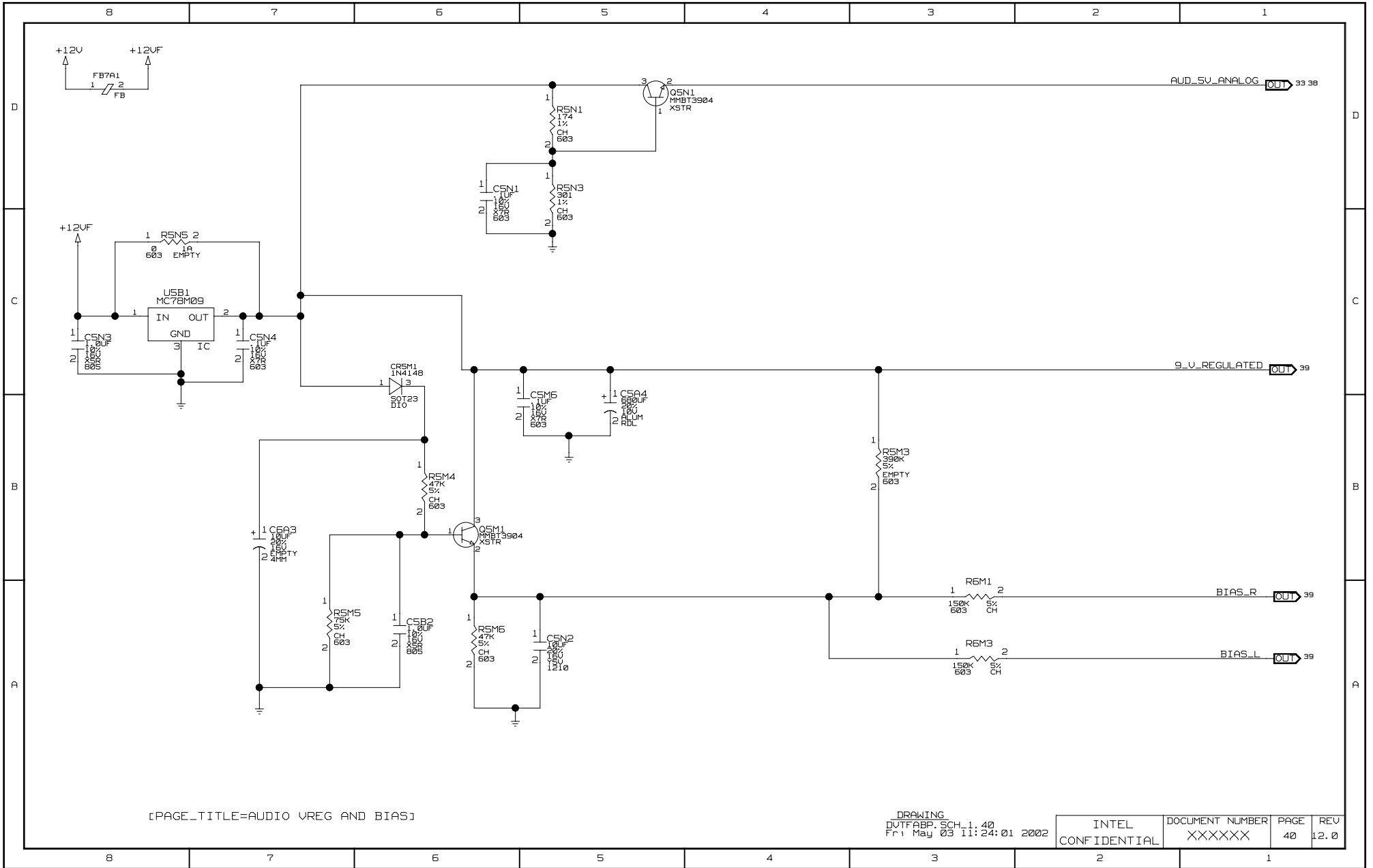
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	38	12.0



[PAGE\_TITLE=AUDIO AMPLIFIER]

DRAWING  
 DUTFABP\_SCH 1 39  
 Fri May 03 11:24:00 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 39	REV 12.0
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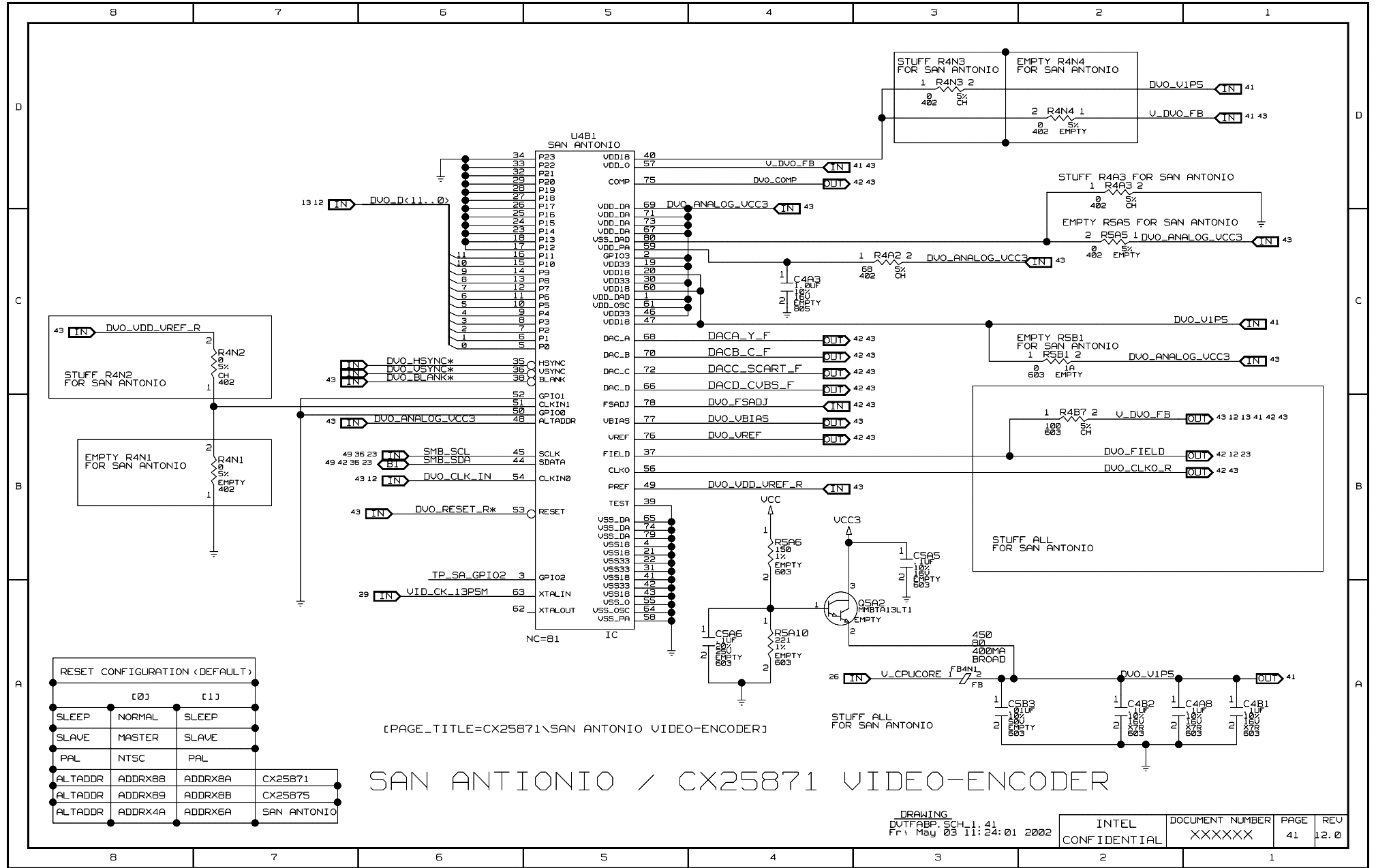


[PAGE\_TITLE=AUDIO VREG AND BIAS]

DRAWING  
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 Fri May 03 11:24:01 2002

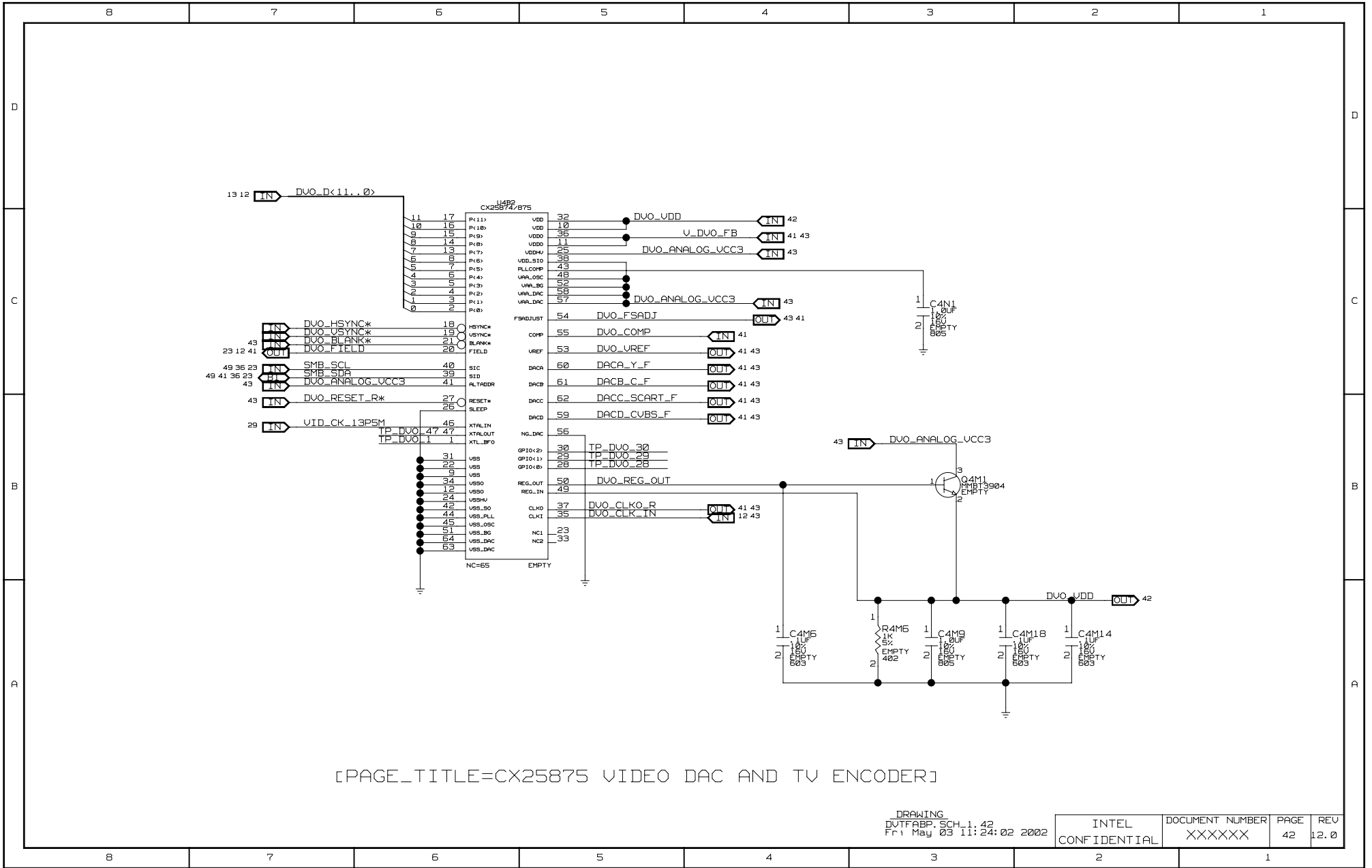
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 40	REV 12.0
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RESET CONFIGURATION (DEFAULT)

	[0]	[1]	
SLEEP	NORMAL	SLEEP	
SLAVE	MASTER	SLAVE	
PAL	NTSC	PAL	
ALTADDR	ADDRX8B	ADDRX8A	CX25871
ALTADDR	ADDRX89	ADDRX8B	CX25875
ALTADDR	ADDRX4A	ADDRX6A	SAN ANTONIO

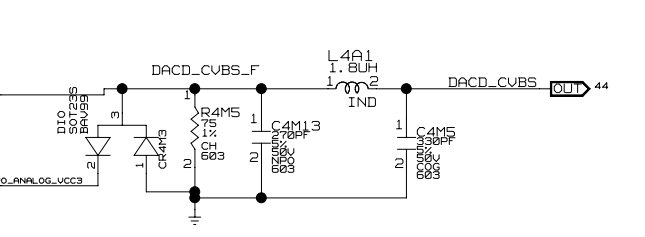
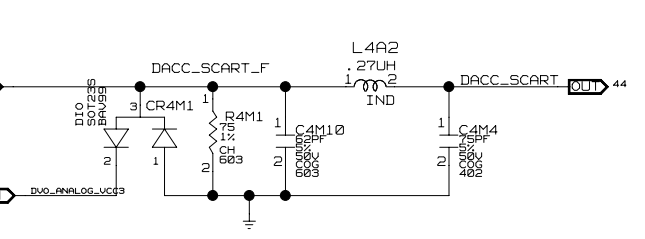
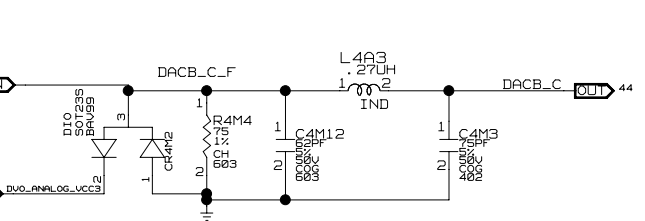
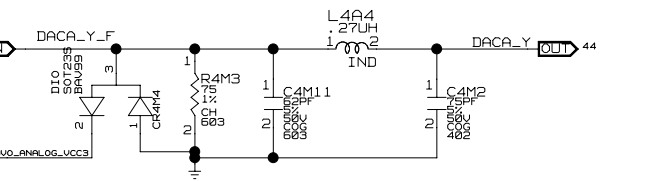
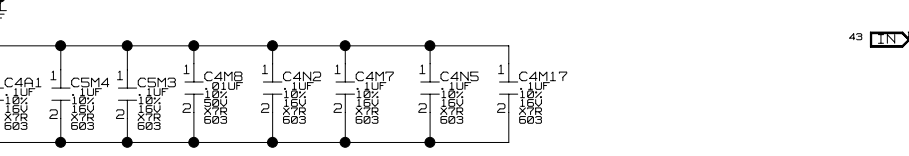
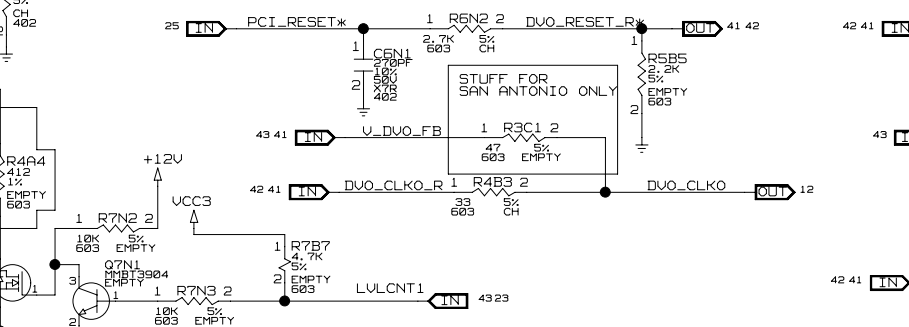
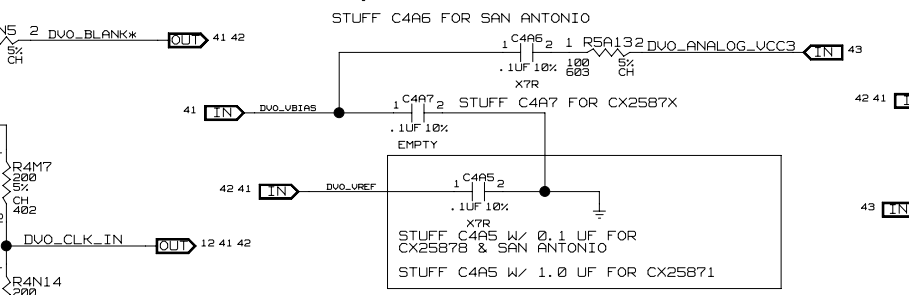
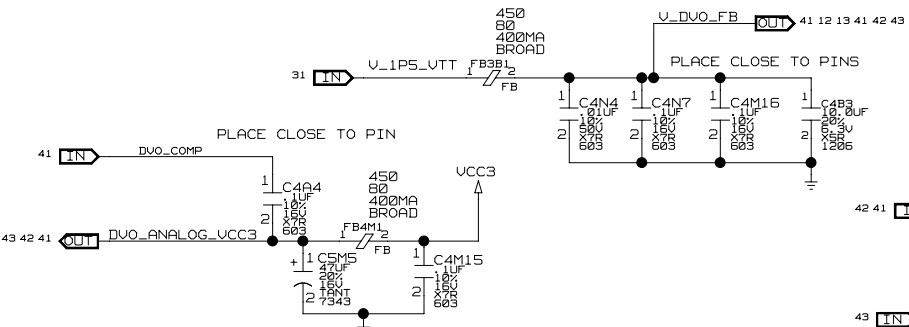


[PAGE\_TITLE=CX25875 VIDEO DAC AND TV ENCODER]

DRAWING  
 DVTFABP\_SCH\_11:42  
 Fri May 03 11:24:02 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 42	REV 12.0
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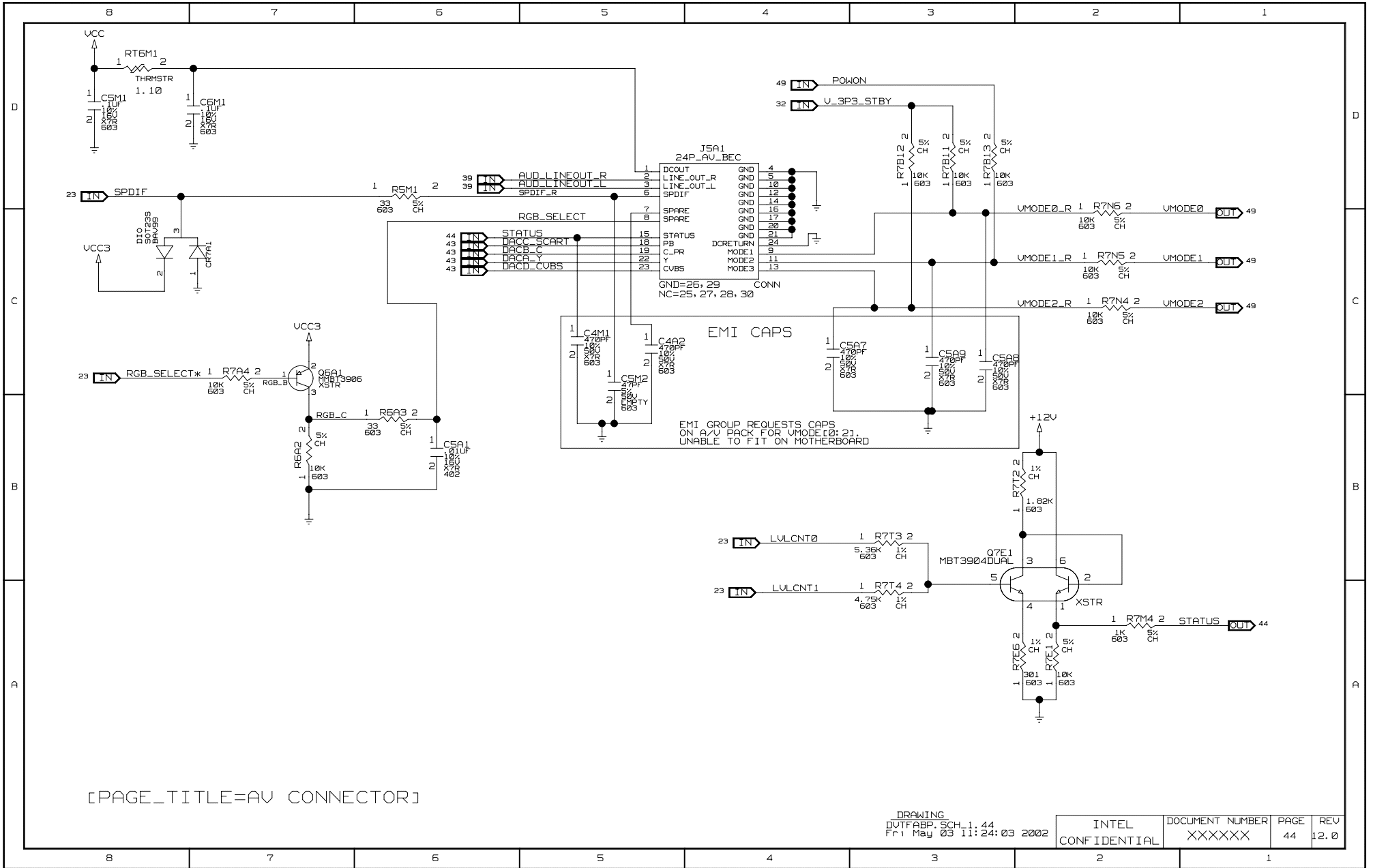
DAC	TVOUT	SCART	HDTV
A	Y(LUMA)	G	Y
B	C(CHROMA)	R	PR
C	N/A	B	PB
D	CVBS( COMP)	COMP	N/A



[PAGE\_TITLE=VIDEO DAC AND TV ENCODER]

DRAWING  
DVTFABP\_SCH\_11\_43  
Fri May 03 11:24:03 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	43	12.0



8 7 6 5 4 3 2 1

# LABELS

A19177-001  
LB8D1  
LABEL



1375X250\_TARGET

INTEL INTELLIGENT SERIAL NUMBER TARGET.

D

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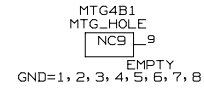
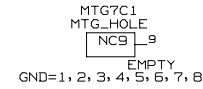
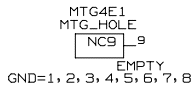
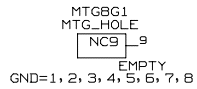
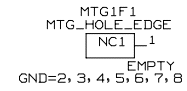
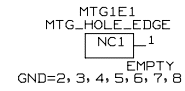
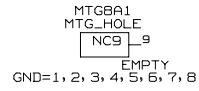
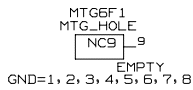
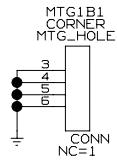
B

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# MOUNTING HOLES

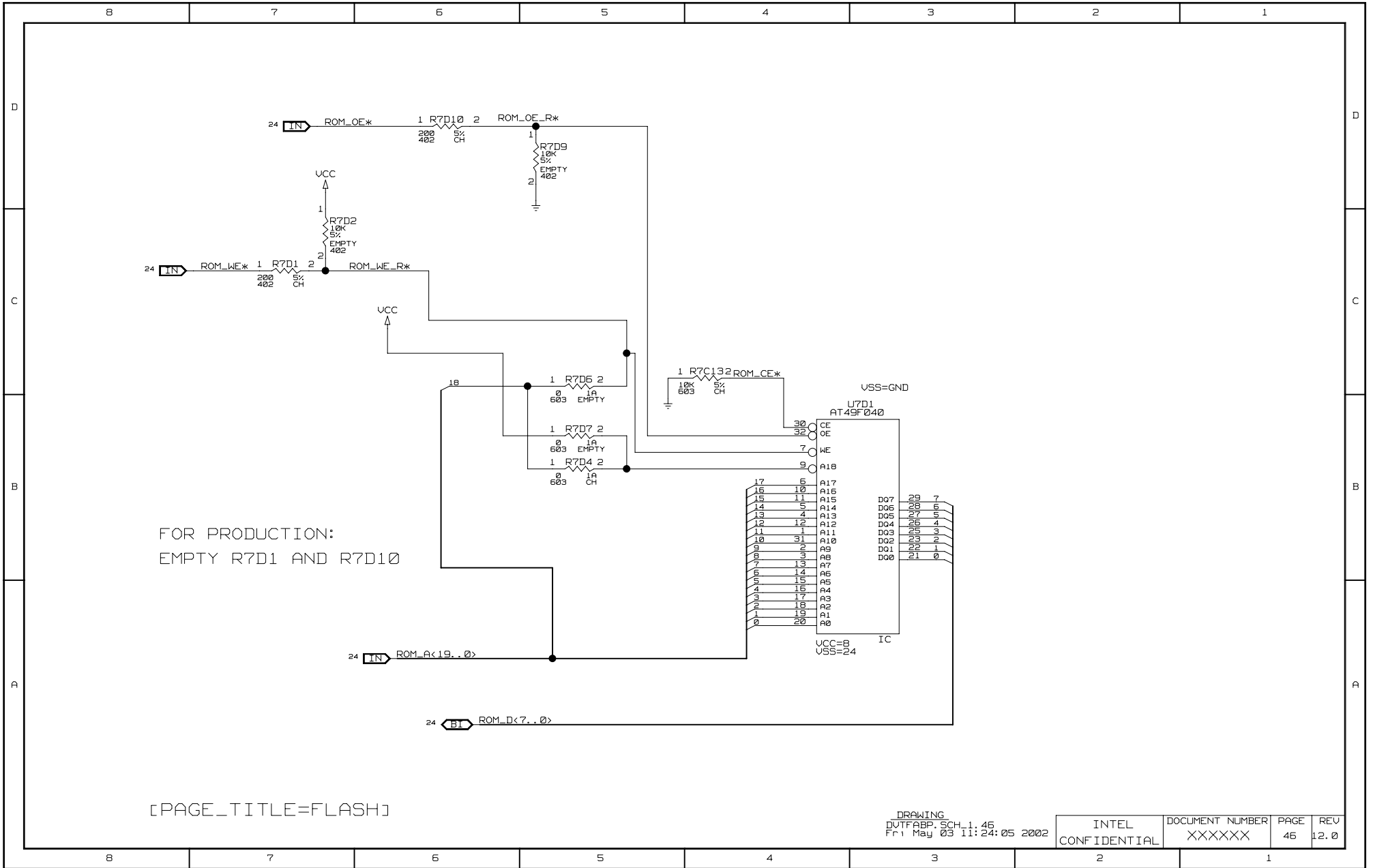


[PAGE\_TITLE=LABELS AND MOUNTING HOLES]

DRAWING  
DUTFABP\_SCH\_1\_45  
Fri May 03 11:24:04 2002

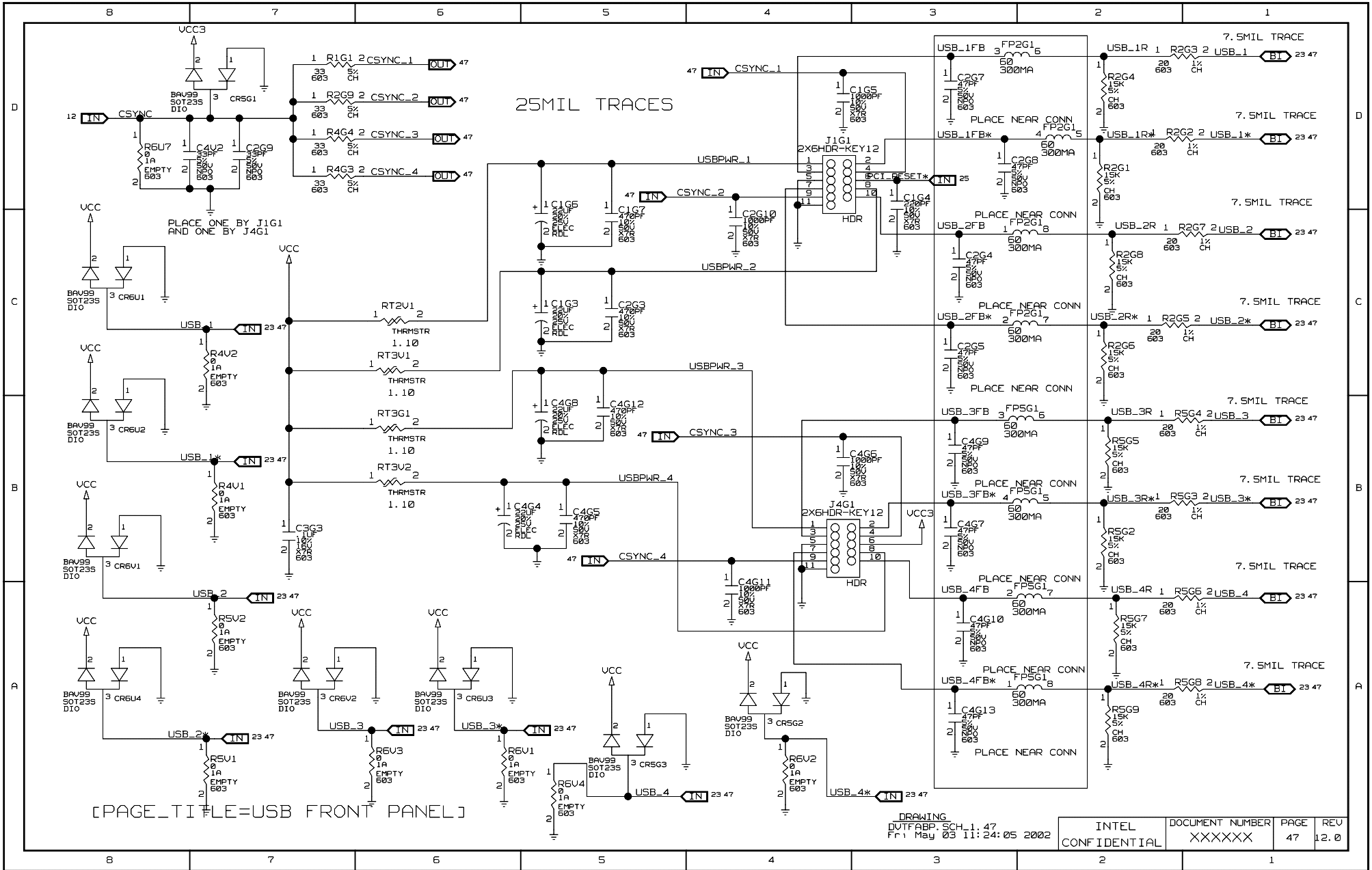
INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 45	REV 12.0
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8 7 6 5 4 3 2 1



DRAWING  
DVTFABP\_SCH\_1\_46  
Fr 1 May 03 11:24:05 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 46	REV 12.0
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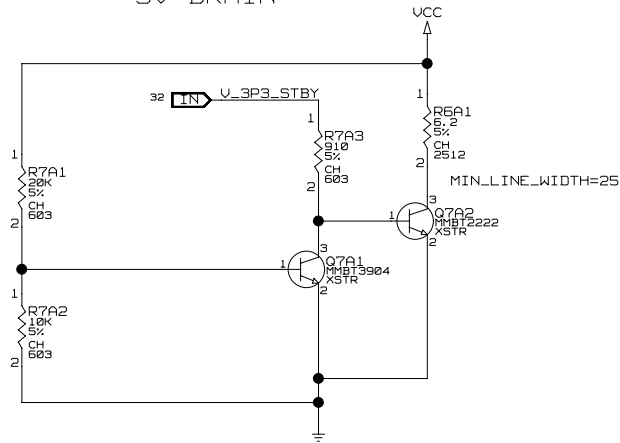


[PAGE\_TITLE=USB FRONT PANEL]

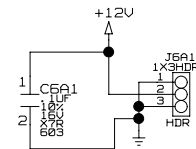
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DUTFABP\_SCH 1: 47  
Fr: May 03 11:24:05 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	47	12.0

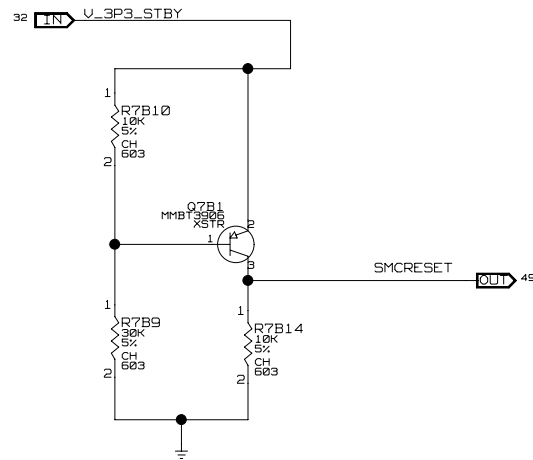
5V DRAIN



NV2A FAN HEADER



SMC BROWN OUT

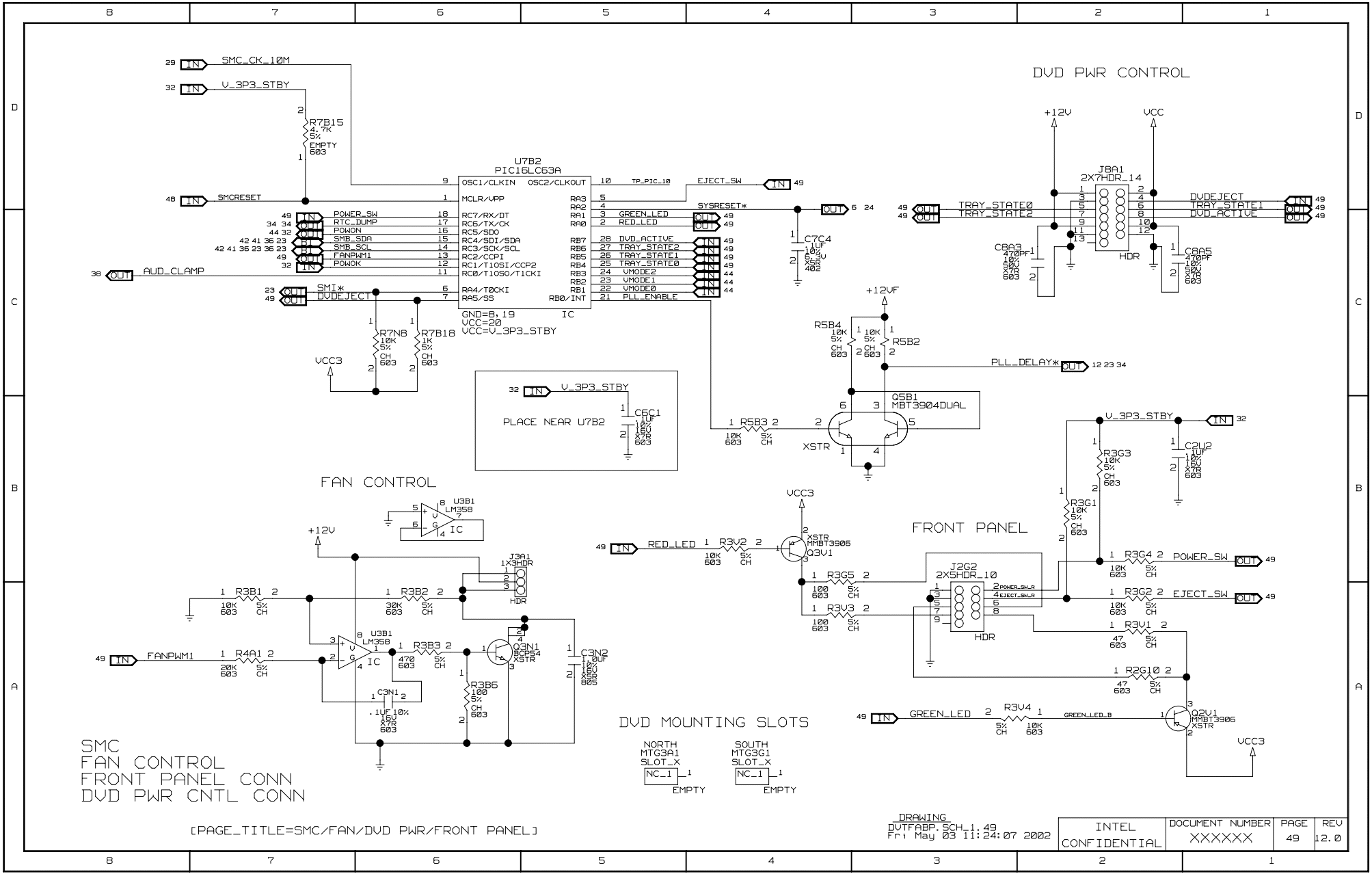


[PAGE\_TITLE=NV2A FAN/5V DRAIN/BROWN OUT]

DRAWING  
DVT/FABP\_SCH 11:24:06 2002  
Fri May 03 11:24:06 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 48	REV 12.0
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SMC  
FAN CONTROL  
FRONT PANEL CONN  
DVD PWR CNTL CONN

[PAGE\_TITLE=SMC/FAN/DVD PWR/Front Panel]

DVD MOUNTING SLOTS  
NORTH MTG3A1 SLOT\_X  
SOUTH MTG3G1 SLOT\_X  
[NC\_I]\_1 EMPTY

DRAWING  
DVTFABP\_SCH.1:49  
Fri May 03 11:24:07 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 49	REV 12.0
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# MCPX MUXED PIN ASSIGNMENT

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
A5	IDE_ADDR_S0	TRST0	Y20	PCI_AD0	XBUS_A23
E6	IDE_ADDR_S1	RESERVED	Y19	PCI_AD1	XBUS_A22
B5	IDE_ADDR_S2	TRST1	AA19	PCI_AD2	XBUS_A21
C5	IDE_CS1_S*	RESERVED	AB17	PCI_AD3	XBUS_A20
B4	IDE_CS3_S*	RESERVED	AA17	PCI_AD4	XBUS_OE*
A6	IDE_DACK_S*	TDI0	Y17	PCI_AD5	XBUS_WE*
B8	IDE_DATA_S0	TD01	V17	PCI_AD6	RESERVED
C8	IDE_DATA_S1	RESERVED	AA16	PCI_AD7	XBUS_D07
D8	IDE_DATA_S2	RESERVED	V16	PCI_AD8	XBUS_A19
B9	IDE_DATA_S3	TCK1	AB15	PCI_AD9	XBUS_A14
D9	IDE_DATA_S4	RESERVED	AA15	PCI_AD10	XBUS_A15
B10	IDE_DATA_S5	TMS1	Y15	PCI_AD11	XBUS_D06
E10	IDE_DATA_S6	RESERVED	W15	PCI_AD12	XBUS_A16
B11	IDE_DATA_S7	TDE1*	V15	PCI_AD13	XBUS_A17
A11	IDE_DATA_S8	TDE0*	AB14	PCI_AD14	XBUS_D04
E11	IDE_DATA_S9	RESERVED	AA14	PCI_AD15	XBUS_A13
C10	IDE_DATA_S10	RESERVED	Y11	PCI_AD16	XBUS_D03
E9	IDE_DATA_S11	RESERVED	W11	PCI_AD17	XBUS_CE*
A9	IDE_DATA_S12	TMS0	V11	PCI_AD18	XBUS_A12
C9	IDE_DATA_S13	RESERVED	AA10	PCI_AD19	XBUS_A9
E8	IDE_DATA_S14	RESERVED	Y10	PCI_AD20	XBUS_D02
A8	IDE_DATA_S15	TCK0	V10	PCI_AD21	XBUS_A10
E7	IDE_DRQ_S	RESERVED	AB9	PCI_AD22	XBUS_A6
B6	IDE_INTR_S	TDI1	AA9	PCI_AD23	XBUS_D00
B7	IDE_IOR_S*	TD00	W9	PCI_AD24	XBUS_D01
C7	IDE_IOW_S*	RESERVED	V9	PCI_AD25	XBUS_A8
C6	IDE_RDY_S	RESERVED	AA8	PCI_AD26	XBUS_A3
			Y8	PCI_AD27	XBUS_A4
			W8	PCI_AD28	XBUS_A0
Y21	PCI_GNT0*	RESERVED	V8	PCI_AD29	XBUS_A5
Y18	PCI_GNT1*	RESERVED	V7	PCI_AD30	XBUS_A2
AA13	PCI_GNT2*	RESERVED	V6	PCI_AD31	XBUS_A1

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
Y7	PCI_GNT3*	RESERVED	Y16	PCI_CBE0*	XBUS_A18
Y6	PCI_GNT4*	RESERVED	W14	PCI_CBE1*	XBUS_D05
V12	PCI_IRDY*	RESERVED	AA11	PCI_CBE2*	XBUS_A11
Y14	PCI_PAR	RESERVED	Y9	PCI_CBE3*	XBUS_A7
Y13	PCI_PERR*	RESERVED	Y12	PCI_DEUSEL*	RESERVED
AA20	PCI_REQ0*	RESERVED	AB11	PCI_FRAME*	RESERVED
AA18	PCI_REQ1*	RESERVED	V14	PCI_SERR*	RESERVED
AA12	PCI_REQ2*	RESERVED	V13	PCI_STOP*	RESERVED
AA7	PCI_REQ3*	RESERVED	W12	PCI_TRDY*	RESERVED
AA6	PCI_REQ4*	RESERVED			

## VOLTAGE RAILS

RAIL	TYPICAL (V)	
V_CPUCORE	1.7V (CPU DEPENDENT)	
VCC	5V	
VCC3	3.3V	
V_3P3_STBY	3.3V STANDBY	
V_2P5	2.65V	
V_1P5	1.65V	
V_1P5_VTT	1.5V	
V_1P25_MEMVTT	1.325V	

[PAGE\_TITLE=MCPX MUXED PIN ASSIGNMENT]

DRAWING  
DVTFABP\_SCH\_1\_50  
Fri May 03 11:24:07 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 50	REV 12.0
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\*\*\* Signal Cross-Reference \*\*\*  
 --- for the entire design ---

9\_V\_REGULATED 40C1 39D8  
 10\_BIAS 35B3 35D4  
 100\_BIAS 35B3 35D2  
 AUD\_SV\_ANALOG 40D1 33B4 3BB7  
 AUD\_BCLK 38C2 23C8  
 AUD\_BCLK\_R 23C7  
 AUD\_CK\_24M 29D2 38C7  
 AUD\_CK\_24M\_R 29D5  
 AUD\_CLAMP 49C8 39A6  
 AUD\_LINEOUT\_L 39C1 44D6  
 AUD\_LINEOUT\_R 39C1 44D6  
 AUD\_LINK\_BCLK\_CODEC\_R 38C4  
 AUD\_LINK\_SDI\_CODEC\_R 38C4  
 AUD\_RST\* 23C7 38C7  
 AUD\_SDI0 38C2 23C7  
 AUD\_SDO 23C8 38C7  
 AUD\_SYNC 23C7 38C7  
 BGA2\_BRE00\_C6 6B4  
 BIAS\_L 40A1 39A8  
 BIAS\_R 40A1 39C8  
 CK\_H\_133M\_CPU 11B5 6A7  
 CK\_H\_133M\_CPU\_BUF 6B5 6B8  
 CK\_H\_133M\_CPU\_R 6B5  
 CK\_H\_133M\_FB 11B6  
 CK\_H\_133M\_FB\_R 11B6  
 CK\_H\_PICCLK 11B6  
 CK\_H\_PICCLK\_R 11B4 6B5  
 CLK\_XTAL\_X1 29D7  
 CLK\_XTAL\_X2 29D7  
 CNFG\_SEL0 25C7 23C4  
 CNFG\_SEL1 25C7 23B4  
 CNFG\_SEL2 25C7 23C4  
 CSYNC 12B2 47D8  
 CSYNC\_1 47D6 47D4  
 CSYNC\_2 47D6 47D5  
 CSYNC\_3 47D6 47B5  
 CSYNC\_4 47D6 47B5  
 DAC\_A\_Y 43D1 44C6  
 DAC\_A\_Y\_F 41C4 42C4 43D3  
 DAC\_B\_C 43C1 44C6  
 DAC\_B\_C\_F 41C4 42C4 43C3  
 DAC\_SCART 43B1 44C6  
 DAC\_SCART\_F 41C4 42B4 43B3  
 DACD\_CUBS 43A1 44C6  
 DACD\_CUBS\_F 41C4 42B4 43A3  
 DUDEJECT 49C7 49D1  
 DUDEACTIVE 49C1 49C4  
 DVO\_ANALOG\_VCC3 43D7 41B6 41C1 41C2 41C4 42B3 42C4  
 42C7 43A3 43A8 43B3 43C3 43C4  
 DVO\_BLANK\* 43C5 41C6 42C7  
 DVO\_CLK0 43A4 12C2  
 DVO\_CLK0\_R 41B2 42B4 43A6  
 DVO\_CLK\_IN 12C2 43B6 41B6 42B4  
 DVO\_COMP 41D4 42C4 43D7  
 DVO\_D(11..0) 12C2 13D7 41D6 42D7  
 DVO\_FIELD 41B2 42C7 12C2 23C2  
 DVO\_FIELD\_3P3\* 23B5  
 DVO\_FSADJ 42C4 43B8 41B4  
 DVO\_HSYNC\* 12C2 41C6 42C7  
 DVO\_REG\_OUT 42B5  
 DVO\_RESET\_R\* 43B4 41B6 42B7  
 DVO\_VIPS 41A1 41C1 41D1  
 DVO\_VBIAS 41B4 43C6  
 DVO\_VDD 42A2 42C4  
 DVO\_VDD\_VREF\_R 43B8 41B4 41C8  
 DVO\_VREF 41B4 42C4 43C6  
 DVO\_VSYNC\* 12C2 41C6 42C7

EJECT\_SW 49A1 49D4  
 EJECT\_SW\_R 49A3  
 FANPM1 49C7 49A8  
 GREEN\_LED 49C4 49A3  
 GREEN\_LED\_B 49A2  
 HD\_R\_PDD(15..0) 37C3  
 H\_LA\*(31..3) 5D3 11D5  
 H\_LA20M\* 24D5 5B3  
 H\_LA20M\_R\* 5B5  
 H\_LADS\* 6C2 11C6  
 H\_LBNR\* 6B5 11C6  
 H\_LBPRI\* 11C6 6B5  
 H\_LCPU\_RST\* 11C5 24D5  
 H\_LCPU\_RST\_R\* 11C4 6C7  
 H\_LD\*(63..0) 5D7 11D8  
 H\_LDBSY\* 6B2 11C6  
 H\_DEFER\* 11C6 6B2  
 H\_DRDY\* 6B2 11C6  
 H\_FERR\* 5B3 24D5  
 H\_HIT\* 6C2 11C6  
 H\_HITM\* 6B2 11B6  
 H\_IGNNE\* 24D5 5B3  
 H\_INIT\* 6C5  
 H\_INTR 24A6 6B7  
 H\_INTR\_R 6B5  
 H\_LOCK\* 6B5 11B6  
 H\_LNMI 24D5 6B7  
 H\_LNMI\_R 6B5  
 H\_LPREQ\* 10B2 5B4  
 H\_LREQ\*(4..0) 6B5 11A8  
 H\_LRS\*(2..0) 11B5 6B2  
 H\_LSMI\* 6A1 6B6  
 H\_LSMI\_R\* 24D5 6A3  
 H\_LTC 10B7 5B4  
 H\_TDI 10B2 5B4  
 H\_THERM1 7C7 36A3 36C4  
 H\_THERM2 36B3 36C4 7C7  
 H\_TMS 10B7 5B4  
 H\_TRDY\* 11B6 6B2  
 H\_TRST\* 10B2 5B4  
 H\_VID\_0 26B8  
 H\_VID\_1 26B8  
 H\_VID\_2 26B8  
 H\_VID\_3 26B8  
 ICS\_S0 29A6 29D7  
 ICS\_S1 29A6 29D7  
 ICS\_SEL 29A6 29D7  
 IDE\_CSEL 37A2  
 IDE\_LIRQ14\_R 37B4  
 IDE\_PDA\*(2..0) 23D4 37A6 37B6  
 IDE\_PDA\_R(2..0) 37A4 37B4  
 IDE\_PDCS1\* 23D4 37A6  
 IDE\_PDCS1\_R\* 37A4  
 IDE\_PDCS3\* 23D4 37A6  
 IDE\_PDCS3\_R\* 37A4  
 IDE\_PDD(15..0) 23D4 37D6  
 IDE\_PDDACK\* 23D4 37B6  
 IDE\_PDDACK\_R\* 37B4  
 IDE\_PDDREQ 37B8 23D4  
 IDE\_PDDREQ\_R 37B5  
 IDE\_PD1OR\* 23D4 37B6  
 IDE\_PD1OR\_R\* 37B5  
 IDE\_PD1OW\* 23D4 37B6  
 IDE\_PD1OW\_R\* 37B5  
 IDE\_PINTR 37B6 23D4  
 IDE\_PIORDY 37A8 23D4  
 IDE\_PRI\_RST\_R\* 37B3  
 KBRSTIN\* 24C5  
 LAN\_CK\_25M 29D2 35B6  
 LAN\_CK\_25M\_R 29D6

LAN\_CLK\_2\_5M\_RX 35C1 23B7  
 LAN\_CLK\_2\_5M\_RX\_R 35C3  
 LAN\_CLK\_2\_5M\_TX 35B1 23B7  
 LAN\_CLK\_2\_5M\_TX\_R 35B3  
 LAN\_CT 35B3 36B8  
 LAN\_CT\_R 36B7  
 LAN\_MII\_COL 35B1 23B7  
 LAN\_MII\_CRS 35C1 23B7  
 LAN\_MII\_CRS\_R 35C3  
 LAN\_MII\_RX\_DV 35C1 23B7  
 LAN\_MII\_RX\_DV\_R 35C3  
 LAN\_MII\_RX\_ER 35C1 23B7  
 LAN\_MII\_RX\_ER\_R 35C3  
 LAN\_MII\_TX\_EN 23B7 35B1  
 LAN\_RD\_N 36C8 35C3  
 LAN\_RD\_P 36C8 35C3  
 LAN\_TD\_N 35B3 36C8  
 LAN\_TD\_N\_R 36D7  
 LAN\_TD\_P 35B3 36D8  
 LAN\_TD\_P\_R 36D8  
 LDT\_RESET\* 12A4 24A5  
 LDT\_RXD\*(8..0) 24A5 12B5  
 LDT\_RXD\*(B..0) 24A8 12C4  
 LDT\_RX\_CK 24A7 12B2  
 LDT\_RX\_CK\* 24A5 12B2  
 LDT\_TXD\*(8..0) 12B4 24B5  
 LDT\_TXD\*(B..0) 12C4 24B8  
 LDT\_TX\_CK 12B2 24A7  
 LDT\_TX\_CK\* 12B2 24A5  
 LINE\_OUT\_L 38C2 39B8  
 LINE\_OUT\_R 38C2 39D8  
 LVL\_CNT0 23C4 44B4  
 LVL\_CNT1 23C4 43A5 44A4  
 L\_AD(3..0) 23D7 23A4 25C5  
 L\_FRAME\* 23D7 23A3  
 L\_SERI0 23A2 23D8  
 MCPX\_TCK0 24C5 25B5  
 MCPX\_TCK1 24C5 25B5  
 MCPX\_TDE0 24C5 25C5  
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 MCPX\_TDI0 24C5 25C5  
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 MCPX\_TMS0 24C5 25C5  
 MCPX\_TMS1 24C5 25C5  
 MCPX\_TRST0 24C5 25B5  
 MCPX\_TRST1 24C5 25B5  
 MCP\_3P3\_DELAY 23A7  
 MCP\_VDD\_PLL 23A5 23B4  
 MII\_MDC 23B8 35C7  
 MII\_MDIO 23B7 35C8  
 MII\_RXD(3..0) 35C8 23B7  
 MII\_TXD(3..0) 23B7 23D2 35C7  
 M\_AB\_CKE 14A4 15A4  
 M\_A\_ADDR(13..0) 11D4 14D7  
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 M\_A\_CLK 11C4 14A4  
 M\_A\_CLK\* 11C2 14A4  
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 M\_A\_WE\* 11C4 14B2 14B6  
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 M\_D\_WE\* 12A7 17B2 17B7  
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 M\_VREF\_1 16A3 16B8 17A2 17A7  
 NB\_CK\_13PSM 29D1 11B5  
 NB\_CK\_13PSM\_R 29D5  
 NV2A\_3P3\_DELAY 12A2  
 NV2A\_INTA\* 12B2 24C4  
 NV2A\_TEST 12B2  
 NV2A\_VREF\_0 11C2  
 NV2A\_VREF\_1 12C6  
 OUTPUT\_CLAMP\_L 39A3 39A1  
 OUTPUT\_CLAMP\_R 39A4 39D1  
 P8AC 35C3 36B8  
 P8AC\_R 36B7  
 P1CL 35C3 36A8  
 P2LI 35C3 36A8  
 P2LI\_R 36A7  
 P3TD 35C3 36A8  
 P4RD 35C3 36A8  
 PCI\_CLK 24C5 23A3  
 PCI\_CLK\_FB 24C6  
 PCI\_FRAME 24A1 25D5  
 PCI\_PULLUP 23A3 24A1  
 PCI\_RESET\* 25A5 12B2 14A7 16A7 23A4 35B6 37B5  
 43B6 47D3  
 PCI\_RESET\_B\* 24C4 25A8  
 PICD0 6B7  
 PICD1 6B8  
 PLLVDD 12A2  
 PLL\_DELAY\* 49C2 12A4 23A8 34D3  
 PLL\_ENABLE 49C5  
 POWER\_S4 49B1 49C7  
 POWER\_S4\_R 49B3  
 POWOK 32C4 29C4 29D7 49C7  
 POWON 49C7 32C6 44D4  
 RED\_LED 49C4 49B5  
 RGB\_B 44C7  
 RGB\_C 44B7  
 RGB\_SELECT 44C6  
 RGB\_SELECT\* 23C4 44C8  
 ROM\_A(19..0) 24D8 46A6  
 ROM\_CE\* 46C4  
 ROM\_D(7..0) 24C8 46A6  
 ROM\_OE\* 24C7 46D7  
 ROM\_OE\_R\* 46D6  
 ROM\_WE\* 24C8 46C7  
 ROM\_WE\_R\* 46C7

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C								
B								
A								
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RTC_X1 23B5
RTC_X0 23B5
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SB_CK_13P5M_LR 29D6
SMB_SCL 23B3 36D3 49C7 23A4 36B3 36C2 41B6
42C7
SMB_SDA 23A2 23B3 36B2 36B3 36D1 41B6 42C7
49C7
SMCRESET 4BA3 49D7
SMC_CK_10M 29D2 49D7
SMC_CK_10M_LR 29D5
SM1* 49C7 23C4
SPDIF 23B3 44D8
SPDIF_R 44D6
SPKR_STRAP 23B5
STATUS 44A1 44C6
SYSRESET* 49C4 6B2 24D5
SYSRESET_R* 6B2 6C7
TP16_EN 26B8 26C7
TP_1032_4 36B3
TP_1032_6 36B2
TP_3709_5 36C4
TP_BGA2_24 5C4
TP_BGA2_A5 5C4
TP_BGA2_AA1 6C3
TP_BGA2_AA17 7C7
TP_BGA2_AA21 5B4
TP_BGA2_AB1 6C3
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TP_BGA2_C5 5C4
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TP_BGA2_H4 7C7
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TP_BGA2_W21 5B4
TP_BGA2_Y1 6B3
TP_BGA2_Y2 6C3
TP_BGA2_Y21 5B4
TP_BUF24H 24A3
TP_CPURSV0 11B6
TP_CPURSV1 11B6
TP_DEBUG_GP1015 23C4
TP_DVO_1 42B6
TP_DVO_20 42B5
TP_DVO_29 42B5
TP_DVO_30 42B5
TP_DVO_47 42B6
TP_INIT* 24D5
TP_MCPX_AA19 24D7
TP_MCPX_AB17 24D7
TP_MCPX_H21 23C4
TP_MCPX_TD00 24C5
TP_MCPX_TD01 24C5

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TP_MCPX_Y2 23B5
TP_MCPX_Y19 24D7
TP_MCPX_Y20 24D7
TP_PIC_10 49D5
TP_PRIIDE_32 37A2
TP_PRIIDE_34 37A2
TP_PRIIDE_39 37A3
TP_REF6 26B8
TP_ROM_CE* 24C7
TP_SA_GPI02 41B6
TRAY_STATE0 49C3 49C4
TRAY_STATE1 49C1 49C4
TRAY_STATE2 49C3 49C4
USBPWR_1 47D4
USBPWR_2 47C4
USBPWR_3 47C4
USBPWR_4 47B5
USB_1 23D7 47D1 47C7
USB_1* 23D7 47D1 47B7
USB_1FB 47D3
USB_1FB* 47D3
USB_1R 47D2
USB_1R* 47D2
USB_2 23D7 47C1 47A7
USB_2* 23D7 47C1 47A7
USB_2FB 47C3
USB_2FB* 47C3
USB_2R 47C2
USB_2R* 47C2
USB_3 23D7 47B1 47A6
USB_3* 23D7 47B1 47A6
USB_3FB 47B3
USB_3FB* 47B3
USB_3R 47B2
USB_3R* 47B2
USB_4 23D7 47A1 47A6
USB_4* 23C7 47A1 47A3
USB_4FB 47A3
USB_4FB* 47A3
USB_4R 47A2
USB_4R* 47A2
USB_5 23C7 25A1
USB_5* 23C7 25B1
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VID_CK_13PSM 29D2 41A6 42B7
VID_CK_13PSM_LR 29A6 29D5
VMODE0 44C1 49C4
VMODE0_R 44C2
VMODE1 44C1 49C4
VMODE1_R 44C2
VMODE2 44C1 49C4
VMODE2_R 44C2
VREG_1PS_GATE 26B8 31D8
VREG_2PS_GATE 26B8 31B8
VREG_CSN 26B5
VREG_CSP 26C5
VREG_CSP_R 26B3
VREG_FETDRVA 26C5
VREG_FETDRVA_FETDRVB_PN1 26C3
VREG_FETDRVB 26C5
VREG_PUCC 26D7
VREG_PARGOOD 26B6
VREG_UCC 26D8
VREG_UCCP_R 26C2
VREG_VO_SENSE 26A4
V_IPS 26C1 12B2 22D8 24A7 24C1 29B2 34D3
V_IPS_FEEDBACK 26A4
V_IPS_VTT 31C2 5C2 6D7 7B6 7D1 7D4 7D8 9D7
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21D2 21D6 21D7 22D5 26A6 28B6 28C6
30B7 38C6
U_3P3_FB 29A1 29A6 29C7
U_3P3_STBY 32D8 29A6 34D7 38A6 44D4 48B5 48D7
49B1 49C5 49D7
U_SPO_FILTERED 26D3 28D7 32A4 32B4
U_BAT_RTC 34C1 23B4
U_BAT_RTC_FET 34D3
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U_CPUCORE 26C1 7C4 8D3 8D7 27C6 41A3
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Fri May 03 11:24:09 2002

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	XXXXXX	52	12.0

	8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
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XCAP	21C7	C4N7 CAPN	43D4	C1G6 CAP-P	47D5	C2P21 CAPN	8B6	C4A1 CAPN	43A7	C4N8 CAPN	31D6	C1G7 CAPN	47C5	C2P22 CAPN	8B5	C4A2 CAPN	44C5	C4N9 CAPN	31D7	C1P1 CAPN	8B5	C2P23 CAPN	8B5	C4A3 CAPN	41C4	C4P1 XCAP	20A3	C1P2 CAPN	27B4	C2P24 CAPN	9A5	C4A4 CAPN	43D6	C4P2 CAPN	12B1	C1P3 CAPN	8D2	C2R1 CAPN	11C4	C4A5 CAPN	43C5	C4P3 CAPN	22D3	C1P4 CAPN	27B4	C2R2 CAPN	9C6	C4A6 CAPN	43C5	C4P4 CAPN	22A4	C1P5 CAPN	8B2	C2R3 CAPN	9B6	C4A7 CAPN	43C5	C4P5 CAPN	22B4	C1P6 CAPN	7A4	C2R4 CAPN	9B6	C4A8 CAPN	41A1	C4P6 CAPN	22B4	C1P7 CAPN	9B6	C2R5 CAPN	9C6	C4B1 CAPN	41A1	C4P7 CAPN	22A4	C1P8 CAPN	9B6	C2R6 CAP-P	7D5	C4B2 CAPN	41A2	C4P8 CAPN	22A4	C1P9 CAPN	8C2	C2R7 CAPN	26A7	C4B3 CAPN	43D4	C4P9 CAPN	22C3	C1P10 CAPN	9A6	C2T1 CAPN	26D7	C4B4 CAPN	31D7	C4P10 CAPN	22B4	C1P11 CAPN	9C6	C2T2 CAPN	33A4	C4B5 CAPN	31D8	C4P11 CAPN	33B6	C1P12 CAPN	7A5	C2U1 CAPN	26C2	C4B6 CAPN	12A1	C4P12 XCAP	22C5	C1R1 CAPN	9A6	C2U2 CAPN	49B1	C4E1 XCAP	21D7	C4P13 XCAP	22B5	C1R2 CAPN	8C2	C2V1 CAPN	32B1	C4E2 XCAP	20D2	C4P14 XCAP	22C3	C1R3 CAPN	8C2	C3A1 CAPN	33D5	C4E3 XCAP	21B4	C4P15 XCAP	22C5	C1R4 CAPN	27B5	C3B1 CAPN	11C5	C4E4 XCAP	20A3	C4P16 CAPN	22C3	C1R5 CAPN	27B5	C3B2 CAPPDFPN	31C6	C4E5 XCAP	20C2	C4P17 CAPN	11A6	C1R6 CAPN	8B2	C3B3 CAPN	31C5	C4E6 XCAP	21B5	C4P18 CAPN	22A7	C1R7 CAPN	8A5	C3B4 CAPN	31C4	C4E7 XCAP	20B3	C4P19 CAP-P	22C7	C1R8 CAPN	7A5	C3B5 CAPN	31C4	C4E8 XCAP	21B5	C4P20 CAPN	22B7	C1R9 CAPN	7A7	C3B6 CAPN	31C4	C4F1 XCAP	21C4	C4P21 CAPN	22C7	C1T1 CAPN	33D6	C3B7 CAPN	22C1	C4F2 XCAP	20C2	C4P22 XCAP	12C1	C2D1 CAPN	26D8	C3D1 XCAP	5A8	C4F3 XCAP	21A3	C4P23 CAPN	12C1	C2D2 CAPN	26B4	C3D2 XCAP	5A8	C4F4 XCAP	21B4	C4R1 CAPN	22A6	C2D3 CAPN	26A7	C3E1 CAPN	20B5	C4F5 XCAP	21A4	C4R2 CAPN	22B7	C2E1 CAPN	26D7	C3E2 CAP-P	27C4	C4F6 CAPN	16A3	C4R3 XCAP	22B5	C2E2 CAPN	26A4	C3E3 XCAP	20A5	C4F7 XCAP	20C2	C4R4 CAPN	22C7	C2E3 CAP-P	27C5	C3E4 CAPN	20B3	C4F8 XCAP	21C3	C4R5 CAPN	22B7	C2E4 CAP-P	27C3	C3E5 XCAP	21D3	C4F9 CAP-P	30B3	C4R6 CAPN	22C7	C2E5 CAP-P	27C3	C3E6 XCAP	21B3	C4G1 CAPPDFPN	30C5	C4R7 XCAP	22C5	C2E6 CAPN	32C5	C3E7 XCAP	21C5	C4G2 CAPN	30B4	C4R8 CAPN	11A4	C2E7 CAPN	32C6	C3E8 XCAP	20A5	C4G3 CAPN	30B5	C4R9 XCAP	22C5	C2F1 CAP-P	26D5	C3E9 XCAP	21D2	C4G4 CAP-P	47B6	C4R10 XCAP	22A5	C2G1 CAPN	32B1	C3F1 XCAP	20A5	C4G5 CAPN	47B5	C4R11 XCAP	22B5	C2G2 CAPPDFPN	32A1	C3F2 XCAP	21D2	C4G6 CAPN	47B4	C4R12 CAPN	22D6	C2G3 CAPN	47C5	C3F3 CAPN	32B2	C4G7 CAPN	47B3	C4R13 CAPN	22C6	C2G4 CAPN	47C3	C3F4 CAPN	32B2	C4G8 CAP-P	47B5	C4R14 CAPN	22C4	C2G5 CAPN	47C3	C3F5 XCAP	20A5	C4G9 CAPN	47B3	C4R15 CAPN	22D4	C2G6 CAPN	26D6	C3F6 CAPPDFPN	32A2	C4G10 CAPN	47A3	C4R16 CAPN	22B6	C2G7 CAPN	47D3	C3F7 XCAP	21A3	C4G11 CAPN	47B4	C4R17 CAPN	22B6	C2G8 CAPN	47D3	C3F8 CAPN	32B2	C4G12 CAPN	47B5	C4R18 CAPN	22C4	C2G9 CAPN	47D7	C3F9 CAPN	32B2	C4G13 CAPN	47A3	C4R19 CAPN	22C4	C2G10 CAPN	47C4	C3F10 CAPPDFPN	31B6	C4G14 CAPN	30B5	C4R20 XCAP	12D4	C2N1 CAP-P	31C3	C3F11 CAPN	32A2	C4M1 CAPN	44C5	C4R21 XCAP	20B3	C2N2 CAP-P	31C3	C3G1 CAPPDFPN	32A2	C4M2 XCAP	43C1	C4T1 XCAP	21C7	C2P1 CAPN	7A5	C3G2 CAPN	26D6	C4M3 XCAP	43C1	C4T2 XCAP	20B4	C2P2 CAPN	9B5	C3G3 CAPN	47B7	C4M4 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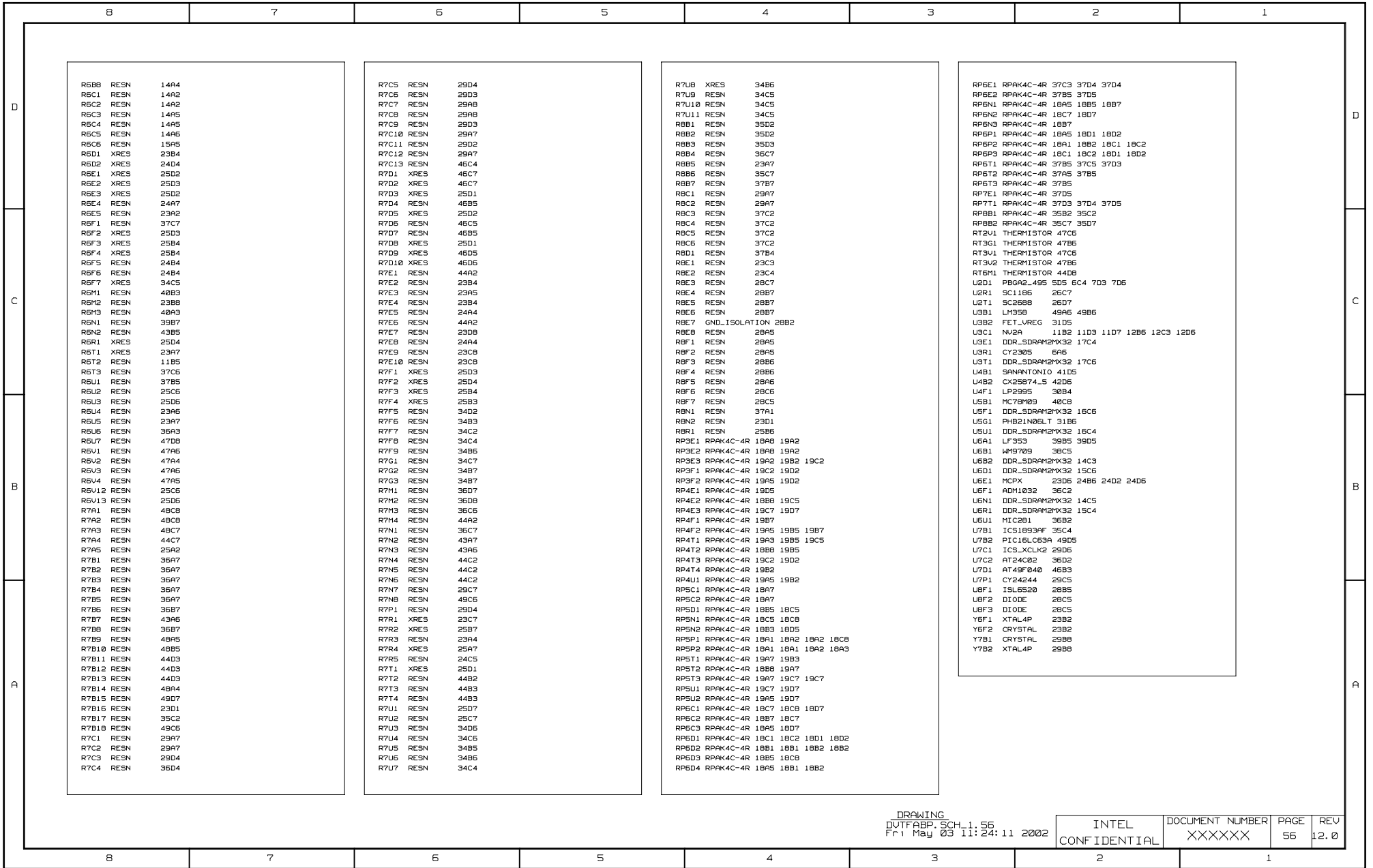
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INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 54	REV 12.0
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Fri May 03 11:24:10 2002

INTEL CONFIDENTIAL	DOCUMENT NUMBER XXXXXX	PAGE 55	REV 12.0
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RP3F1 RPAK4C-4R 19C2 19D2  
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RP4E1 RPAK4C-4R 19D5  
RP4E2 RPAK4C-4R 18B8 19C5  
RP4E3 RPAK4C-4R 19C7 19D7  
RP4F1 RPAK4C-4R 18B7  
RP4F2 RPAK4C-4R 19A5 19B5 19B7  
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RP4T2 RPAK4C-4R 18B8 19B5  
RP4T3 RPAK4C-4R 19C2 19D2  
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RPSN2 RPAK4C-4R 18B3 18D5  
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RPSU2 RPAK4C-4R 19A5 19D7  
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RP6D2 RPAK4C-4R 18B1 18B1 18B2 18B2  
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RP8B2 RPAK4C-4R 35C7 35D7  
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RT3G1 THERMISTOR 47B6  
RT3V1 THERMISTOR 47C6  
RT3V2 THERMISTOR 47B6  
RT6M1 THERMISTOR 44D8  
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U2T1 SC268B 26D7  
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U4F1 LP2995 30B4  
U5B1 MC78M09 40C8  
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U6B1 M9709 38C5  
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U6D1 DDR\_SDRAM2Mx32 15C6  
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U6F1 ADM1032 36C2  
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U7D1 AT49F040 46B3  
U7P1 CY24244 29C5  
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U8F3 DIODE 28C5  
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Y6F2 CRYSTAL 23B2  
Y7B1 CRYSTAL 29B8  
Y7B2 XTAL4P 29B8