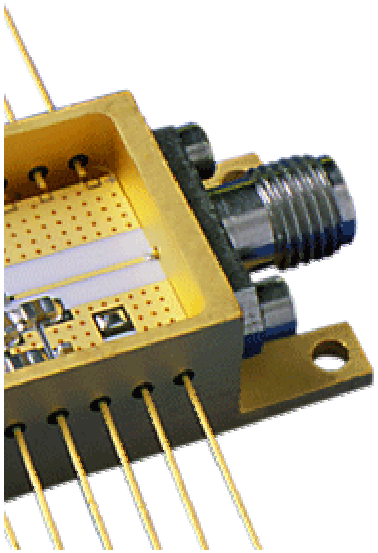
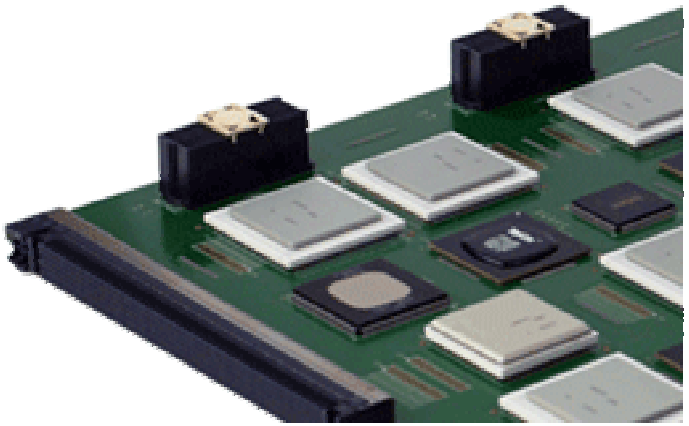
FLEXTRONICS

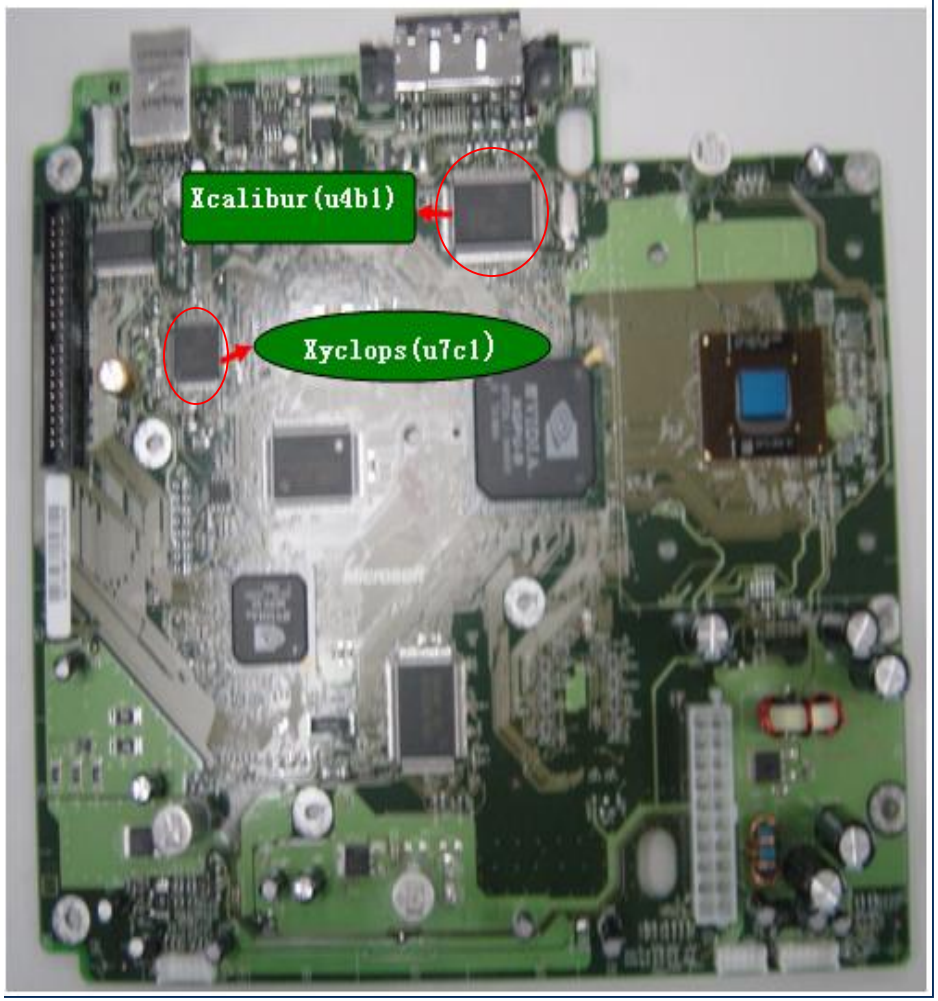
Debug Guideline for the XBox



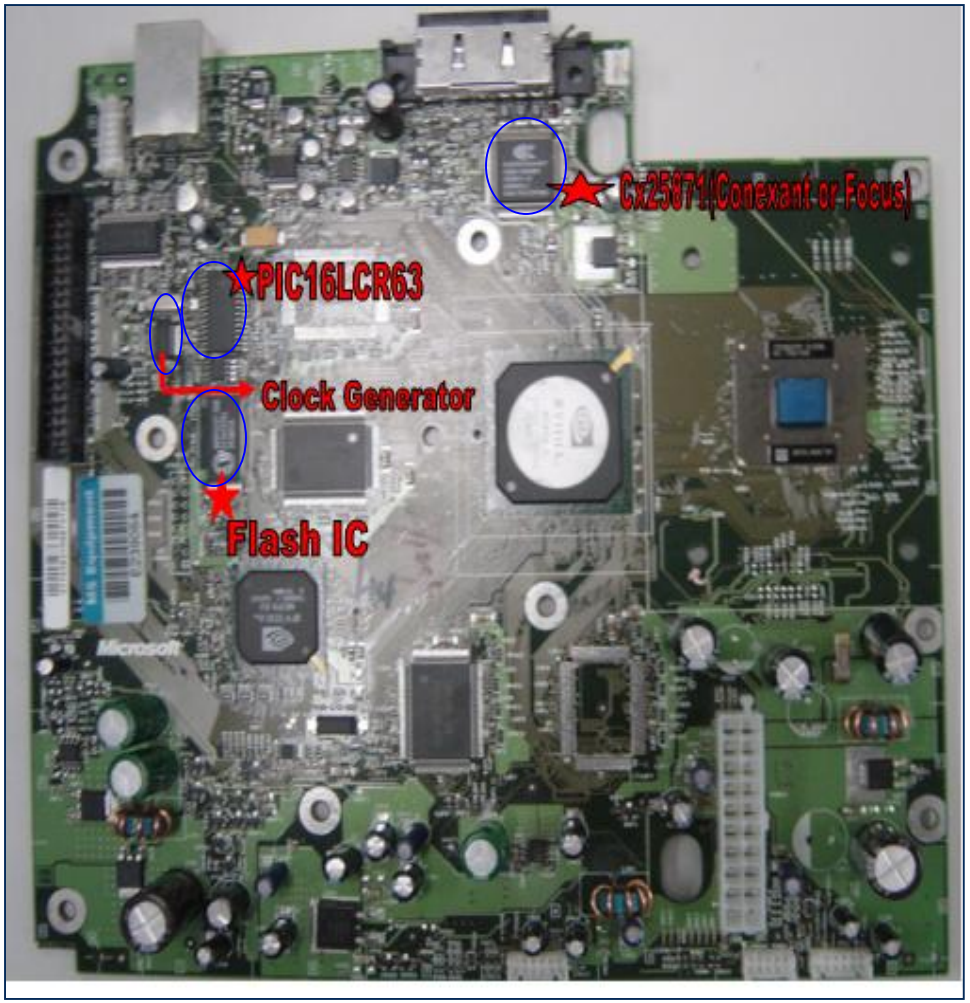


PCBA compare by Tuscany and Xblade

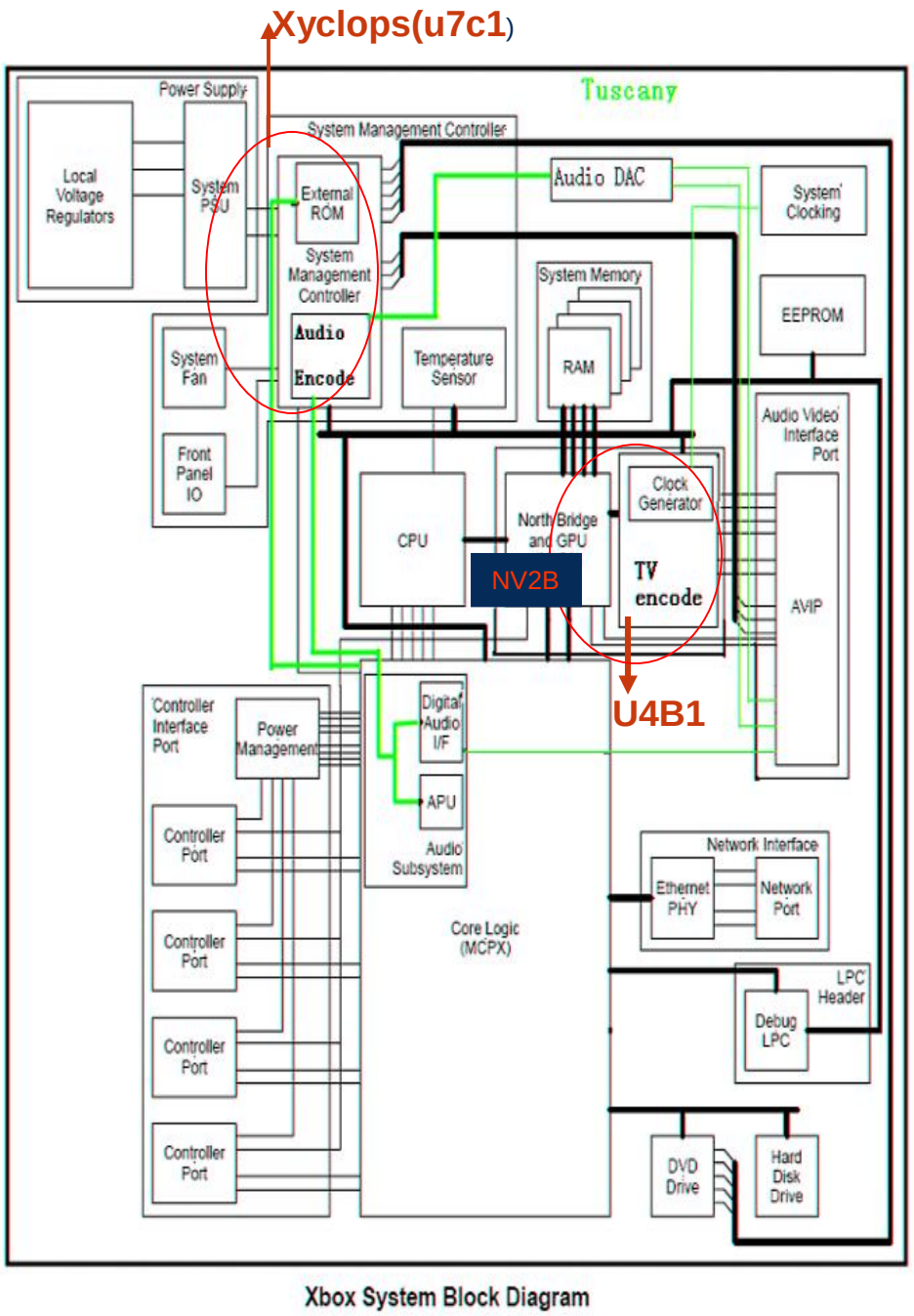
Tuscany



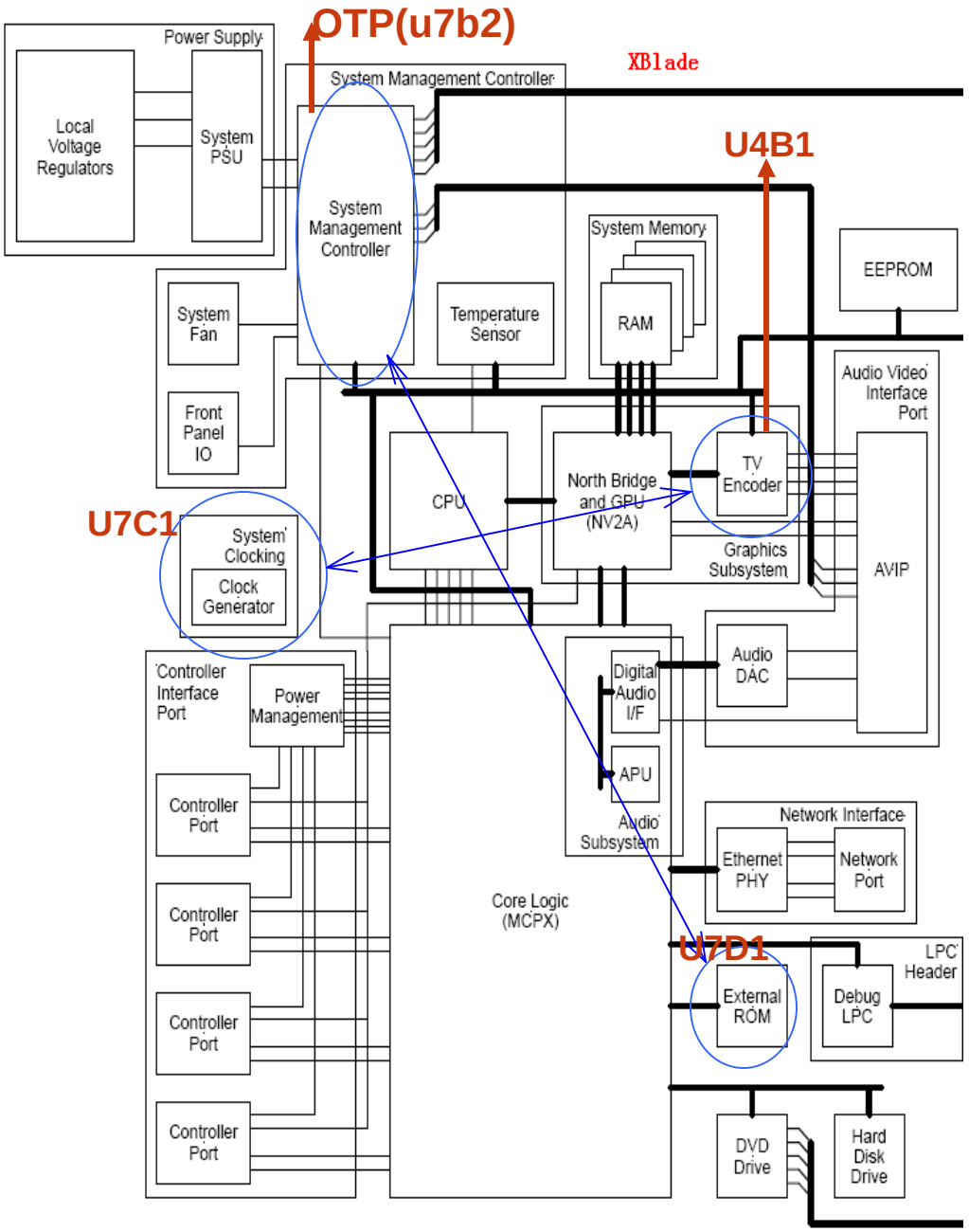
Xblade



Xbox system block diagram compare for Tuscany and Xblade



Xbox System Block Diagram



Xbox System Block Diagram

SMC

uscany SMC (System Management Controller):

This microcontroller (Xyclops) performs several important system control duties.

The SMC is always powered by the stanby voltage output of the power supply.

The SMC communicates with the system CPU via a System Management Bus (SMBus) port on the south bridge.

The duties of the SMC include the following:

- System RESET
- Temperature monitoring and fan control
- Front Panel IO monitoring (POWER, RESET and INDICATORS)
- AVIP Mode monitoring
- DVD control
- AUDIO Encode

If there are problems related with this chips , you need to check

- CLKIN(24MHZ) for crystal operation at U7C1# 25
- 3VSB Power 3.3v U7C1#31
- SMCRESET U7C1#58 high level.

IN (POWSW) U7C1#1 Power Switch input (0=sw pressed , 1= not pressed)

XBlade or QT SMC (System Management Controller)-------- OTP:

- This microcontroller (PIC16LCR63) performs several important system control duties.
- The SMC is always powered by the stanby voltage output of the power supply.
- The SMC communicates with the system CPU via System Management Bus (SMBus) port on the south bridge.
- The duties of the SMC include the following:

1. System RESET
2. Temperature monitoring and fan control
3. Front Panel IO monitoring (POWER, RESET and INDICATORS)
4. AVIP Mode monitoring
5. DVD control

- If there are problems related with this chips , you need to check

1. CLKIN for crystal operation at 10MHz U7B2#9
2. 3VSB Power 3.3v U7B2#20
3. SMCRESET U7B2.4.1 high level.

- IN (POWSW) U7B2#18 Power Switch input (0=sw pressed , 1= not pressed)

SMC

(Xycolps)-------Tuscany

- OUT (POWON) U7C1#28 , Controls power supply (0=power off, 1=power on)
- The PWRGD (Power Good) is driven from the power supply to signal that the VDD3 rail is stable, PWRGD will be driven by the SMC to force the system to RESET. This is the main source of reset for much of the internal logic.PCIRST# and CPURST# are generated from this signal.
- *INIT# is asserted for 16 PCI clocks to reset the processor.*
- CPUTST # is used to reset the CPU and it's cache
- PCIRST # is used to reset the most of the system's peripheral logic.
- See schematics page 39

FRONT PANEL:

Power Switch:

- The power switch is a momentary type push switch , monitored by the System Management Controller (SMC) , which in turn monitors the system power up and power down cycle. The console itself is either "on" or "off" , although the SMC is always on as long as mains power is applied.

Check

- IN POWSW U7C1#6 Power Switch input (0=sw pressed , 1= not pressed)
- OUT POWON U7C1#28 , Controls power supply (0=power off, 1=power on)
- See the schematics page 39

OTP--------Xblade

•OUT (POWON) U7B2.16 , Controls power supply (0=power off, 1=power on)

•The PWRGD (Power Good) is driven from the power supply to signal that the VDD3 rail is stable, PWRGD will be driven by the SMC to force the system to RESET. This is the main source of reset for much of the internal logic.PCIRST# and CPURST# are generated from this signal.

•*INIT# is asserted for 16 PCI clocks to reset the processor.*

•CPUTST # is used to reset the CPU and it's cache

•PCIRST # is used to reset the most of the system's peripheral logic.

•See schematics page 49

FRONT PANEL:

Power Switch:

•*The power switch is a momentary type push switch , monitored by the System Management Controller (SMC) , which in turn monitors the system power up and power down cycle. The console itself is either "on" or "off" , although the SMC is always on as long as mains power is applied.*

Check

•IN POWSW U7B2#18 Power Switch input (0=sw pressed , 1= not pressed)

•OUT POWON U7B2#16 , Controls power supply (0=power off, 1=power on)

•See the schematics page 49

SMC-Disk Eject

Tuscany

Disk Eject:

- The disk eject button is also monitored by the SMC and it is responsible for monitoring the DVD TRAYSTARE lines.
- The SMC must monitor whenever new media (CD/DVD) is placed in the drive. Any time the SMC detected that the DVD tray has been opened and then closed, it will notify the CPU.

Check

- IN Eject Switch Input (0=switch pressed, 1=not pressed),Check EJTSW signal U7C1#7
- OUT DVDEject control to DVD (0=open tray, 1= close tray),check DVDEJECT signal U7C1#5
- see the schematics page 39

Xblade

Disk Eject:

- The disk eject button is also monitored by the SMC and it is responsible for monitoring the DVD TRAYSTARE lines.
- The SMC must monitor whenever new media (CD/DVD) is placed in the drive. Any time the SMC detected that the DVD tray has been opened and then closed, it will notify the CPU.

Check

- IN Eject Switch Input (0=switch pressed, 1=not pressed),check EJTSW signal U7B2#5
- OUT DVDEject control to DVD (0=open tray, 1= close tray),check DVDEJECT signal U7B2#7
- see the schematics page 49

SMC-LED

Tuscany

TIndicator Lights

- The SMC (Xyclops) is responsible for driving the front panel indicator LED, The CPU may override the state of the indicator by issuing commands via SMBus, with the expection of the thermal overhead and power off states.
- The Eject switch is surrounded by a light pipe illuminated by a pair of red and green LEDs. The LEDS are controlled by the SMC based on the SMC state machine and software settings requested by the CPU.
- Pressing either EJECT or POWER , the Xbox immediately begins to flash the LED's GREEN, The Xbox System Services will launch either the application on the DVD or the internal Xdash application, but once the application is running, the light will transition to the solid GREEN state.
- If the application is terminated by the user either by pressing the EJECT or POWER sw, the LED immediately goes to the blinking ORANGE state until the Xbox System Services completes any shutdown activity required.
- If the Xbox overheats , the LEDs go to blinking RED state until the system has dropped to a safe temperature.
- Also if and error is detected during the boot procedure, such as (RAM, chipset, or hardware) error , the LED indicates the error by blinking RED.

Check

LED1 Cathode (Red) active high U7C1#12, Q3V1, J2G1

LED2 Cathode (Green) active high U7C1#11, Q2V1, J2G1

see the schematics page 38

Xblade

TIndicator Lights

- The SMC is responsible for driving the front panel indicator LED, The CPU may override the state of the indicator by issuing commands via SMBus, with the expection of the thermal overhead and power off states.
- The Eject switch is surrounded by a light pipe illuminated by a pair of red and green LEDs. The LEDS are controlled by the SMC based on the SMC state machine and software settings requested by the CPU.
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- If the Xbox overheats , the LEDs go to blinking RED state until the system has dropped to a safe temperature.
- Also if and error is detected during the boot procedure, such as (RAM, chipset, or hardware) error , the LED indicates the error by blinking RED.

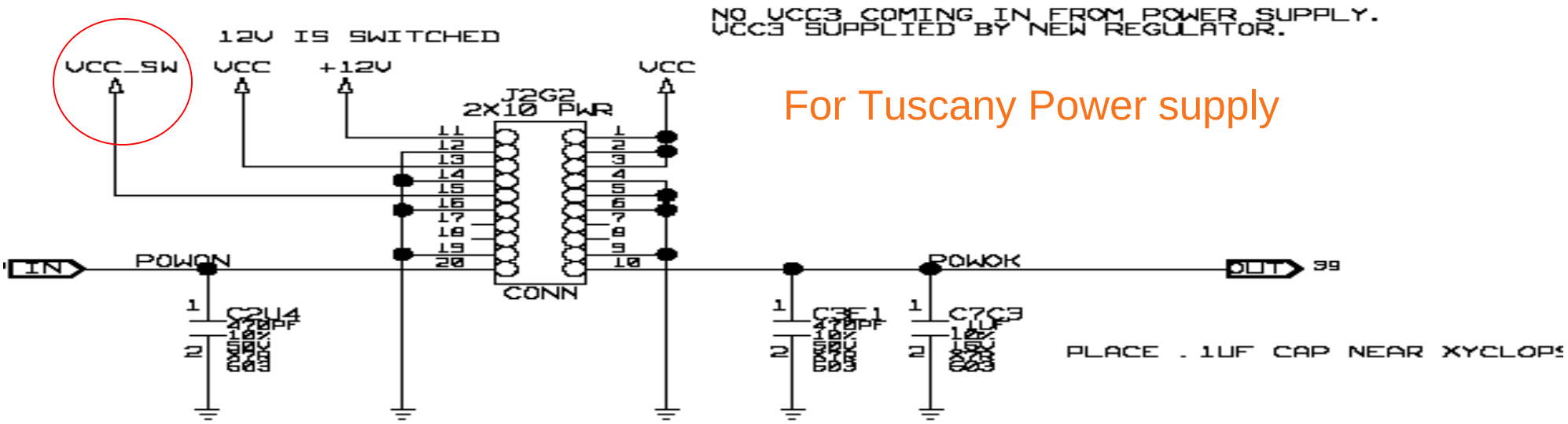
Check

LED1 Cathode (Red) active high U7B2#2, Q2V2, J2G2

LED2 Cathode (Green) active high U7B2#3, Q2V1, J2G2

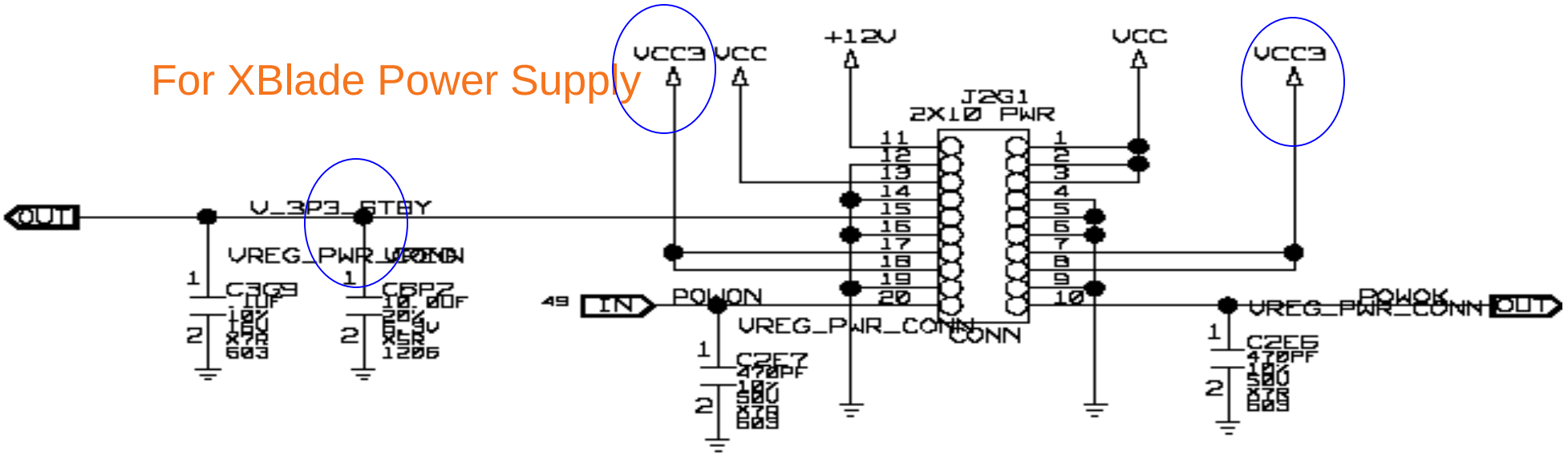
see the schematics page 49

Power supply

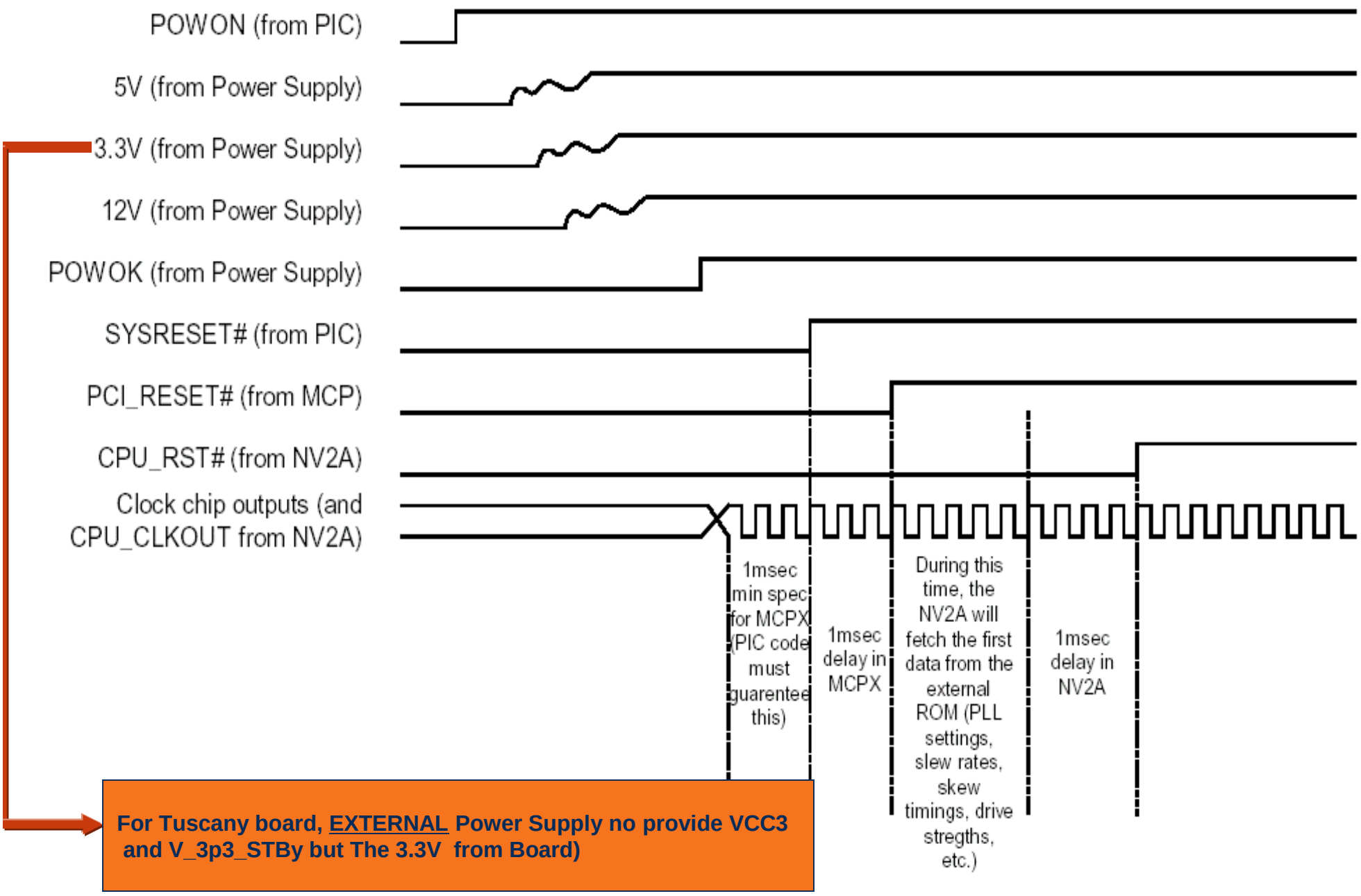


For Tuscany Power supply

For XBlade Power Supply



Power supply



Power supply

Tuscany

EXTERNAL POWER SUPPLY :

- The power supply apply the voltage to the Board until the SW (ON/OFF) is turned ON and the "POWON" signal is sending from the SMC to the Power Supply. After the Power Supply received this signal the voltages are applying (but if there is a very high flow of current requested by the Board the PS is going to disable the outputs indicate to the SMC via the "POWOK"

Check

- The SMC controller described below POWSW U7C1#6 Power Switch input (0=sw pressed , 1= not pressed)
- POWON U7C1#28 , Controls power supply (0=power off, 1=power on)

Xblade

EXTERNAL POWER SUPPLY :

- The power supply apply the voltage to the Board until the SW (ON/OFF) is turned ON and the "POWON" signal is sending from the SMC to the Power Supply. After the Power Supply received this signal the voltages are applying (but if there is a very high flow of current requested by the Board the PS is going to disable the outputs indicate to the SMC via the "POWOK"

Check

- The SMC controller described below POWSW U7B2#18 Power Switch input (0=sw pressed , 1= not pressed)
- POWON U7B2#16 , Controls power supply (0=power off, 1=power on)

REAL TIME CLOCK RTC

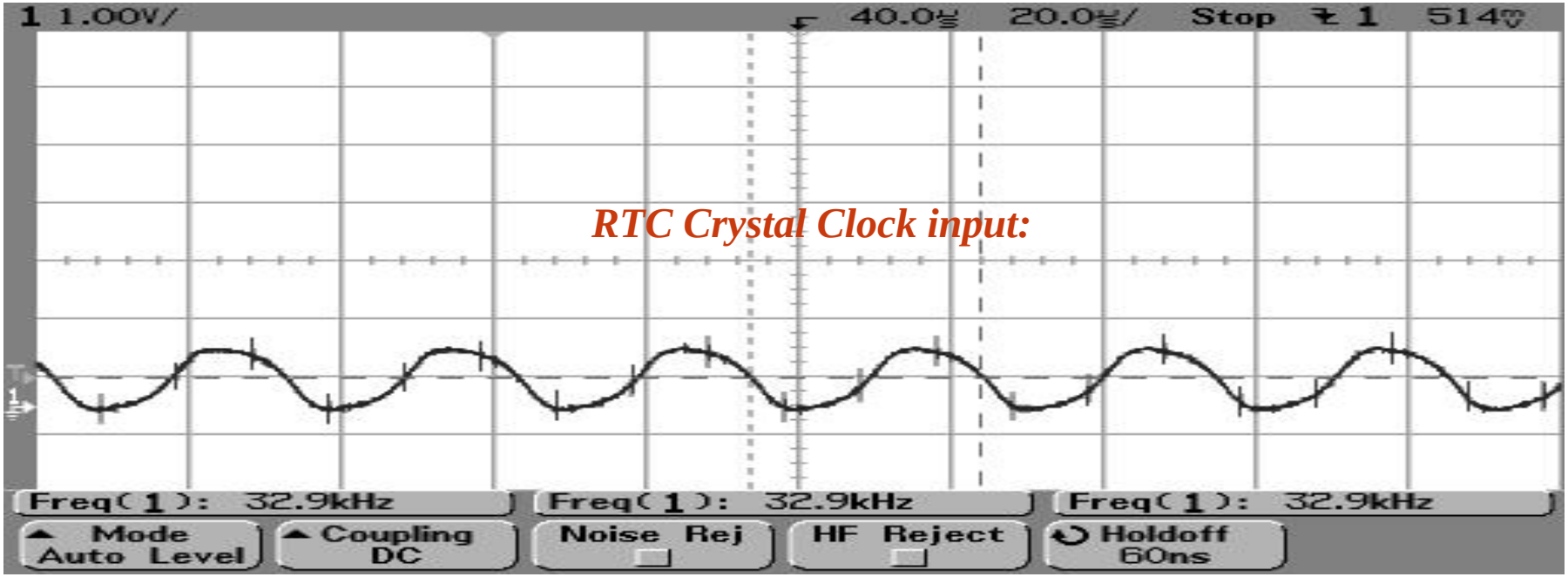
REAL TIME CLOCK RTC:

- The MCPX implements a real time clock that may be powered by an external lithium coin cell. The real time clock includes a 32.768 KHz oscillator, a clock and calendar timer, an alarm and 256 bytes for non volatile RAM.
- The test verifies the accessibility and operation of the RTC general purpose RAM, The size of the RAM is typically 128 or 256 bytes.
- DateTimeAccuracy Test =Verify that the difference between the RTC crystal and the reference timer and the capability of the RTC to keep and update the date/time.
- The test verifies the capability of the RTC to drive the IRQ8 interrupt signal and set the IRQF interrupt flag.

Check

- First be sure that there is not a contamination into the RTC section Y6F1 is stuff (32.768KHz) and working at the right frequency, voltage is lower that 1.3v the RTC clock is not going to function
- If the 32.768 KHz signal not appear , replace the Y6F1
- If this is correct and the Y6F1 is working replace the MCPX

REAL TIME CLOCK RTC

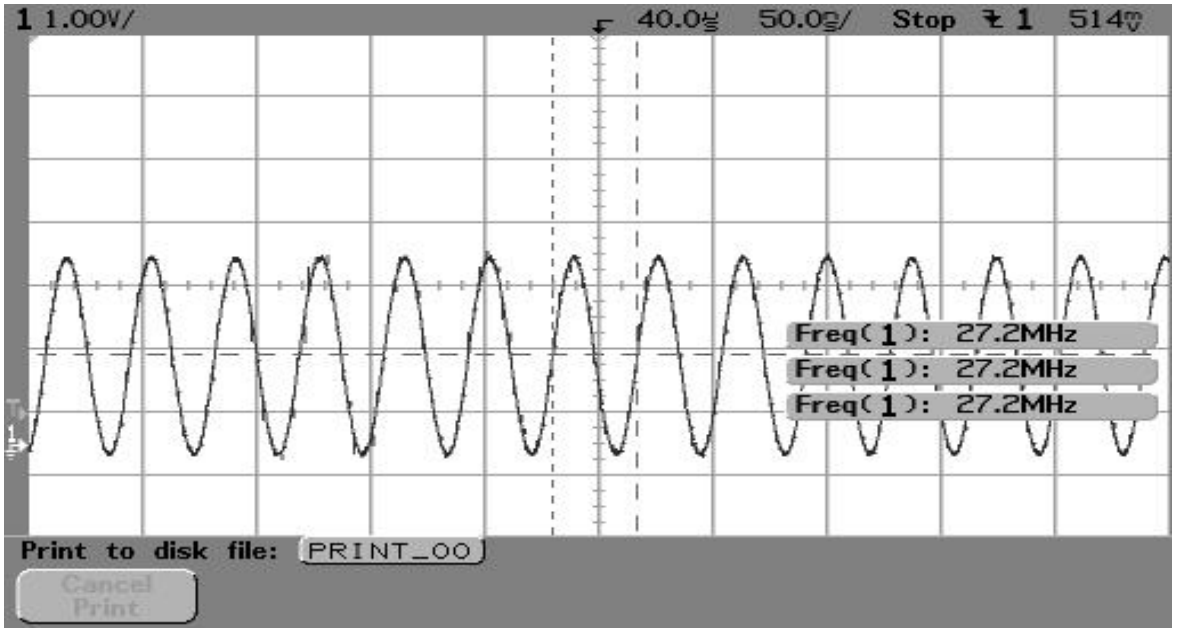


Description	Expected value	Signal name	Measurement point
Oscillator input	**32,768 kHz**	**RTC_X1 (X2)**	**Y6F1**
V_BAT_RTC	1.3V	V_BAT_RTC	Q7E1.3
PLL_DELAY*	12V	PLL_DELAY	Q6F1.1
RTC_DUMP	0.38mV	RTC_DUMP	Q7F1.1

SYSTEM CLOCK ‘s

- The clock synthesizer consists of a reference oscillator , driven by 27MHz crystal, two outputs , though a TV Encoder (xcalibur) for MCPX and NV2B.The PLL’s generate clocks for the Audio, Ethernet, and SMC.

- The synthesizer also includes an ENABLE pin which when shuts down all the outputs but leaves the SMC clock running



Description	Expected value	Signal name	Measurement point
Osc r input	27MHz	CLK_Xtal_x1(x2)	Y3B1
North Bridge NV2A	16.5 MHz	NB_CK_13P5M	DR7R1
South Bridge MCPX	13.5 MHz	SB_CK_13P5M	DB6T1
Audio DAC	24.576 MHz	AUD_CK_24M	C5N5.1
LAN	25 MHz	LAN_CK_25M	C7N5.1

SYSTEM CLOCK ‘s:

- For Xblade the system clock generator is take MCPX as input and uses multiple PLL(phase locked loops) as the synthesizing clock signals proved to the front side bus to CPU/DDR memory and LDT bus to the MCPX/GPU core clock.

Description	Expected value	Signal name	Measurement point
input:	13,5 MHz	NB_CK_13P5M	DB7R1
LDT	200 MHz		
(LDT, APU, USB, Legacy Block) Bus Interface and Ethernet Mac	100 MHz		
APU Core	133 MHz		
USB DPLL	48MHz		
Legacy Block	33 MHz		
ATA	66 MHz		

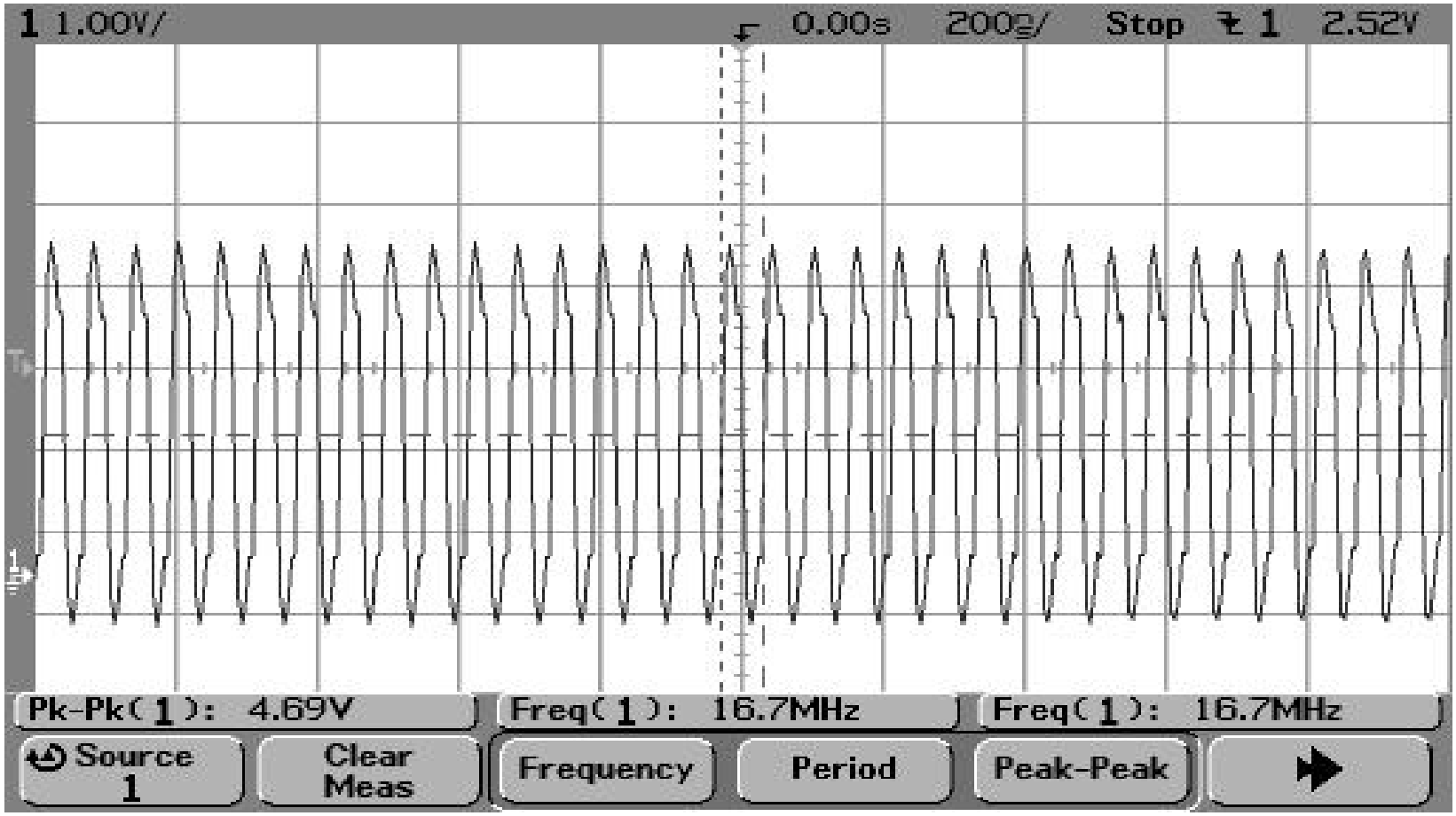
SYSTEM CLOCK ‘s

- **There is another clock generator module in the NV2B that it takes as input a stable clock reference and uses multiple PLL for the synthesizing the clock signals for Clock Generator outputs used for :**

Description	Expected value	Signal name	Measurement point
CPU Clock	133MHz	CK_H_133_CPU_BUF	U3R1#8
DDR memory clock	200MHz		

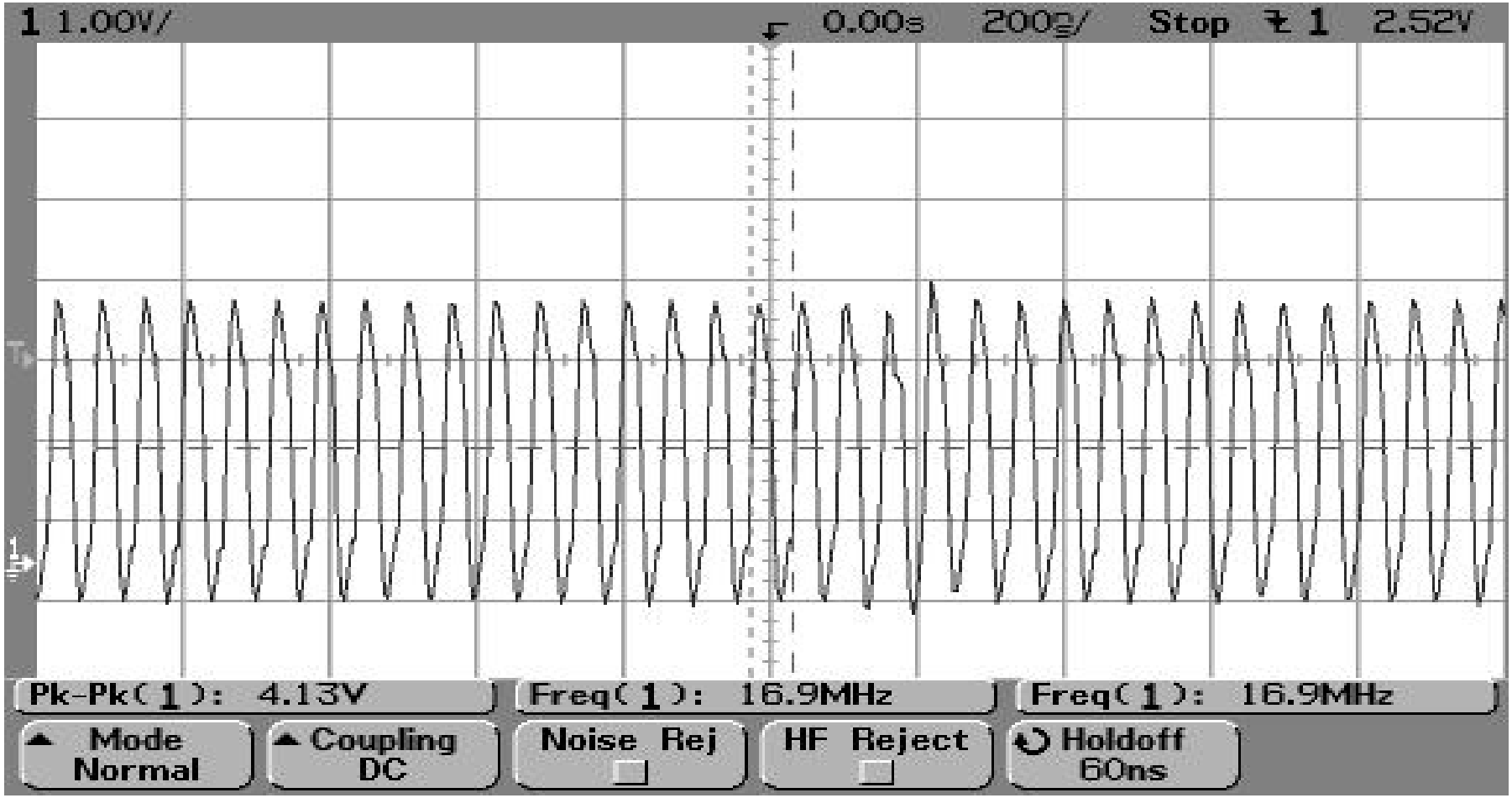
NB_CK_13P5M(DB7R1)

NB_CK_13P5M



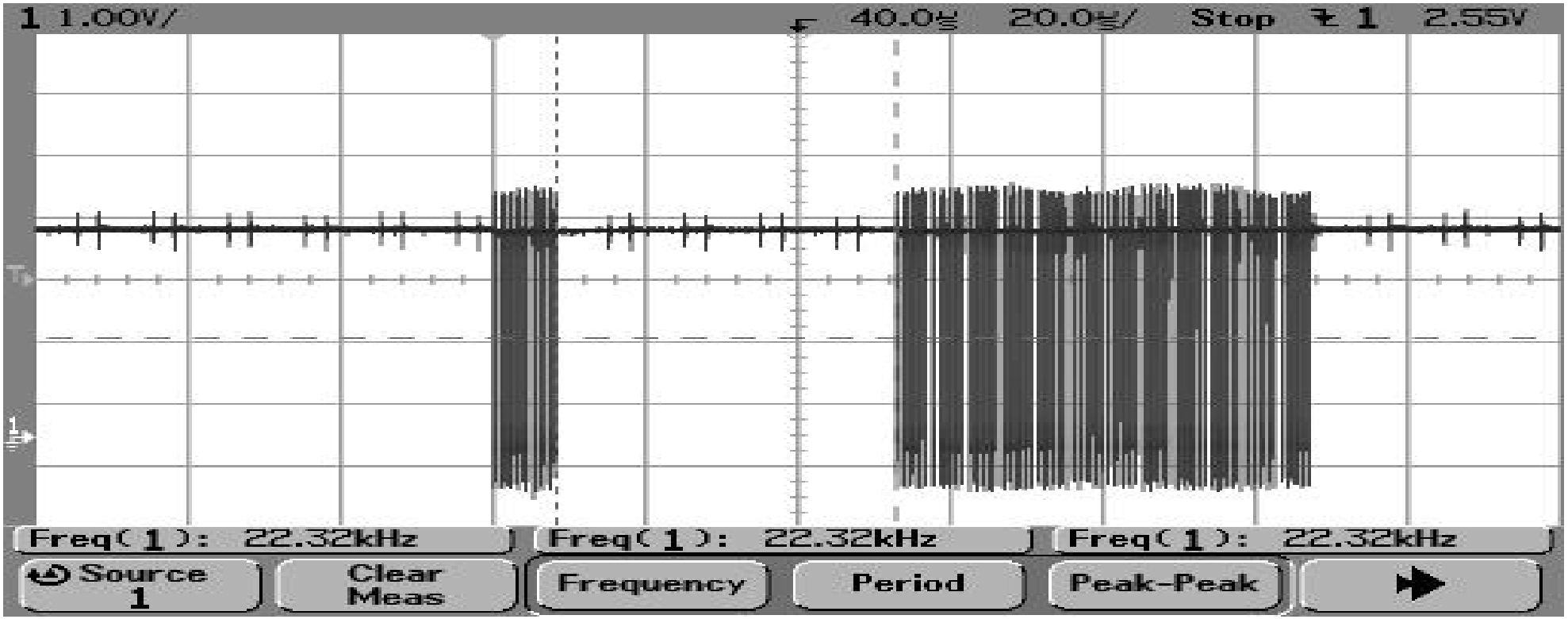
CH_H_PICCLK(R6T1.1)

Further clocks:
CH_H_PICCLK (from NV2B to CPU) – in this case 16.8MHz:



Detail MCPX and NV2B fetch (fetching location:R7D11.1)

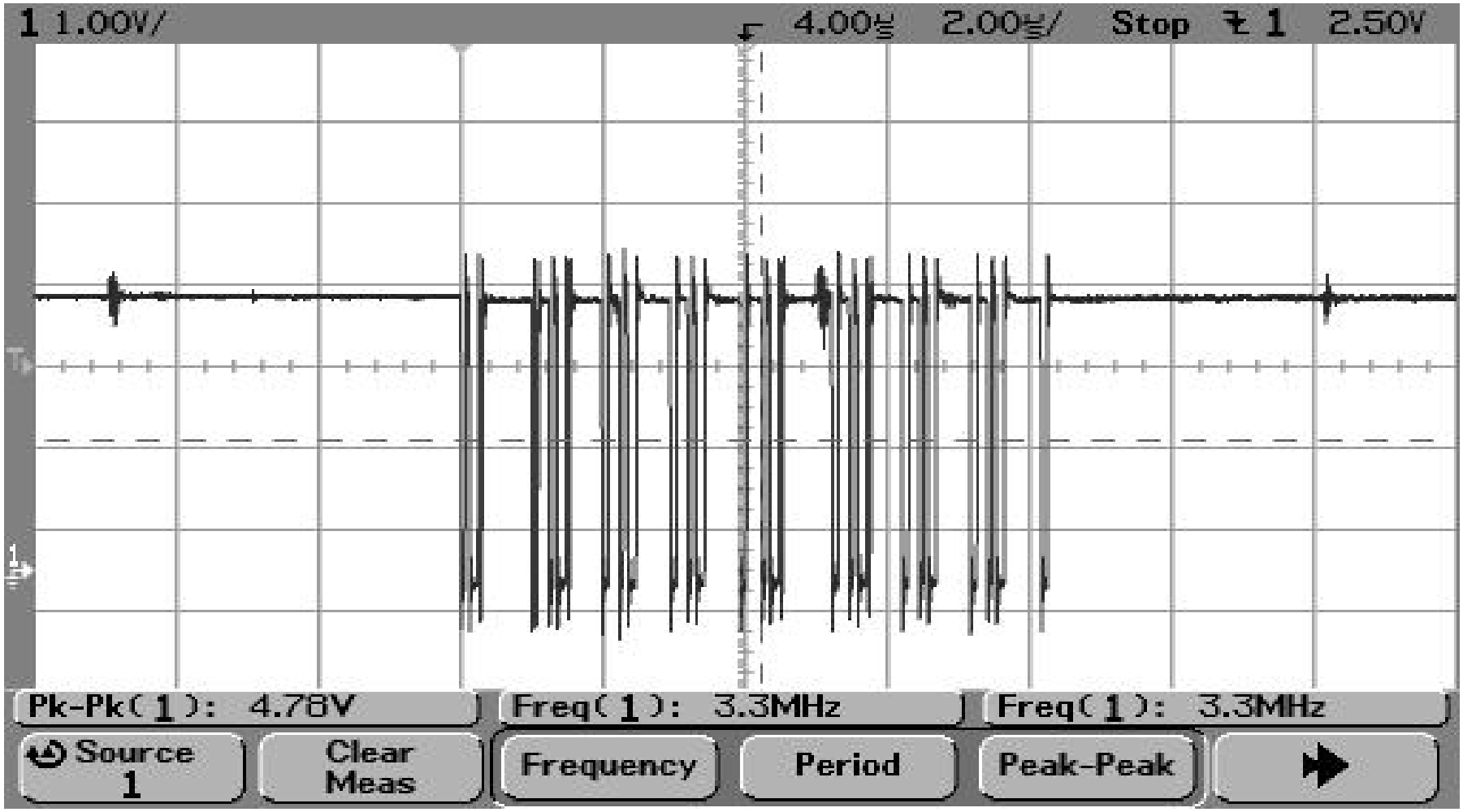
Detail MCPX and NV2B fetch (first part of complete fetching sequence



Remark: for Xblade or QT fetching location is Signals on ROM_CE* (R7D1) during booting phase (after power on).

Detail MCPX fetch

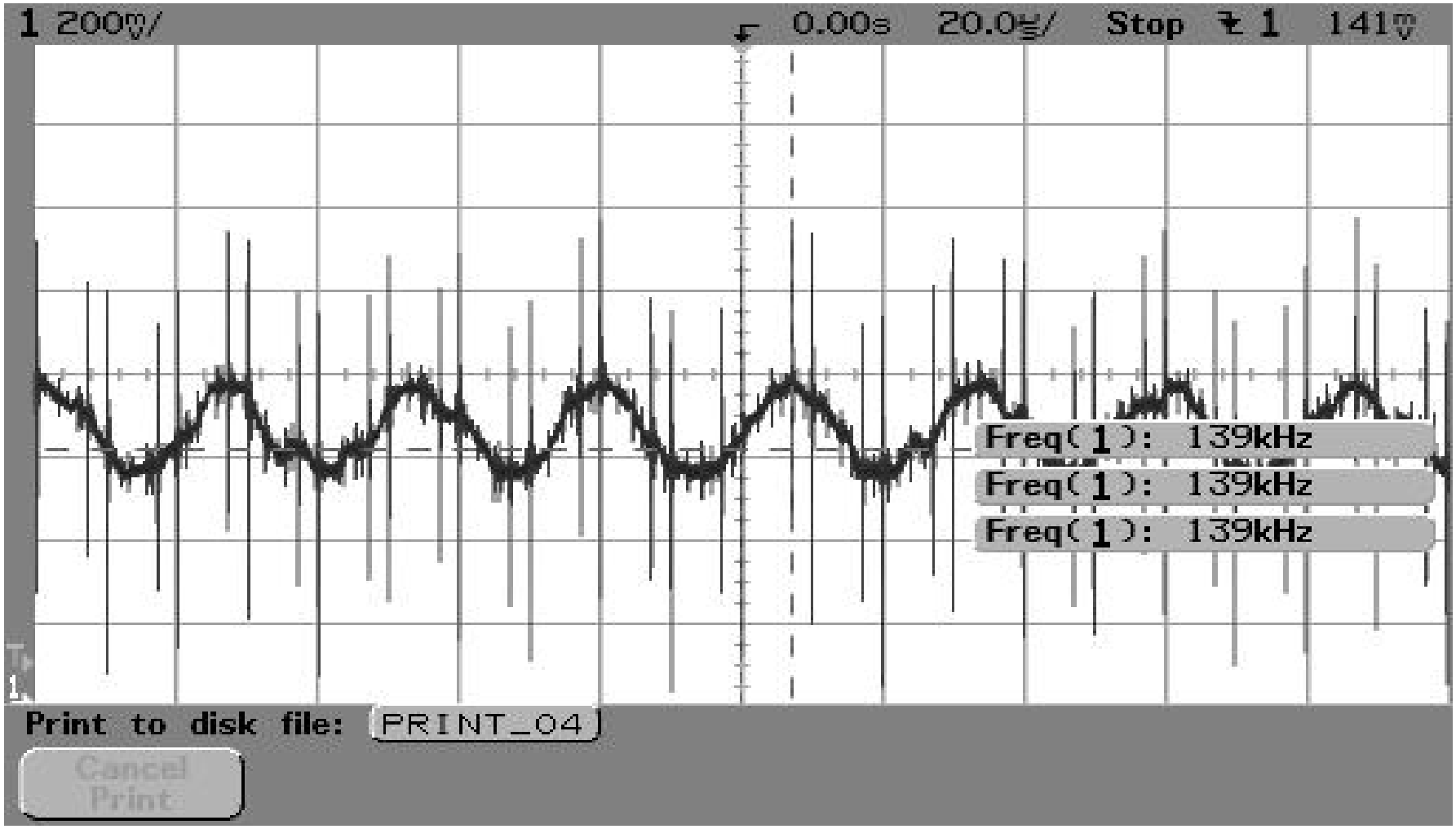
Detail MCPX fetch



Detail 1 of NV2B fetch (complete NV2B fetch)

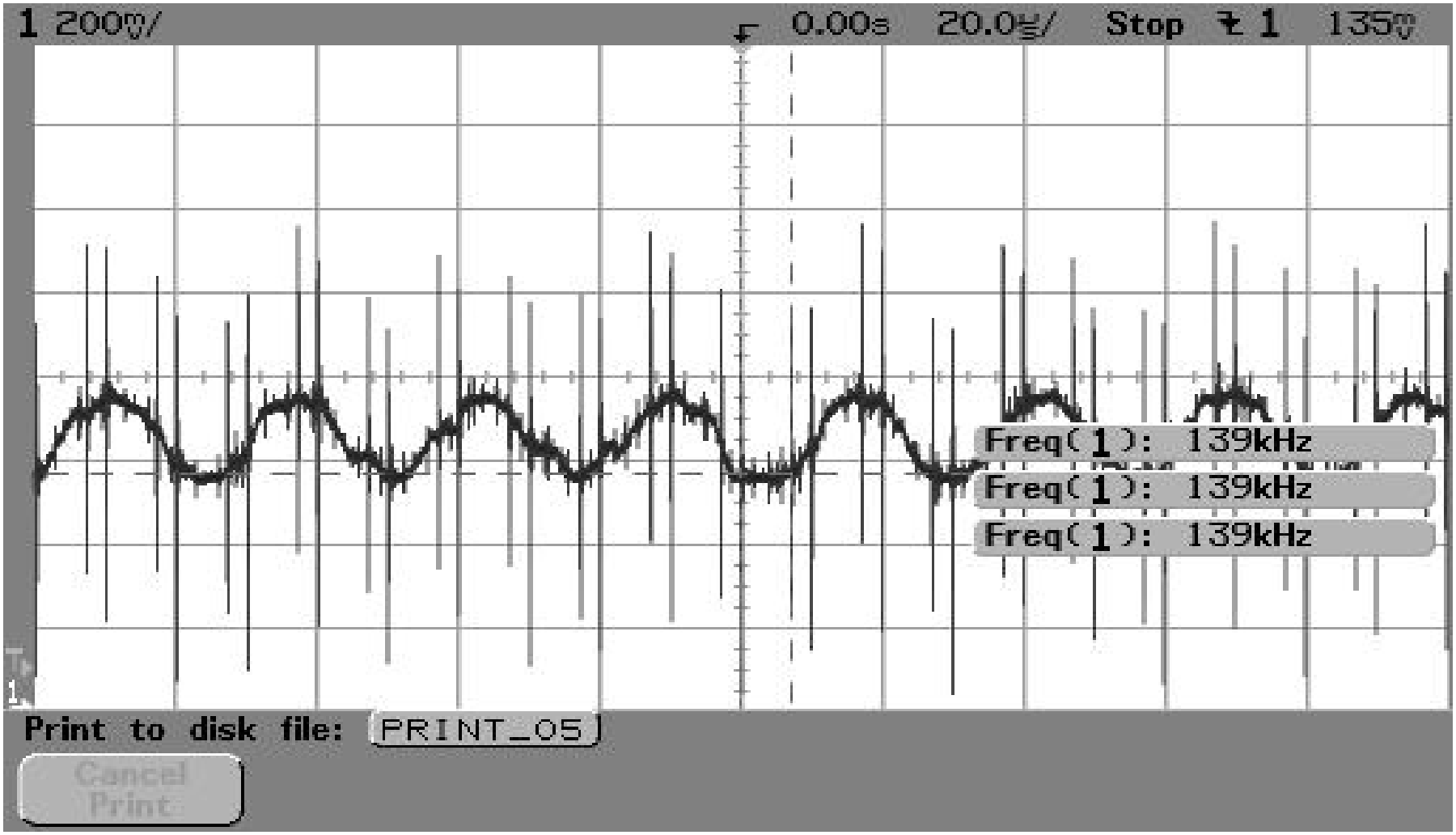
LDT Bus signals

RX_CK :



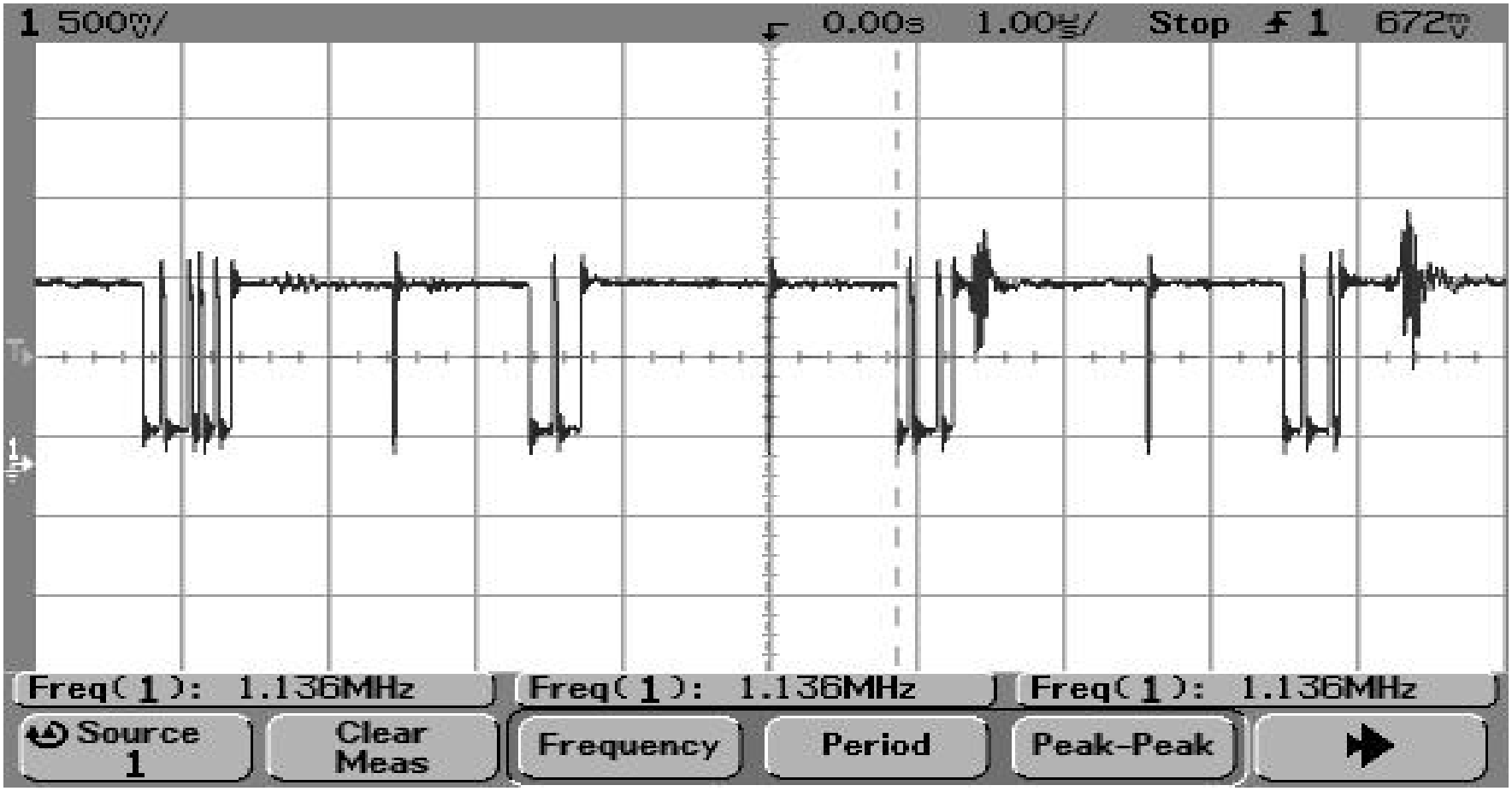
LDT Bus signals

RX_CK*:



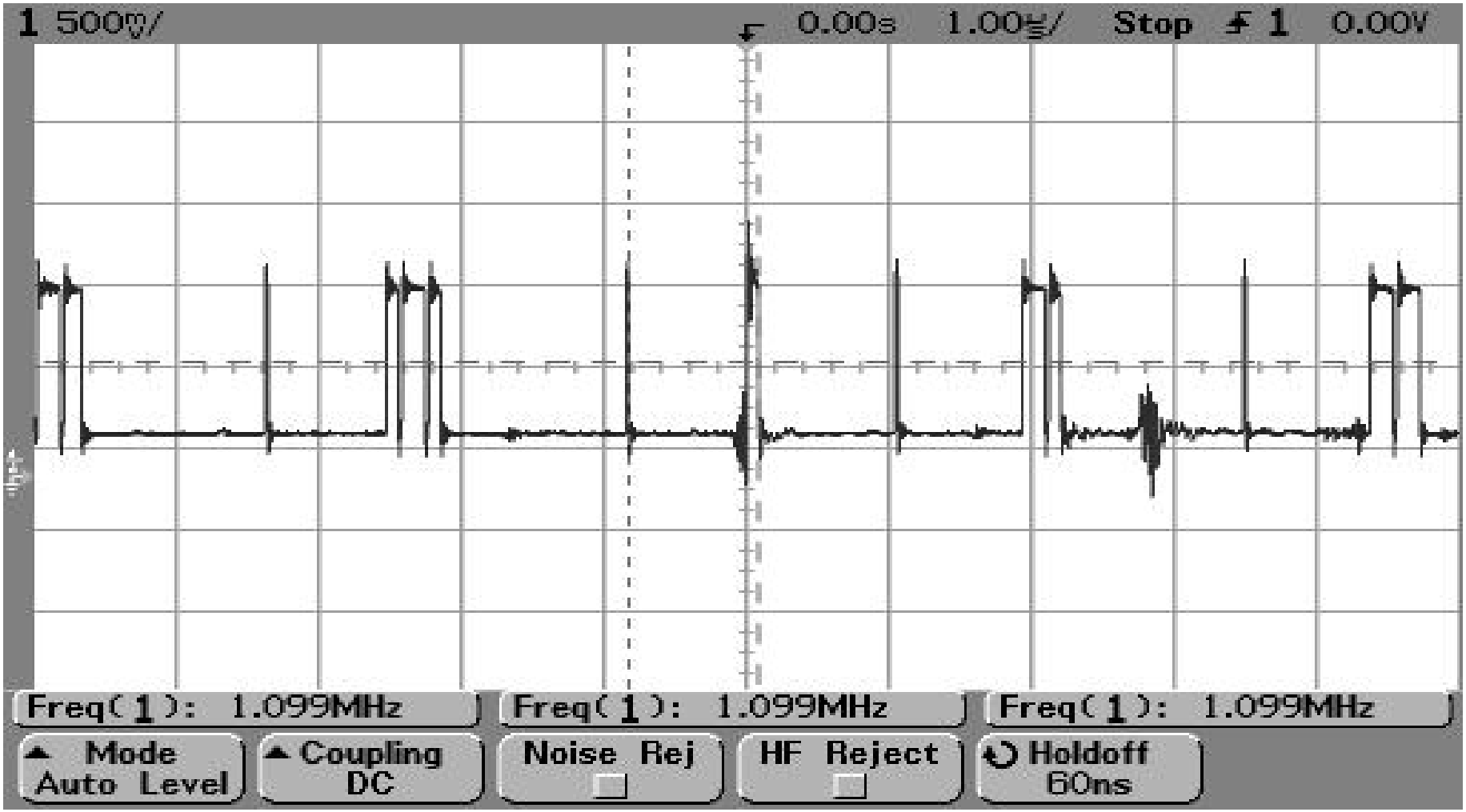
LDT Bus signals

RX_D8(continues pulses):



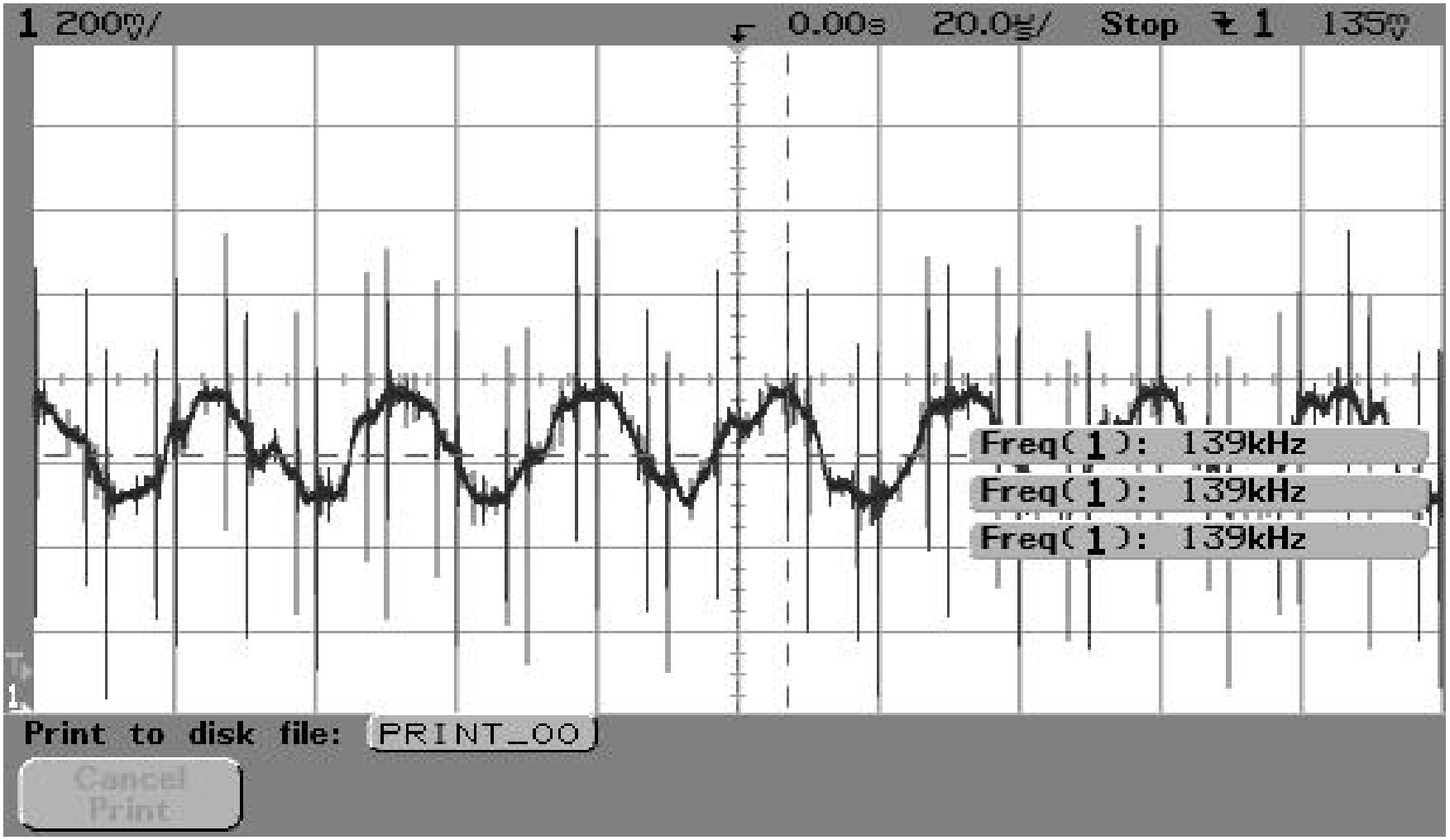
LDT Bus signals

RX_D8*(continues pulses):



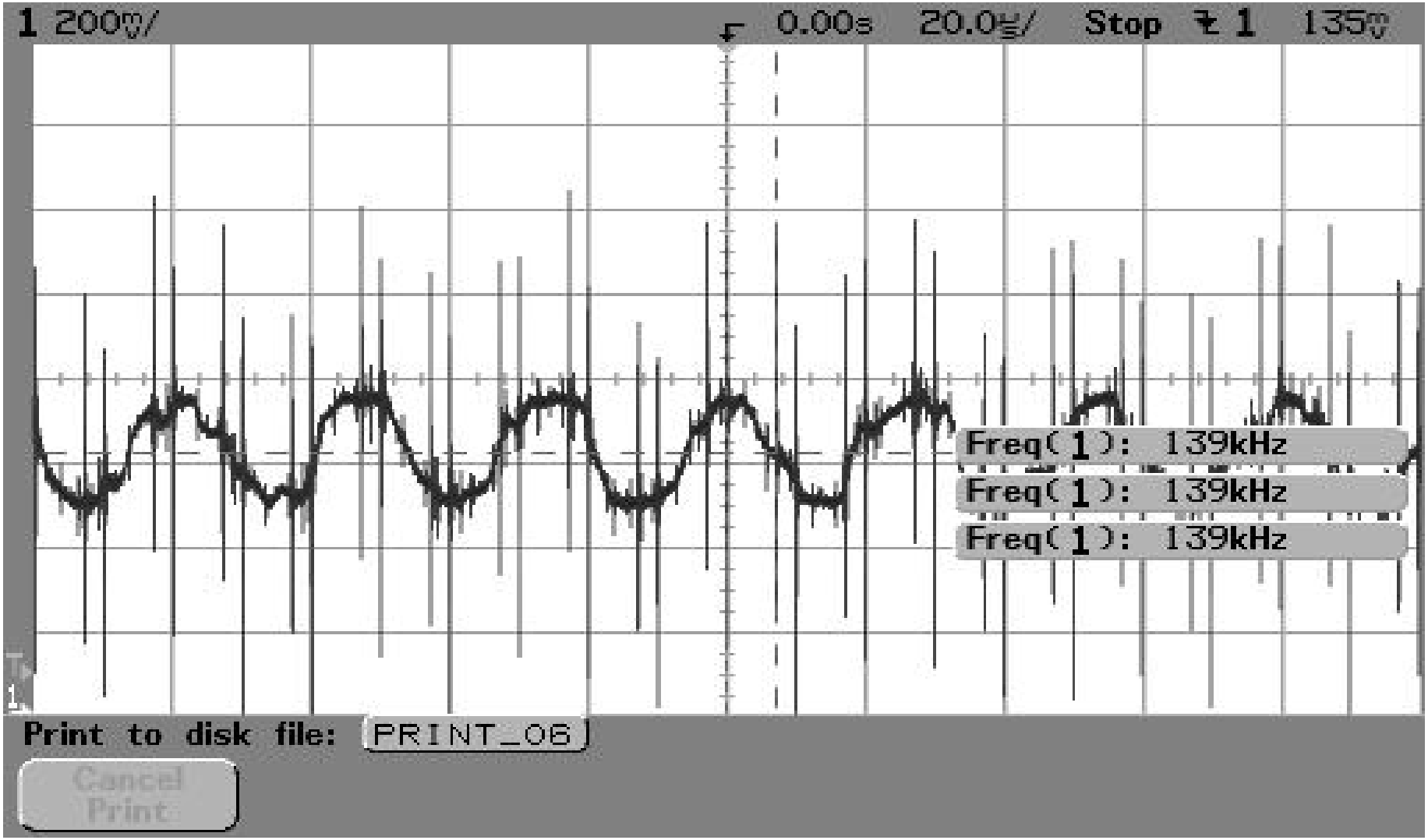
LDT Bus signals

TX_CK:



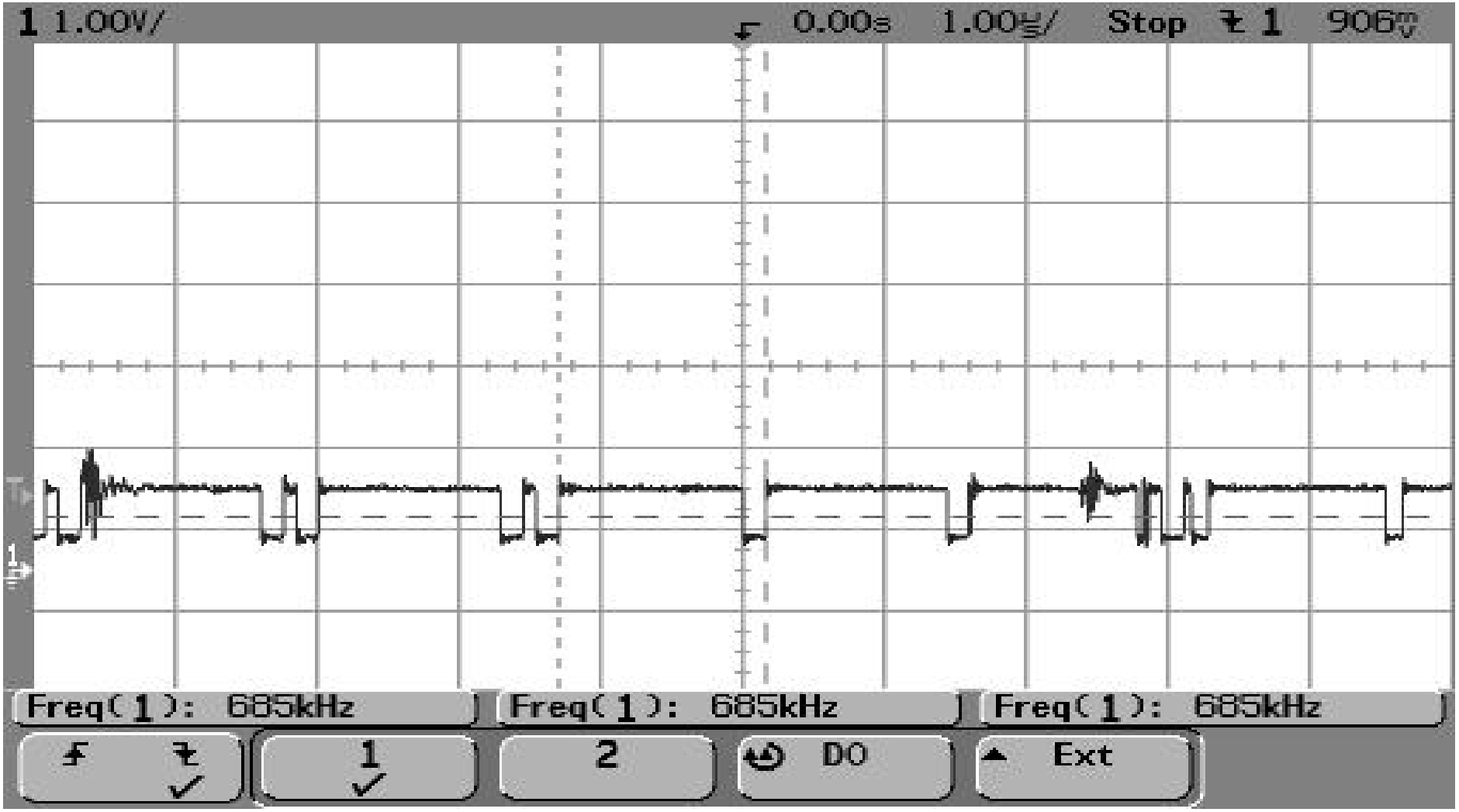
LDT Bus signals

TX_CK*:



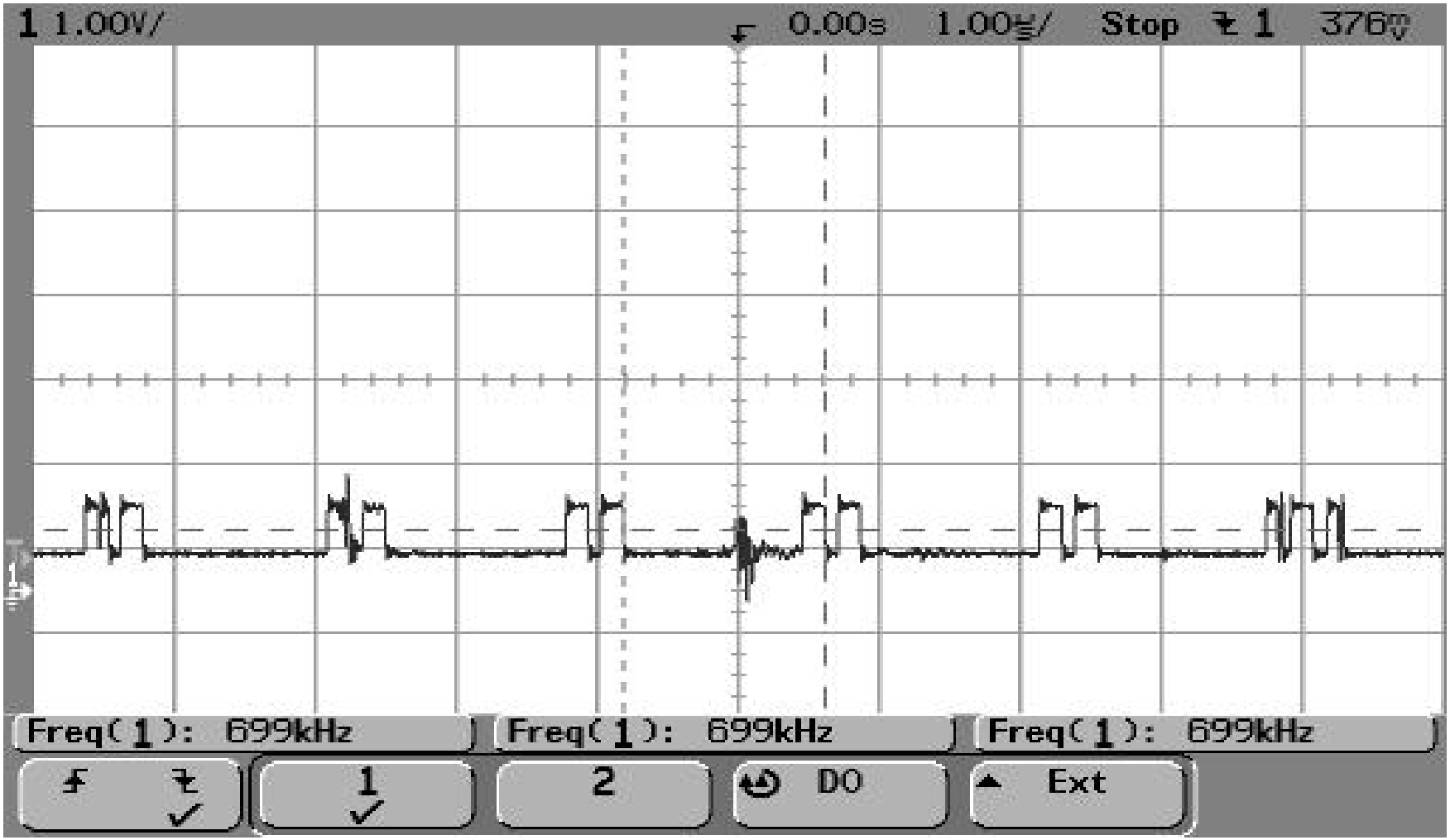
LDT Bus signals

TX_D8 (continues pulses):

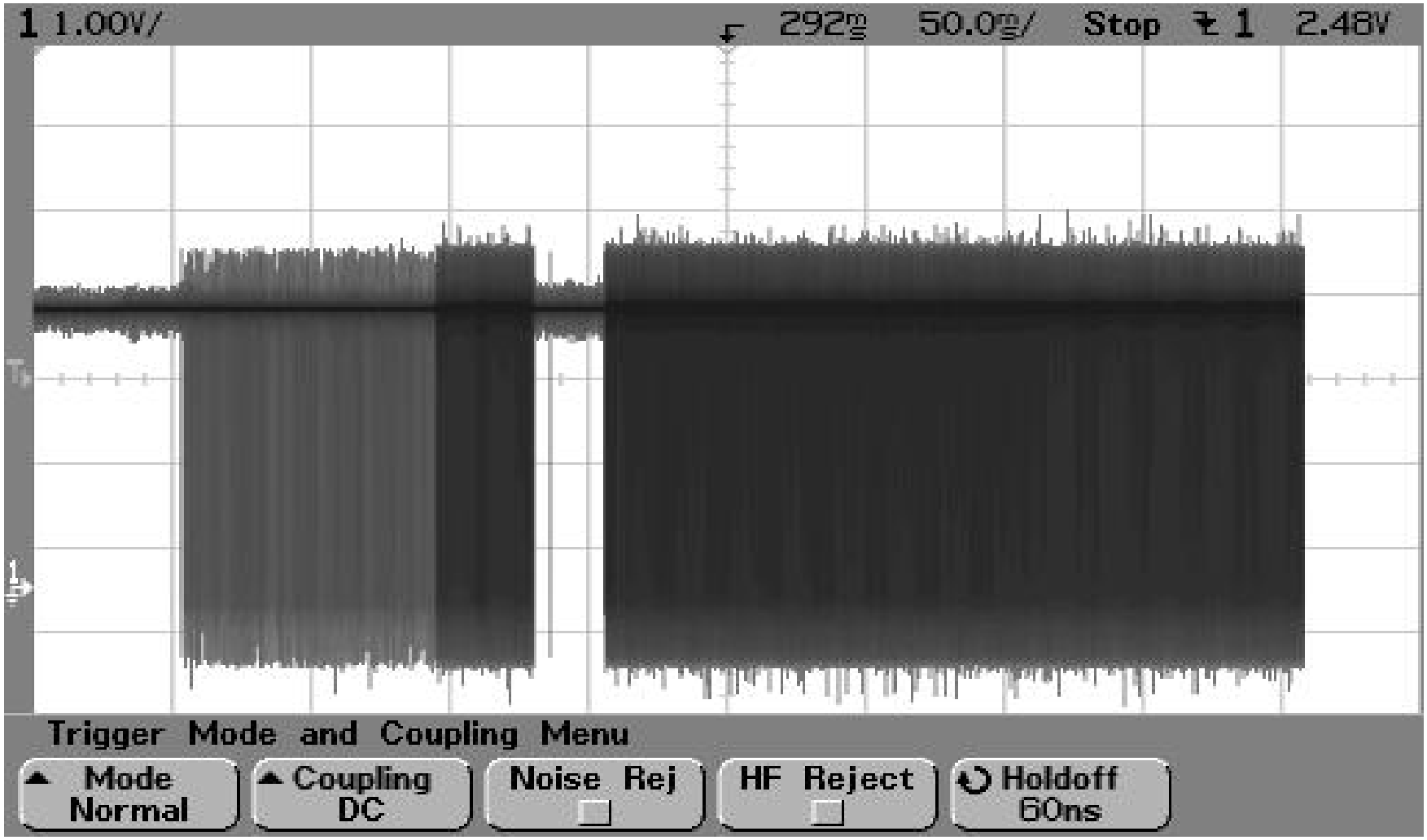


LDT Bus signals

TX_D8* (continues pulses):



Detail CPU fetch(R7D11.1)



CPU

Central processing Unit (CPU):

The foront side bus (FSB) to the CPU runs at 133 MHz at 64 bits , The CPU has a 128KB L2 cache
The CPU is an Intel PIII with the next features :
MMX and SSe instruction set enhancements
733Mhz internal clock
133Mhz Front Side Bus
32k L1 Cache
128k full speed L2 Cache integrated
The CPUID command makes that the CPU provide the information includes the CPU Type, Family, Model and Stepping ID.The features information includes also FPU, SIMD and MMX presence.The Cache information includes the CPU cache sizes and types.
The CPU ID command verify the presence of an MMX unit. Once the MMX unit is verified, a series of reads and writes are preformed on the MMx register set.
The test runs a mathematically intensive algorithm that stress the FPU and internal L1 processor cache.

CPU

The CPU Cache, 32 bit value represents the sizes and types of caches that exist inside the CPU.
The FERR# is the only input from the CPU to the MCPX (indicate an error from the coprocessor).
Check

- V_CLKREF voltage, it should be 1.3v on the C1R5#1
- V_1P5_VTT voltage, it should be 1.5v on the L1R1#2

MCPX

•*The Core Logic, or Media/Communications Processor (MCPX) contains all the core logic functions. Including the audio processor and interface controller, hard disk and DVD drive interfaces, USB controllers, and the system support functions.*

•The MCPX connects to the GPU via an LDT bus that provides 800MB/S transfer rate

•The Xbox System Services (XSS) provides the hardware initialization code , OS kernel , decryption and code signature verification, the application loading,and the drivers for some of the hardware features.

•The Xbox Title Library (XTL) is provided to the application developer as a linkable library, becoming part of the executable code loaded from the DVD media.

The XSS is contained in a Flash memory (1M byte) , the Boot ROM is interfaced,through the core logic.The upper 512 bytes is mapped to ROM internal to the MCPX , the lower 256 bytes of the Boot ROM are reserved for hardware initialization values for the MCPX and NV2B. These locations will be read directly by the core logic chips prior to CPU reset.

Immediately following the rising edge of the POWOK , which signals the end of the reset cycle, the MCPX reads the Dword of ROM space on the External ROM

External Boot ROM

interface at physical address 0xFF00:0000 , this location in the ROM should always be programmed to contain a ‘1’ in the least significant bit of that address.
The Xbox System Services (XSS) provides the hardware initialization code , OS kernel , decryption and code signature verification, the application loading , and the drivers for some of the hardware features.
The Xbox Title Library (XTL) is provided to the application developer as a linkable library, becoming part of the executable code loaded from the DVD media.
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Immediately following the rising edge of the POWOK , which signals the end of the reset cycle, the MCPX reads the Dword of ROM space on the External ROM interface at physical address 0xFF00:0000 , this location in the ROM should always be programmed to contain a ‘1’ in the least significant bit of that address.
Check the Data BUS ROM_D (0 to 7) Data lines for reading and writing data from and to the bus

LDT-Bus

LDT Lightning Data Transport Bus Interface

The LDT interface is made up of two 9 bit differential busses, one to the MCPx and one from the MCPx (each of these busses is unidirectional)

The MCPX implements an LPC interface for bridging to legacy ISA devices , the LPC header provides debug signals only and alternative means of connecting the boot ROM to the MCPX. Data transfer between the NV2B and MCPX are carried over a full duplex (LDT) data bus.This bus consists of two links , one serving transfers from NV2B to MCPX and the other servicing transfer from MCPX to NV2B.

The LDT Bus is a High speed , low pin count bus capable of combined transfers of up to 800MB/s (400MB/s up and 800MB down simultaneously)

Universal Serial Bus USB

Game Controller Ports

The test verifies the functionality of the USB ports (four ports and every Memory unit attached)
The test verify that data can be written to and read from the drives on the Memory Units.This test is also a way of generating traffic on the USB but without intervening with the Gamepads.
The length/size of the file to be written to and/or read from the drives on the Memory units are 4Kb to 100Kb

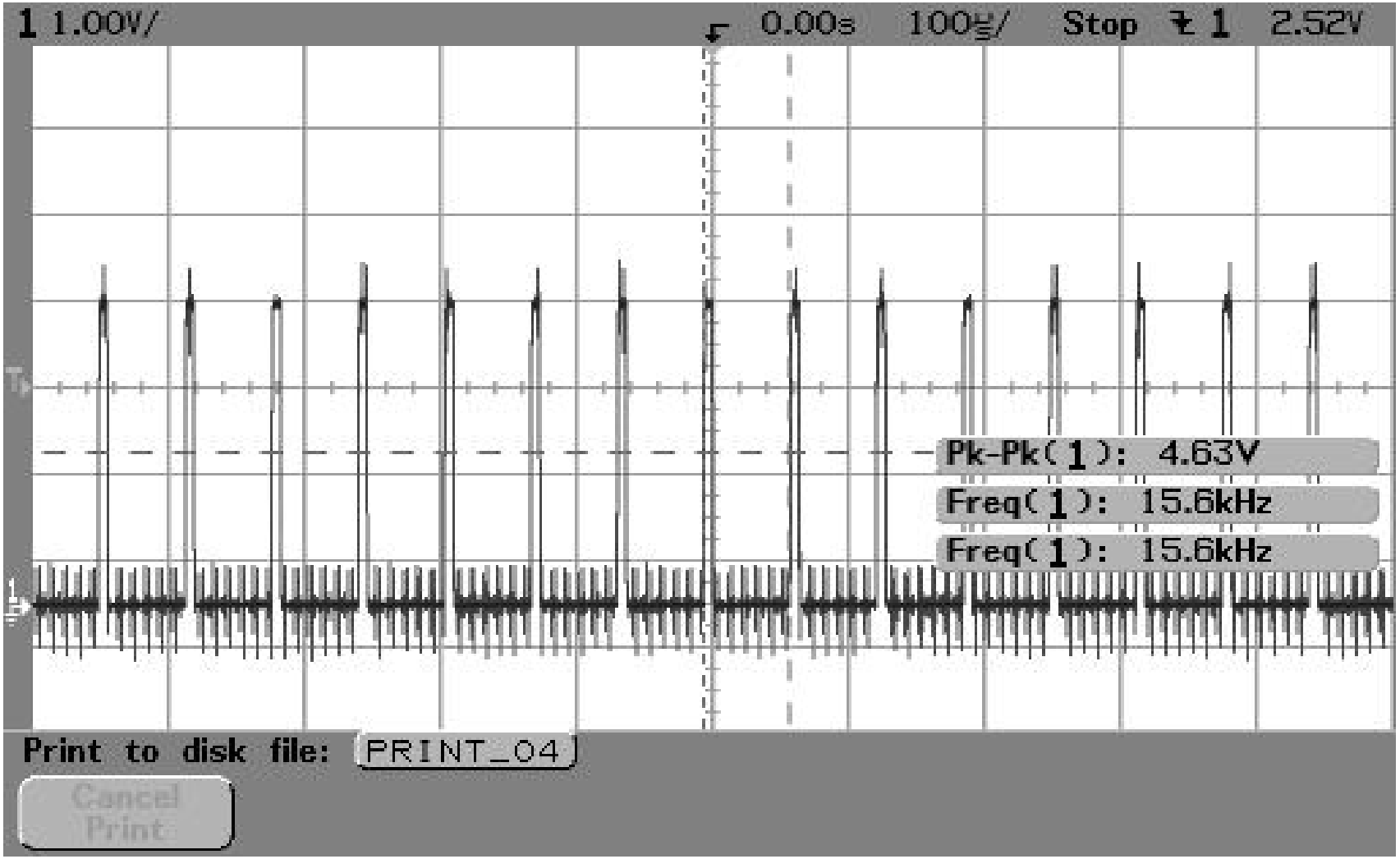
Check the USB four port

USB Bus

Description	Expected value	Signal name	Measurement point
USB reference voltage	1.7V	USB_VREF	R7E3#2
USB Power 1	+5V	USBPWR_1	J1G1#1
USB Power 2	+5V	USBPWR_2	J1G1#8
USB Power 3	+5V	USBPWR_3	J7G1#1
USB Power 4	+5V	USBPWR_4	J7G1#8
USB Composite Sync Output 1	15KHz	CSYNC_1	J1G1#4
USB Composite Sync Output 2	15KHz	CSYNC_2	J1G1#9
USB Composite Sync Output 3	15KHz	CSYNC_3	J7G1#4
USB Composite Sync Output 4	15KHz	CSYNC_4	J7G1#9
Differential DATA minus	See the signals	USB_(1 TO 4)	J1G1#3
Differential DATA plus	See the signals	USB_(1 TO 4)*	J1G1#2

USB Bus

CSYNC(1..4) for the Four UBS Ports signal form C2G2#1.



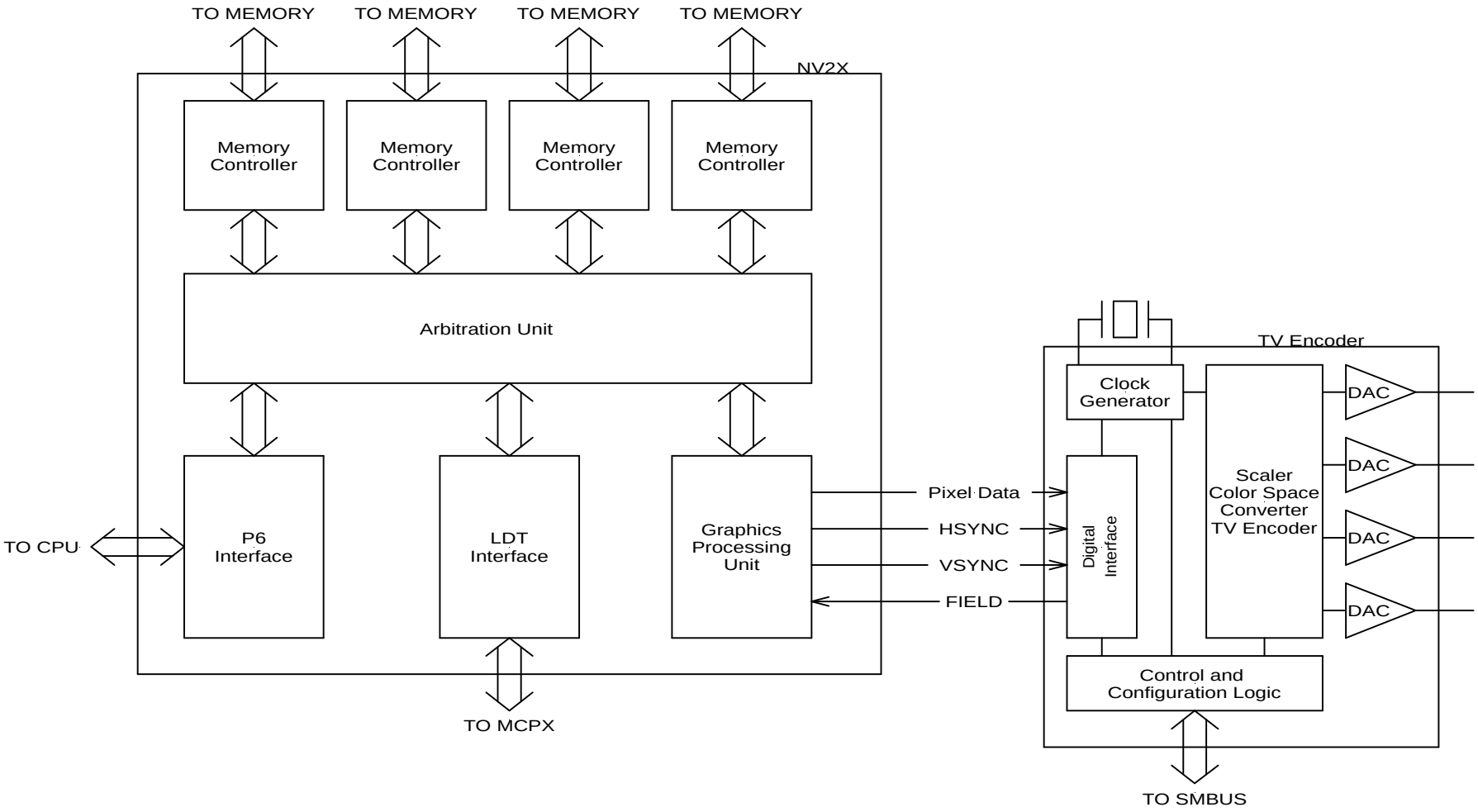
GPU (NV2B)

North Bridge and GPU (NV2B):

The NV2B is an integrated North Bridge memory controller and Graphics Processor Unit (GPU). Xbox uses unified memory architecture (UMA) to consolidate the system RAM and graphics RAM into a single memory pool. An advanced memory controller and bus arbitration unit bridges the CPU system bus, the GPU system bus and the LDT bus provides high speed access to the unified memory pool.

The North Bridge consists of a memory controller, a P6 front side bus interface
(Bus clocked at 133MHz), and LDT interface.
The memory controller also bridges the CPU system bus to the PCI bus for interface to the peripheral logic and IO controllers.

Graphics Subsystem Block Diagram



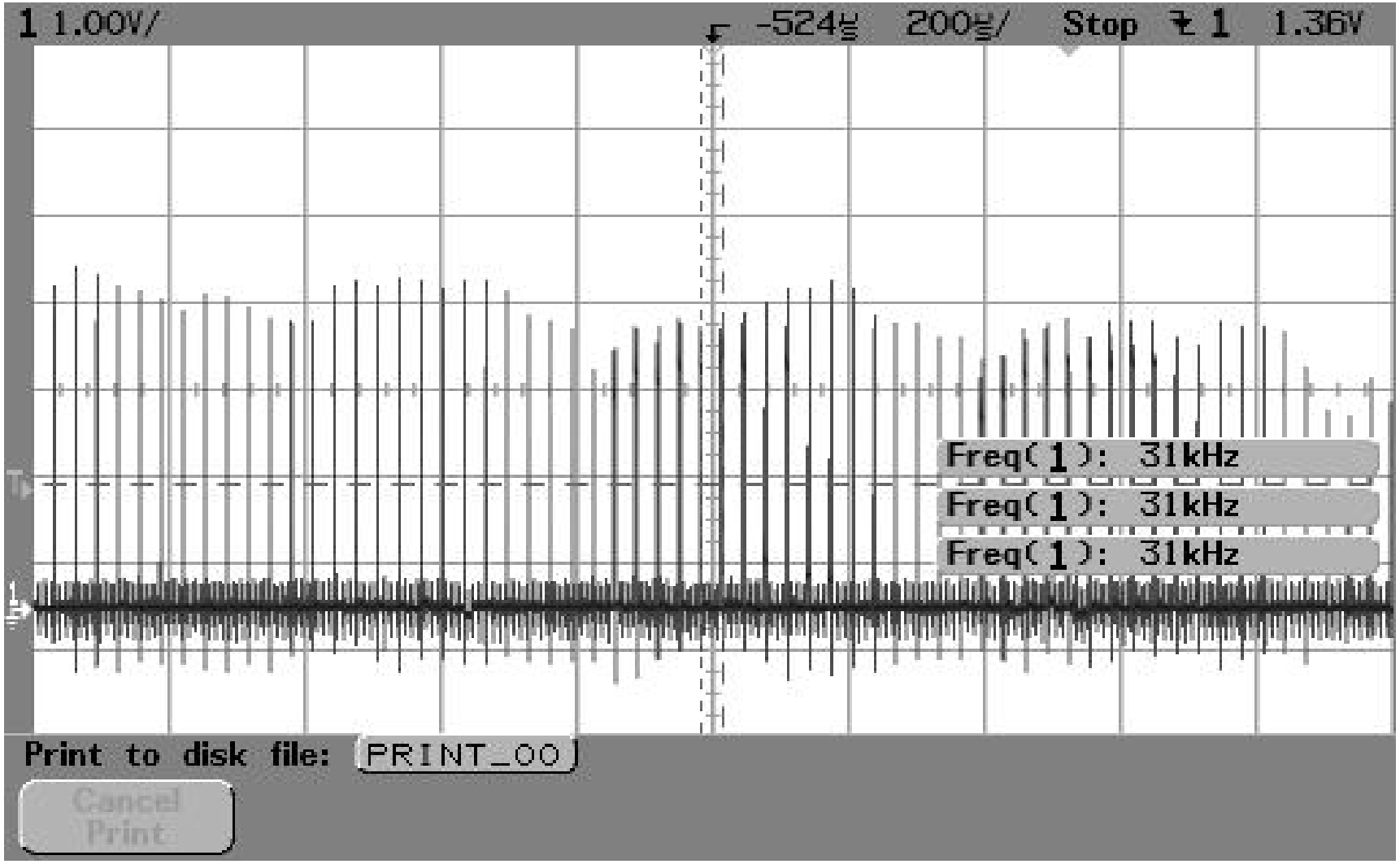
Memory Architecture and Performance

Xbox has a single memory pool, shared among all bus masters ; This is called a unified memory architecture (UMA) , The CPU, GPU (graphics processing unit), APU(Audio processing unit) ,and DMA (direct memory access from the DVD or from the hard disk)

Xbox's memory architecture consists of an Intel PIII/733, an NVIDIA north bridge chip with integrated graphics processing unit (GPU) and memory controller, an NVIDIA south bridge chip with integrated audio processing unit (APU) and peripheral interfaces, and four blocks of 16MB DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory), with all bus masters sharing the same memory (UMA), as shown in the following figure.

Memory

M_DATA(31..0) signal from the Memory Data Bus



Digital Versatile Disk (DVD) and Hard Disk Drive(HDD

DVD

The DVD Drive interfaces to the CPU though an AT- Attachment (ATA) Interface shared with the Hard Disk Drive. The ATA interface connector shall be a 40 pin header using 3.3V signaling.

12VCD power and the loader control/status interface was implemented on a secondary pin connector

IDE interface

Check on connector J8C1 (Primary IDE connector)
PCI_RESET
IDE PDD (0 to 15)
IDE_PDDREQ
IDE_PDDACK*
IDE_PDIOR*
IDE_PDIOW*
IDE_PIORDY
IDE_PINTR
IDE_PDCS1*
IDE_PDCS3*
IDE_PDA (0 to 2)
IDE_CSEL
IDE bus controlled by MCPX

CPU Voltage Regulator:

Check:

+12V on U2T1#24.
voltage on U2T1#9 VTTGATE (V_1P5_VTT)
voltage on U2T1#11 VCKGATE (V_2P5)
VCC (+5V) on Q2F1#3 (Drain)
Driver High (DH) on Q2F1#1 (Gate) Driver Low (DL) on Q1U1pin 1 (Gate)
VCC (+5V) on U2T1#21
V_CPUCORE on DB1R1,voltage around 1.7V
CPU work voltage v_1p5_VTT on FQ1N1#2
see the schematics pag.22

FAN

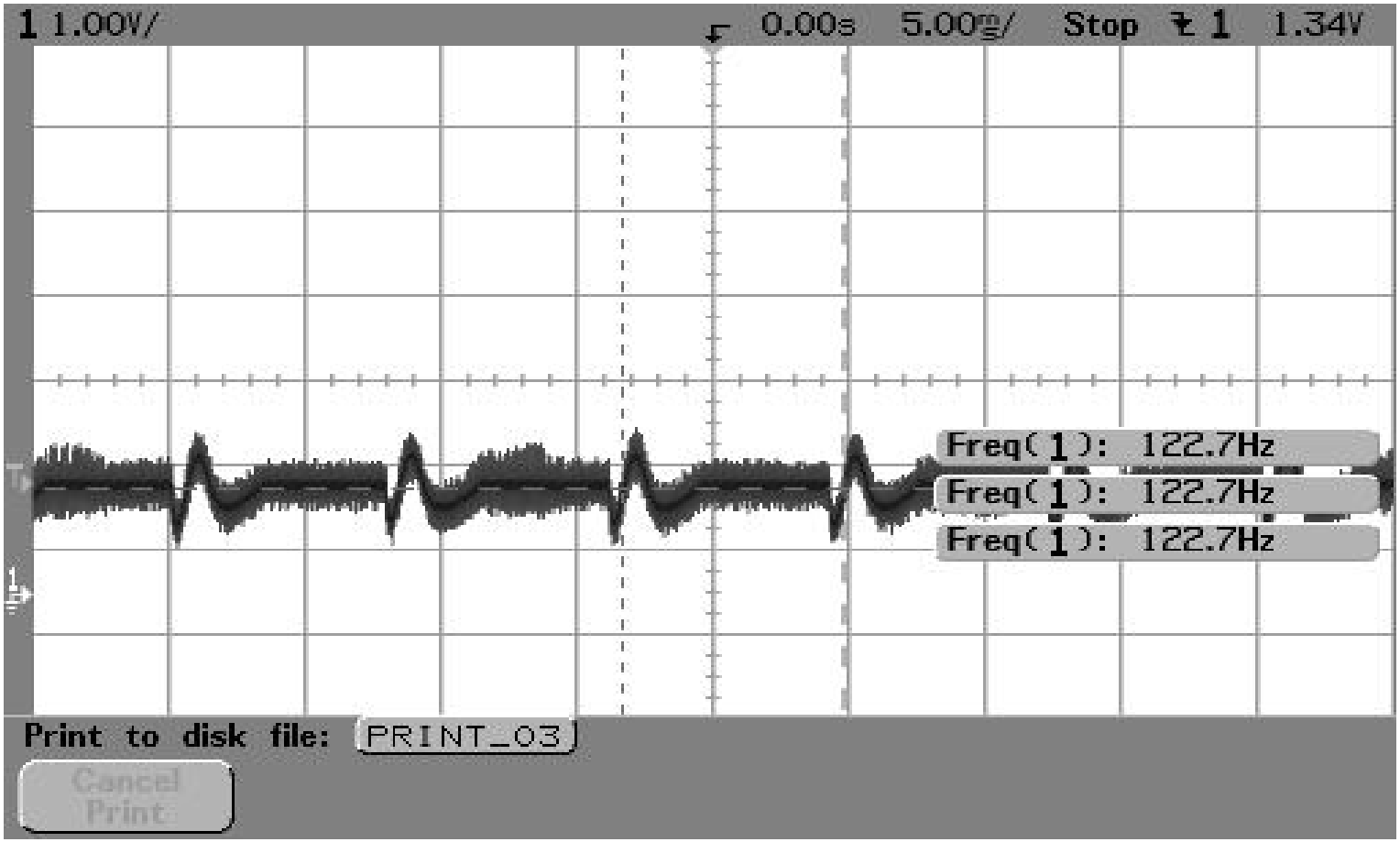
System Fan:

The SMC monitors the system temperature and control the speed of the system fan.The SMC(U7C1) IC to monitor system temperature.

Check

FANPWM PWM output for fan speed control U7C1#66

FANBK signal from U7C1#66



Thermal Sense

Thermal Sense:

The SMC shall monitors the CPU die temperature and the internal ambient air temperature in one location of the chassis, One IC (xcalibur) is sensing the temperature by utilizing an internal temperature sense diode.

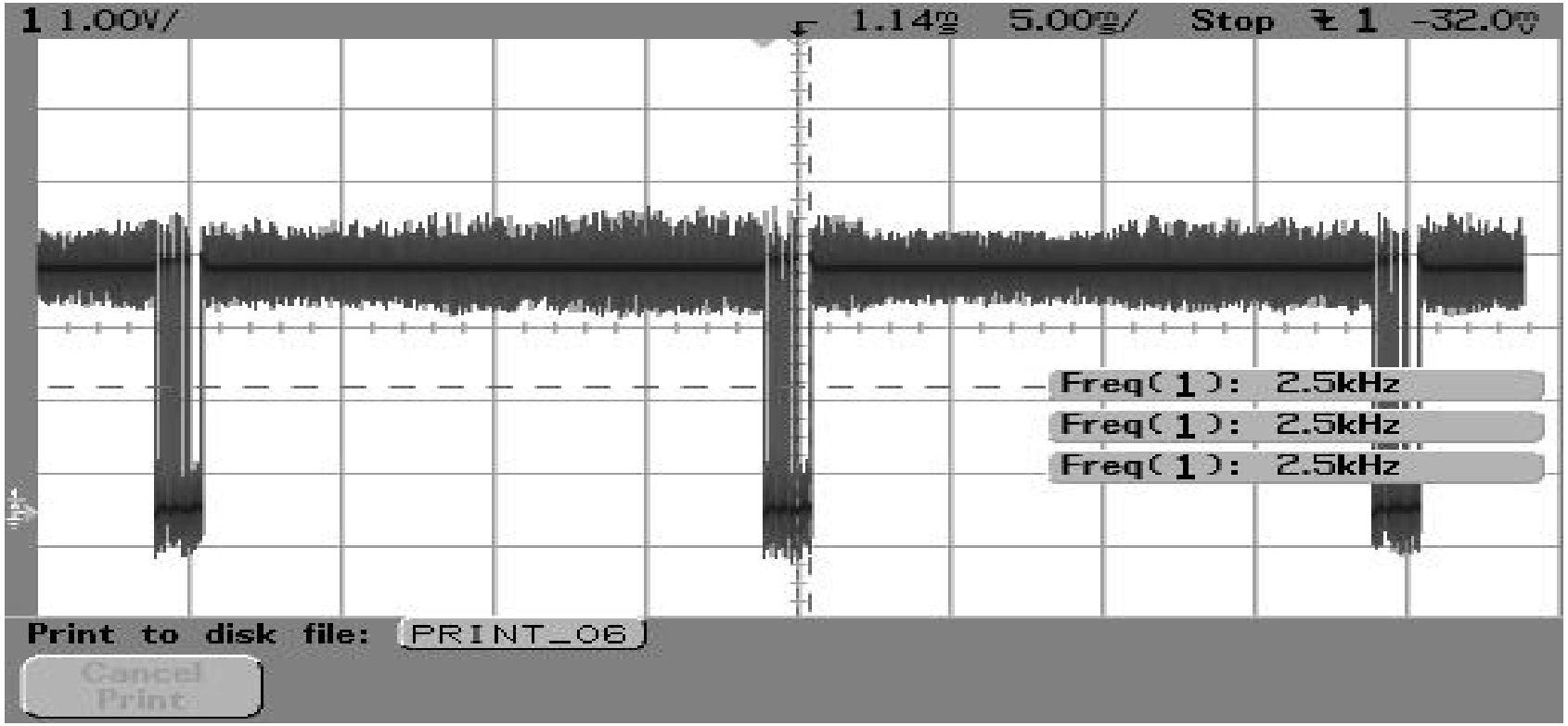
This device can measure the temperature of the Microprocessor using a diode connected NPN , the second measurement channel measures the output of an on chip U4B1 to monitor the temperature of the device and its environment, the xcalibur(U4B1) communicates over a two-wire serial interface compatible with the (SMBus) standards. Under and over temperature limits can be programmed into the device over the serial bus, and an alert output signals when the on-chip or remote temperature measurement is out of range.

Thermal Sense

Check

•C4A2 is buff 1000pF between H_THERMP and HTHERMN that are connected directly to the Microprocessor.

- Check if there is a data into the SMbus (SMB_SCL) U4B1#10 & 11 (SMB_SDA)
- See the u4b1#11 schematics page 24



3-D accelerated Audio

The audio subsystem consist of an Audio Processor Unit (APU) and a digital audio interface controller.The APUs and digital audio interface controller are integrated into the system core logic chip MCPX.The AC Link digital audio stream is converted to an analog signal by an audio DAC.

The DAC provides clocking for the AC-Link interface. The SMC drives a clamp control line that , when used in conjunction with the power supply POWON and the AC-Link nRESET signal, provides a means of power up and down the system.

Audio

The AC Link drives an audio codec provides analog line level audio outputs to the AVIP.

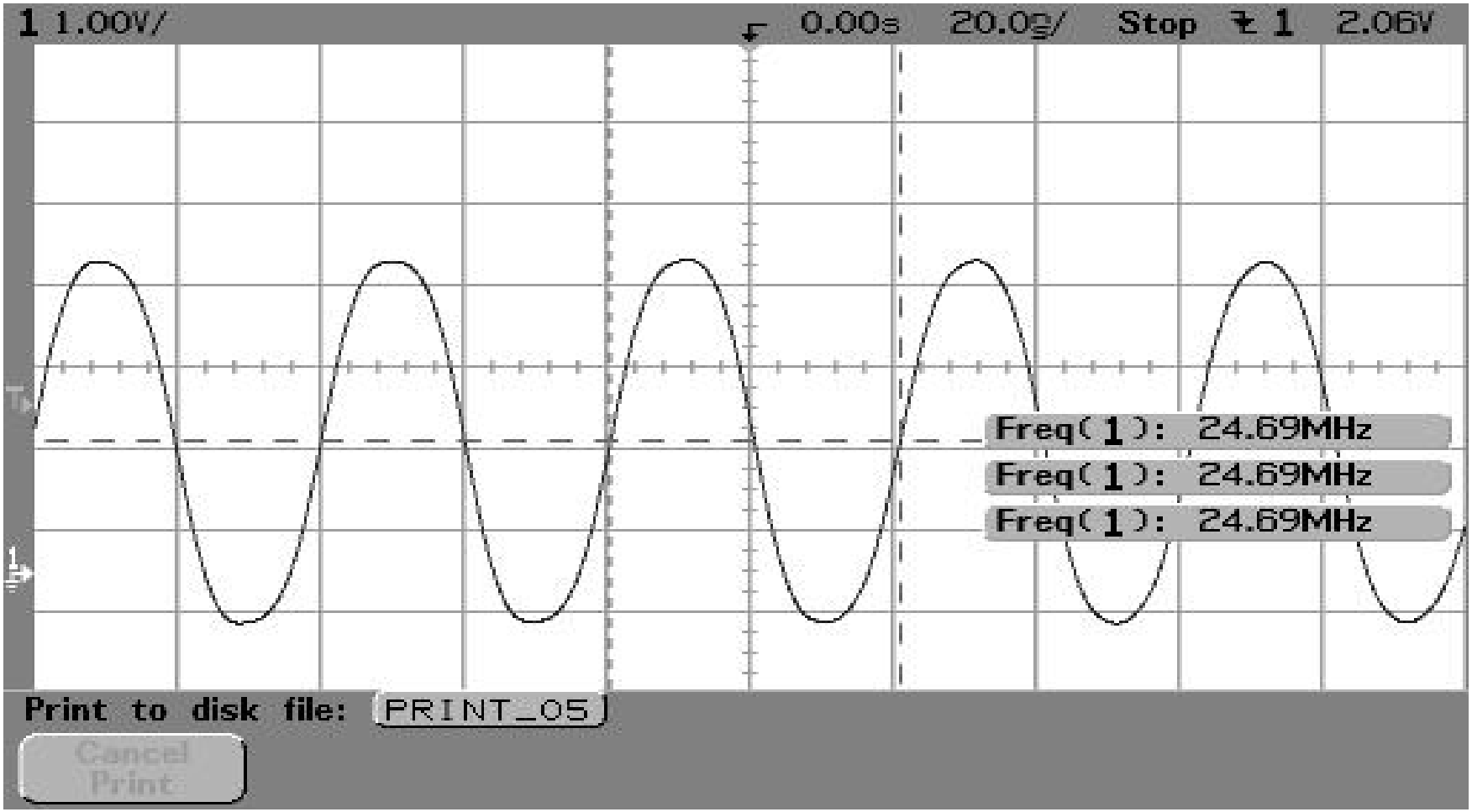
Check

- **AUD_5V_ANALOG U6A3#8 Analog positive supply**
- **AUD_CLAMP Mutes audio when driven high U7C1#59**
- **AUD_CK_24M U7C1#25.**
- **(CAP) U6A3#5 , signal about 3v, Reference input/output**
- **(Reset) U7C1#36 , The AUD_RST* sequence (low to high)**
- **(SYNC) U7C1#39 , Serial interface sync pulse from Ac-link controller or MCPX.**
- **(DATA OUT) U7C1#46 ,Serial data input**
- **(DATA_IN) U7C1#37 , Serial data output to AC-link controller or MCPX.**
- **(LINE OUT LEFT channel) U6A3#9 Main analogue output for left channel**
- **(LINE OUT RIGHT channel) U6A3#6 Main analogue output for right channel**
- **see the schematics page,32,33,39.**

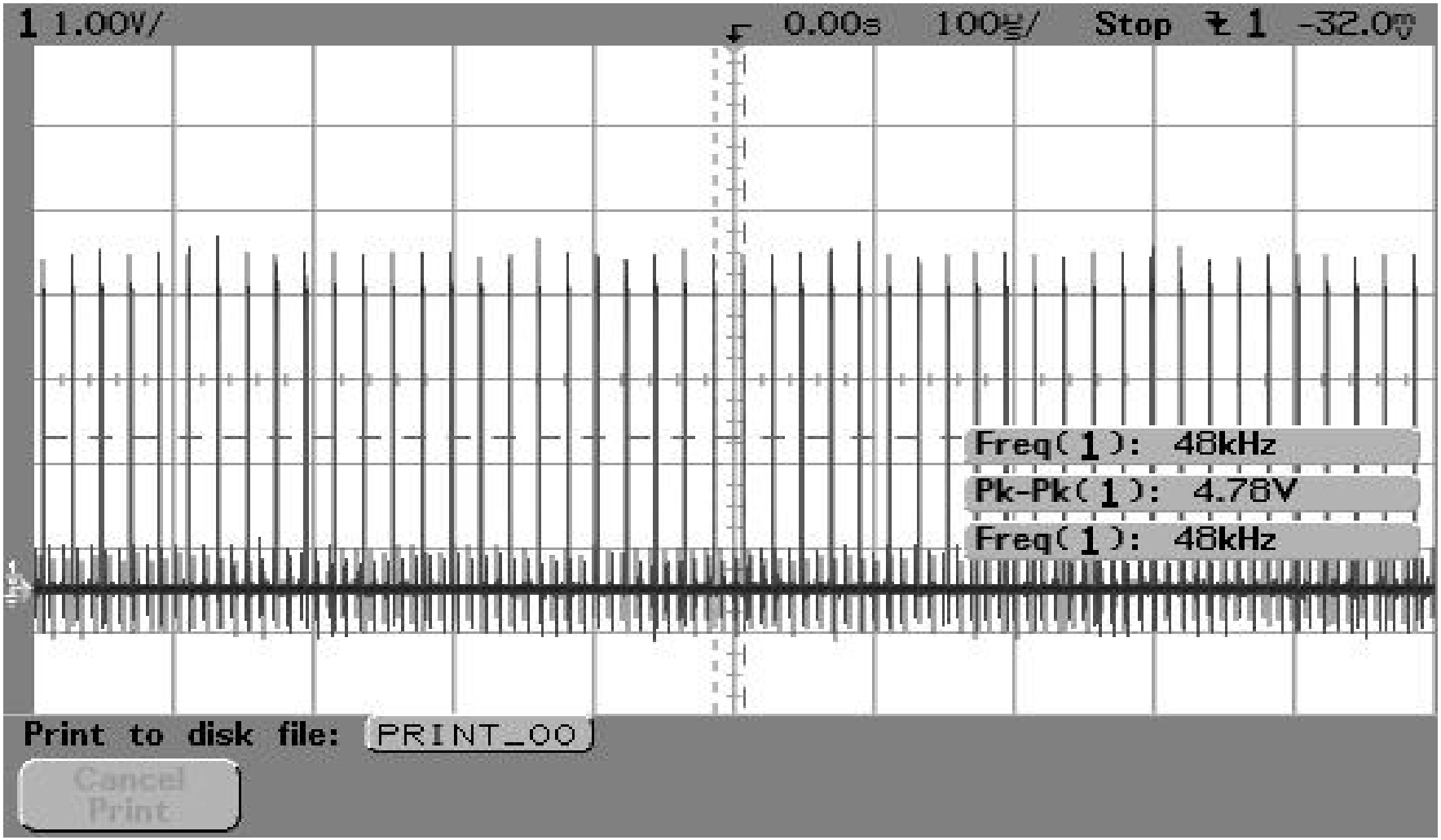
Audio

Clock Frequency Range	Frequency	Signal Name	Measurement point
Crystal Clock	24.576MHz	AUD_CK_24M	U7C1#25
BITCLK frequency	12.288MHz	AUD_BCLK	U7C1#38
SYNC frequency	48 KHz	AUD_SYNC	U7C1#39

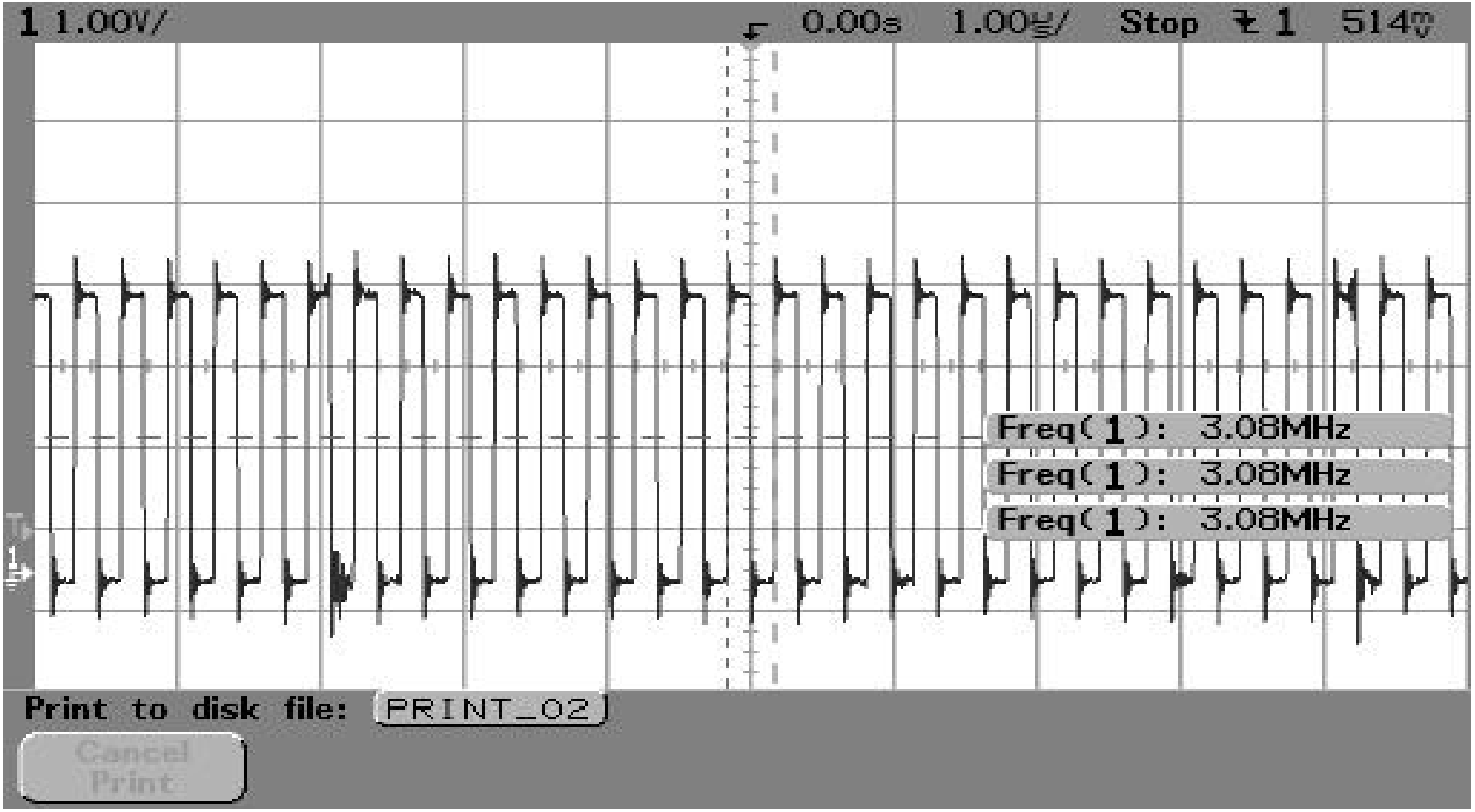
AUD_CK_24M signal from U7C1#25



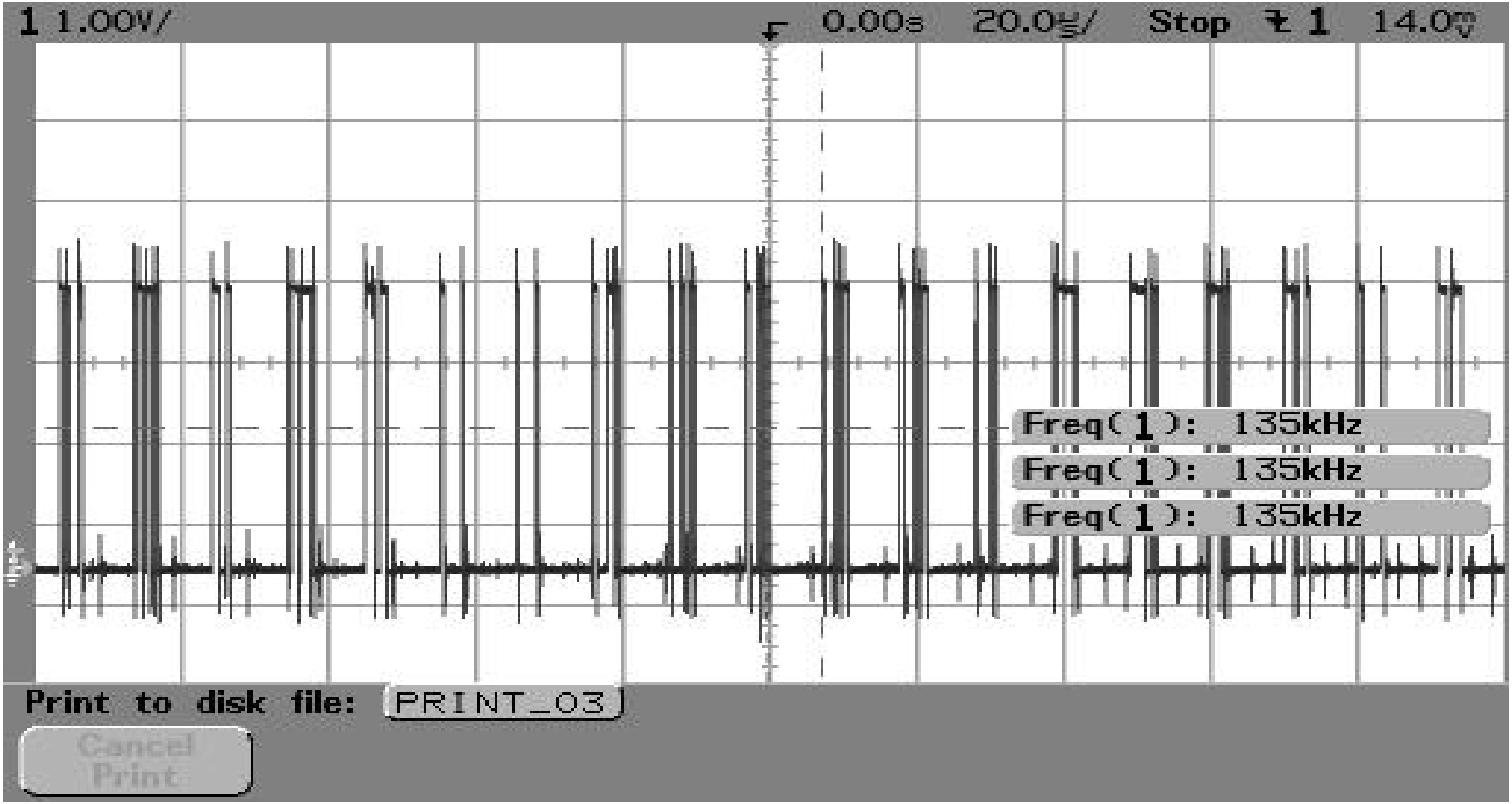
AUD_SYNC signal from U7C1#39



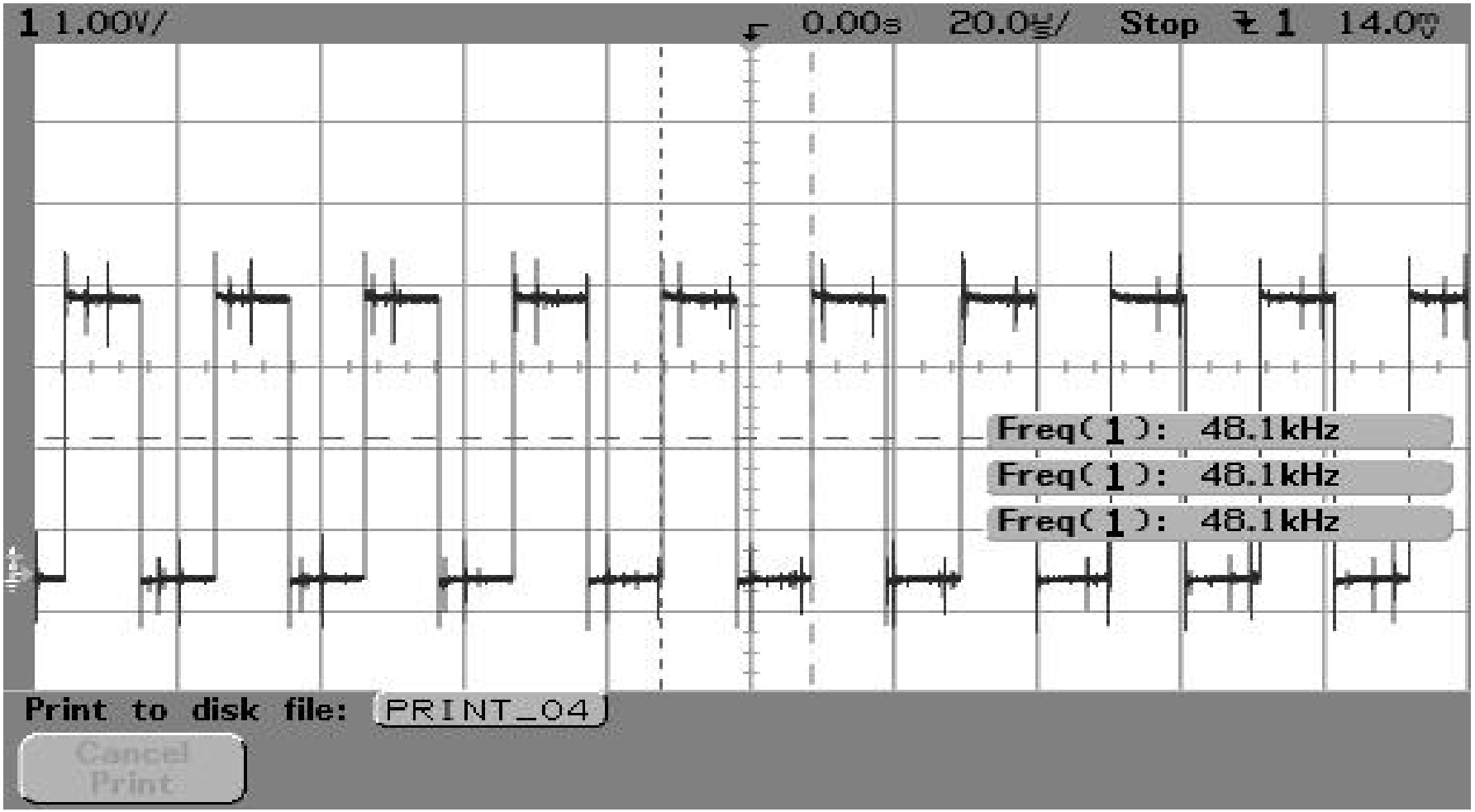
I2SBCLK signal from U6A3#3



I2SDATA signal from U6A3#2



I2S LRC signal from U6A3#1



Audio

Tuscany

The two voltage regulators for 12v the Audio section for the Operational Amplifiers and 5V for the Audio, the 12v of the ext power supply provides the voltage to this section.

The audio channels are independent, so every channel has their Audio Power /Filter Amplifier that takes the output from the Audio Codec.

The Audio Clamp circuitry are controlled by the Xycolps (u7c1) AUD_CLAMP line that control the Audio NO POP section for both channels.

The AVIP is a multi-pin connector that carries all (Audio and Video) the signals required to connect the Xbox console to a television and audio system.

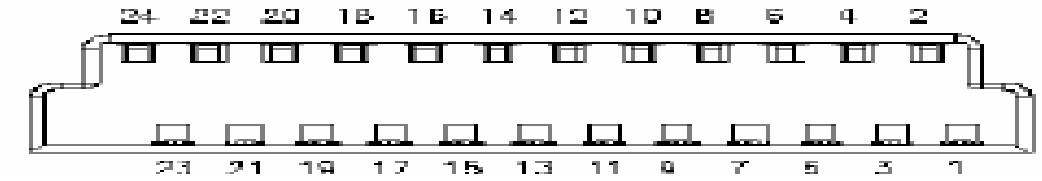
The AVIP has two audio interface ports; line-level stereo audio (left and right channels) is output directly , and a logic-level SPDIF output is provided for interface to an external coaxial of fiber optic driver. This digital signal is provided by the MCPX.

XBlade

- The two voltage regulators for the Audio section (+9V(MC7809 9v regulator) for the Operational Amplifiers and 5V for the Audio Codec that are provided by the 9V reg that go though 5V regulator circuitry (Q5N1) ,and the BIAS cames from Q5M2 that provides a DC offset fro the audio signal , the 12v of the ext power supply provides the voltage to this section.
- The audio channels are independent , so every channel has their Audio Power /Filter Amplifier that takes the output from the Audio Codec.
- The Audio Clamp circuitry are controlled by the SMC AUD_CLAMP line that control the Audio NO POP section for both channels.
- The AVIP is a multi-pin connector that carries all (Audio and Video) the signals required to connect the Xbox console to a television and audio system.
- The AVIP has two audio interface ports; line-level stereo audio (left and right channels) is output directly , and a logic-level SPDIF output is provided for interface to an external coaxial of fiber optic driver. This digital signal is provided by the MCPX.

AVIP Connector Pin out

Pin	Signal Name	Direction	Comment
1	DCOUT	OUT	The output of this pin provides a current-limited DC power supply for active AV Pack circuitry.
2	LINE OUT (R)	OUT	This pin outputs line-level Right channel linear audio.
3	LINE OUT (L)	OUT	This pin outputs line-level Left channel linear audio.
4	GND	-	This ground is provided for connection to the Right channel audio cable shield.
5	GND	-	This ground is provided for connection to the Left channel audio cable shield.
6	SPDIF	OUT	This pin is the SP-DIF logic-level output.
7	Not Used	-	
8	SCARTRGB	OUT	This signal is driven to +5V when the RGB outputs are driven in SCART mode, otherwise it is driven to ground.
9	MODE1	IN	Video output mode select pin 1
10	GND	-	This pin provides a convenient grounding point for the MODE1 input if needed.
11	MODE2	IN	Video output mode select pin 2
12	GND	-	This pin provides a convenient grounding point for the MODE2 inputs if needed.
13	MODE3	IN	Video output mode select pin 3
14	GND	-	This pin provides a convenient grounding point for the MODE3 inputs if needed.
15	STATUS	OUT	SCART Status Pin
16	GND	-	Ground connection for pin 18 (Pb)
17	GND	-	Ground connection for pin 19 (C/Pr)
18	Pb B	OUT	This pin outputs the Pb component signal in HDTV mode, and the BLUE component signal in RGB SCART mode.
19	C Pr R	OUT	This pin outputs the Chroma signal in SDTV mode, and the Pr component signal in HDTV mode, and the RED component signal in RGB SCART mode.
20	GND	-	Ground connection for pin 22 (Y)
21	GND	-	Ground connection for pin 23 (CVBS)
22	Y G	OUT	This pin outputs the Luma signal in both SDTV and HDTV modes, and the GREEN component signal in RGB SCART mode.
23	CVBS	OUT	This pin is dedicated to the Composite Video Out (CVBS) in SDTV mode. In HDTV mode, this pin is not used.
24	DCRETURN	-	This pin is specifically designated to carry the DC return current.



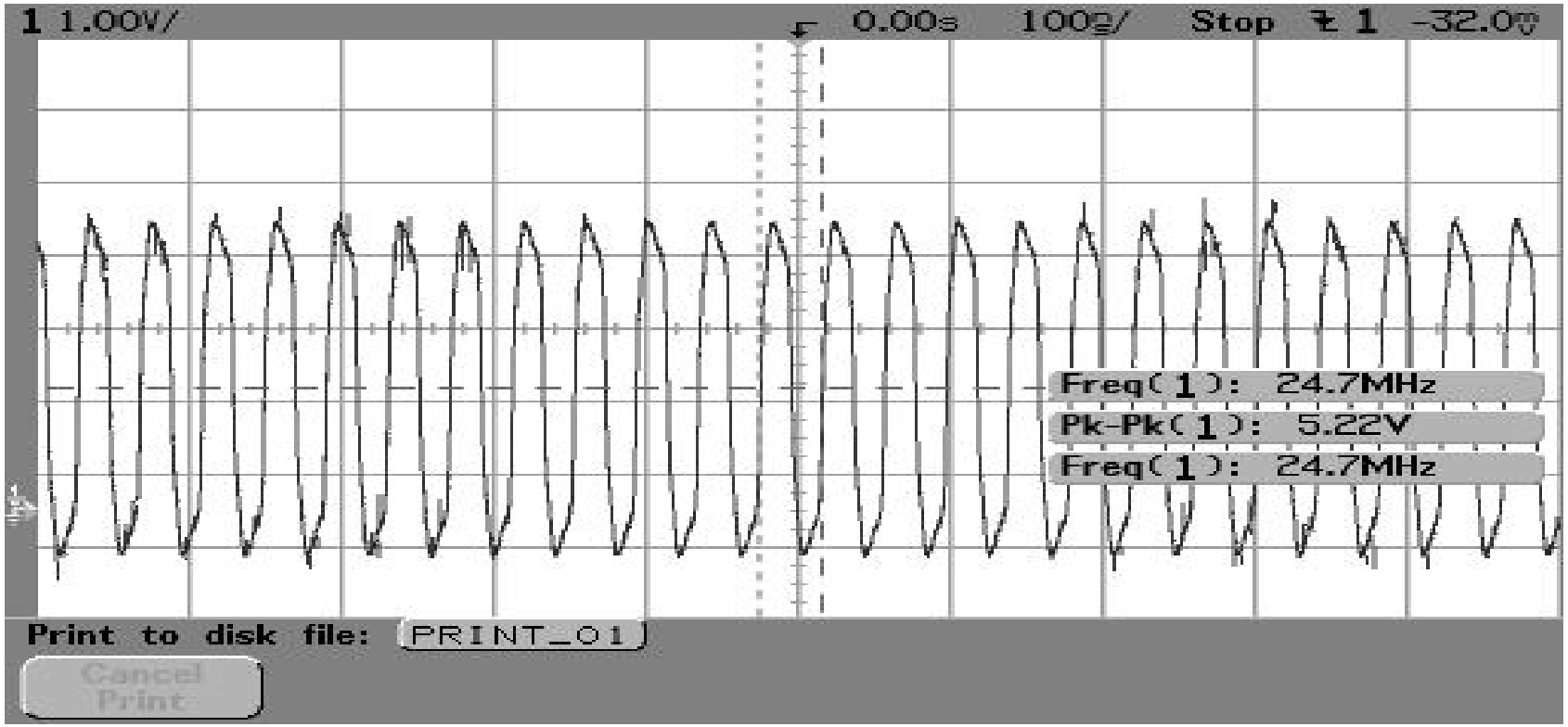
Video Mode Definitions

AVIP Mode Input (Pin)			Video Mode	AVIP Video Output (Pin)			
MODE1 (9)	MODE2 (11)	MODE3 (13)		(23)	(22)	(19)	(18)
OPEN	OPEN	OPEN	NO PACK	-	-	-	-
OPEN	OPEN	GND	RFU Mode	CVBS	Y	C	-
OPEN	GND	OPEN	POWER OFF	-	-	-	-
OPEN	GND	GND	HDTV Mode (Y/Pr/Pb)	-	Y	Pr	Pb
GND	OPEN	OPEN	SDTV Mode Analog Audio	CVBS	Y	C	-
GND	OPEN	GND	Not Used	-	-	-	-
GND	GND	OPEN	SDTV Mode Analog/Digital Audio	CVBS	Y	C	-
GND	GND	GND	SDTV SCART Mode Analog/Digital Audio	CVBS CVBS	- G	- R	- B

TV Encoder

The TV Encoder provides four video DAC outputs. To support all the composite, s-Video, and component modes, the four outputs must be multiplexed.

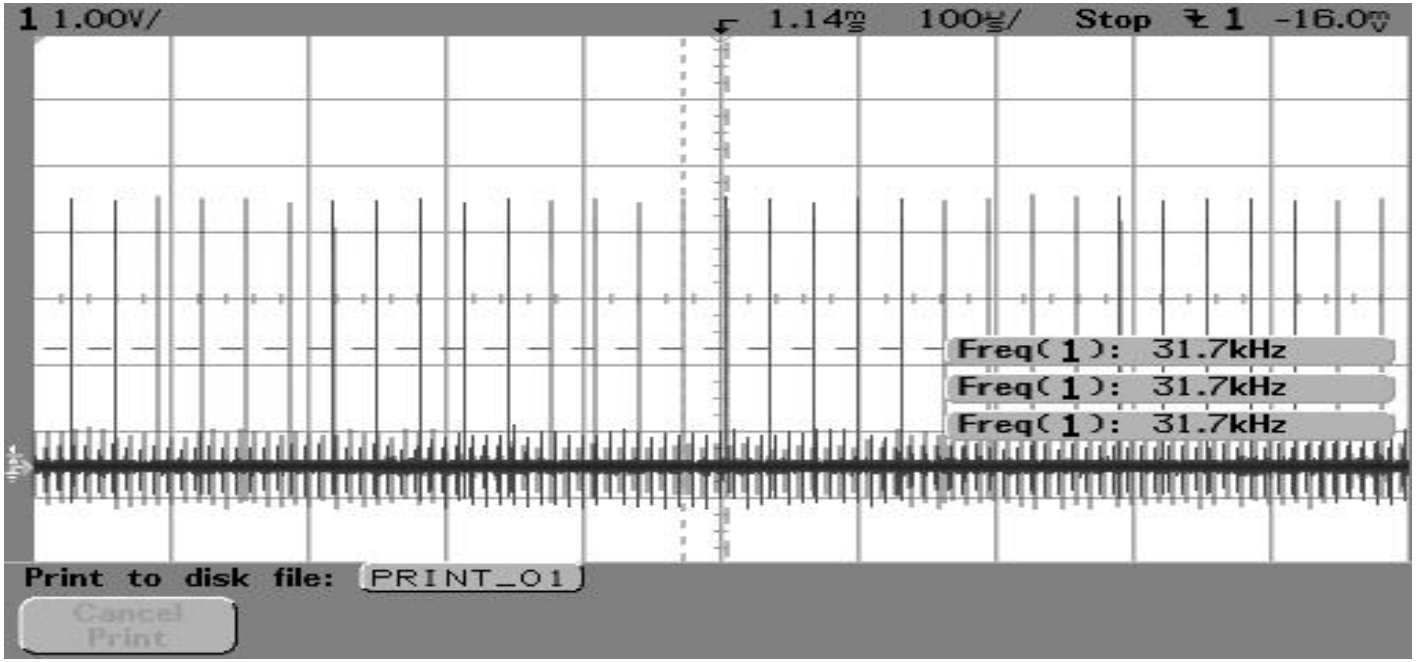
The CLKO purpose is to inform the graphics controller the exact frequency at which the data must be sent to the encoder. Timing signals, HSYNC*,VSYNC*, and BLANK* , are received by the encoder as inputs.



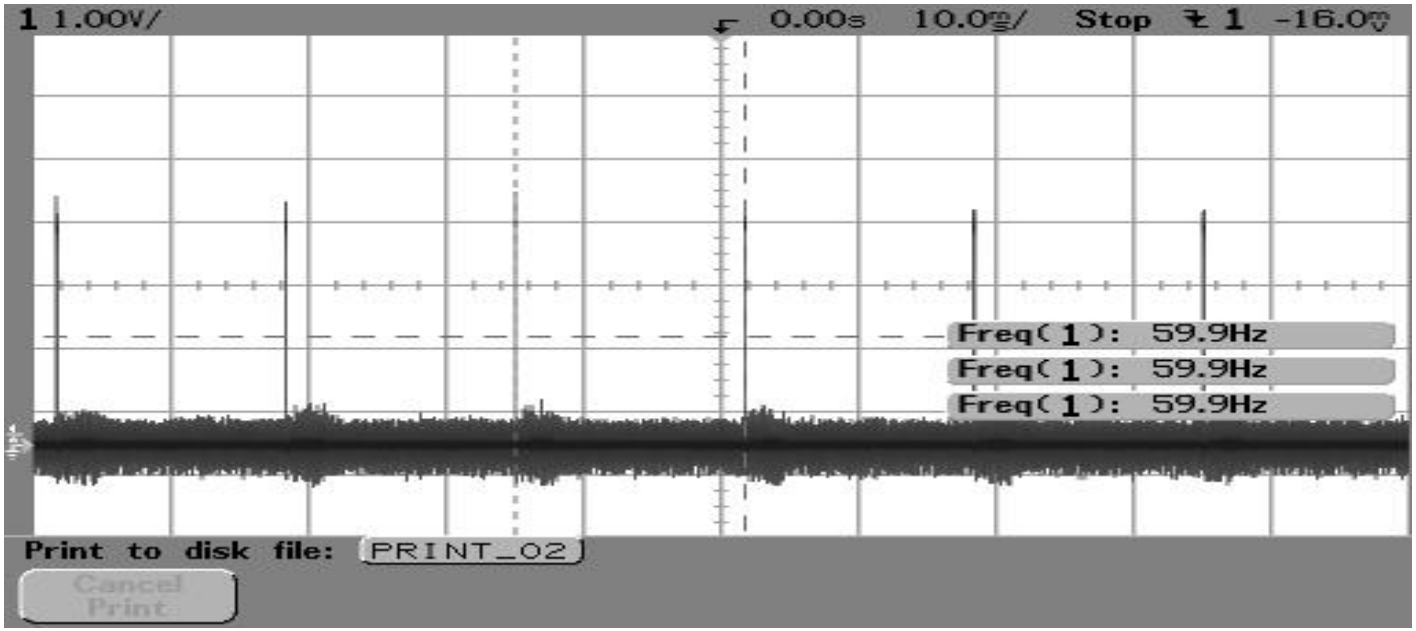
DVO_CLKO_R signal from C4B1#1

TV Encoder

HSYNC*(U4B1#30)

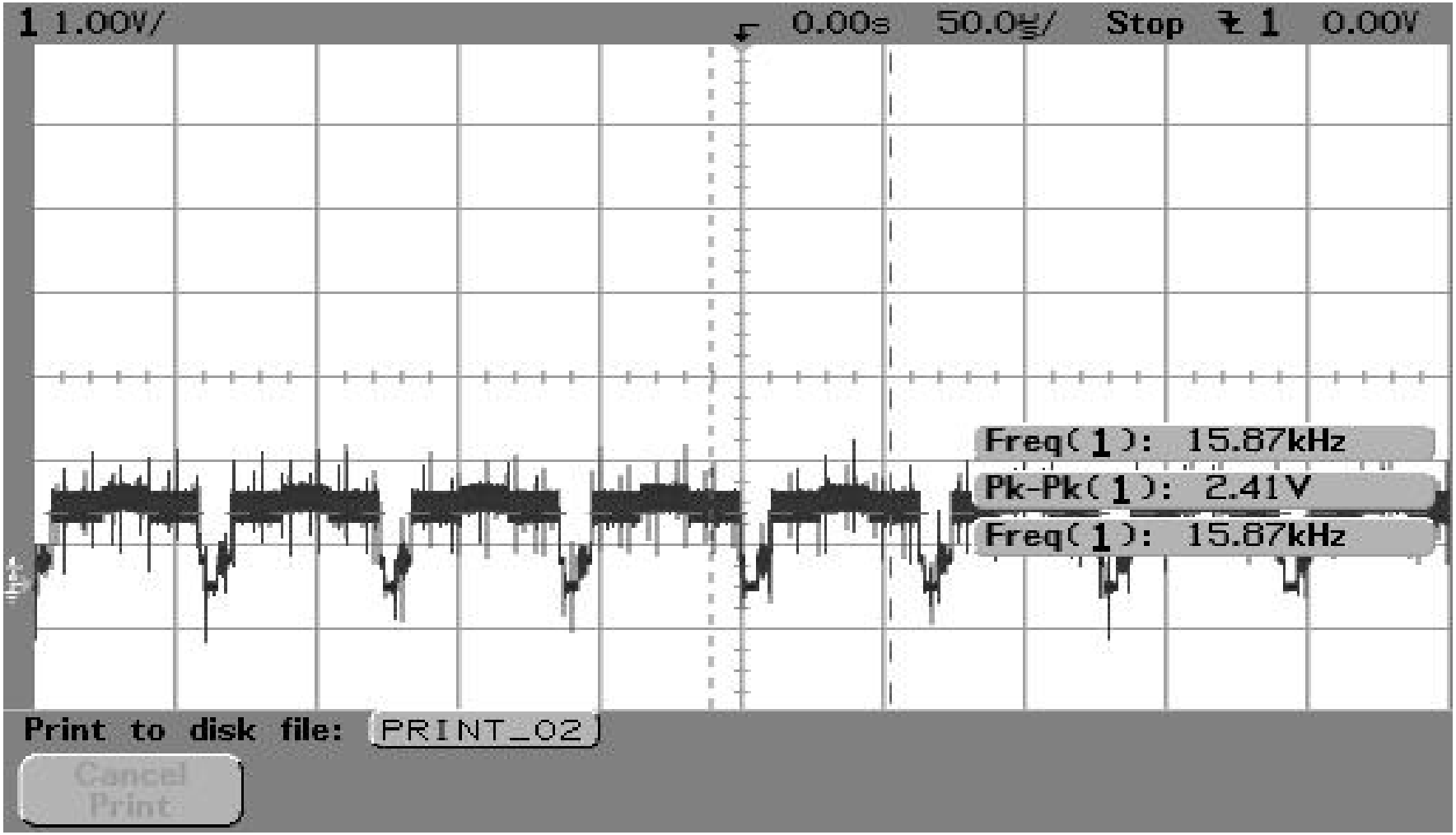


VSYNC*(U4B1#31)

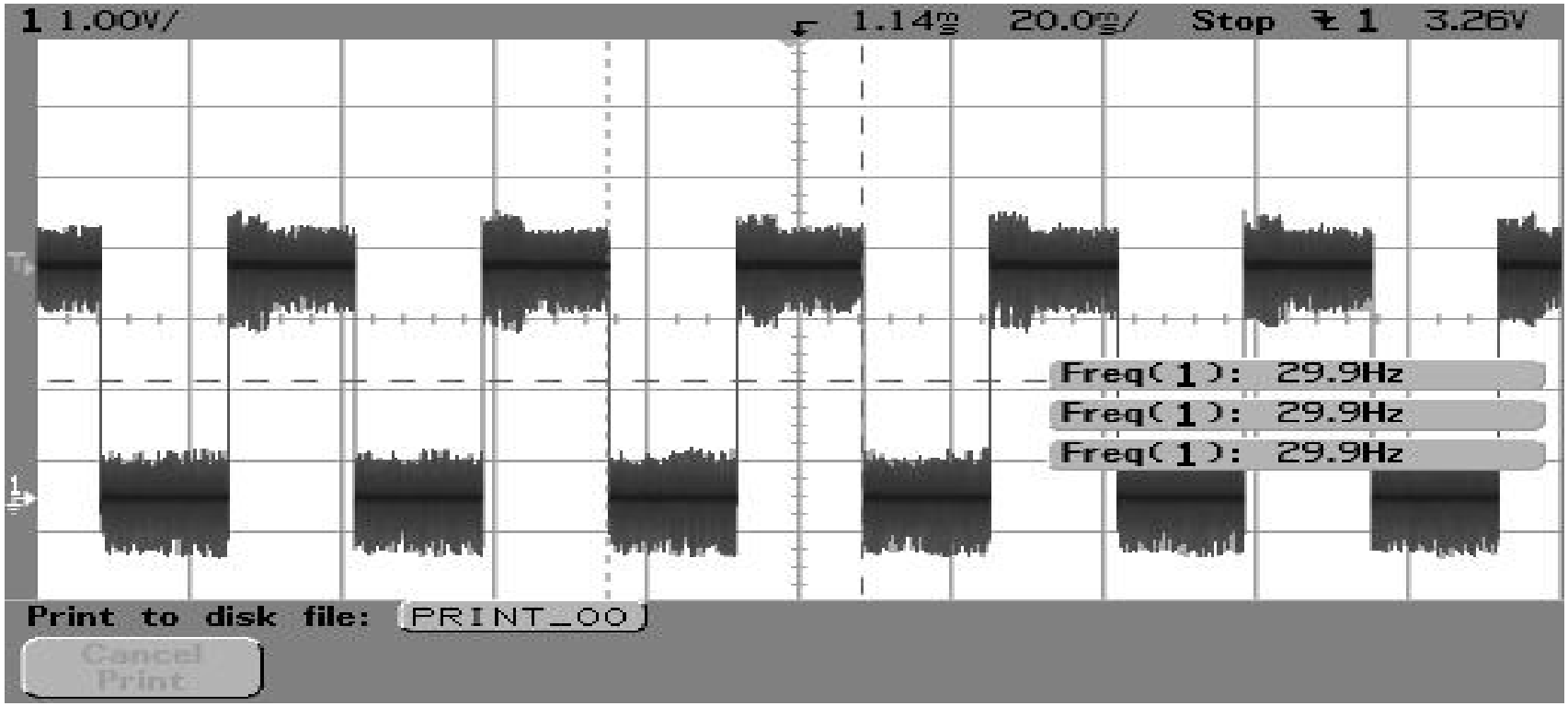


TV Encoder

DACD_CVBS signal from L4A1#1



TV Encoder (NTSC/PAL)



Signal Name		Measurement point
FIELD	30 Hz for NTSC	TV encoder#34
FIELD	25 Hz for PAL or SECAM	TC encoder#34

Network Port:

The network interface port provides a means of networking several Xbox consoles together. This network interface is implemented as a 10/100-Base T (RJ-45) Ethernet port. This port provides access to broadband internet connections such as cable modems, home networks and peer to peer networking.

The Ethernet MAC features dual speed CSMA/CD for 10 and 100 Mb/s, the MAC includes a Media Independent Interface (MII) to an external PHY. The LXT972 provides a MII for easy attachment to 10/100 Media Access Controllers (MACs).

The Xbox utilize an Integrated Ethernet RJ-45 connector with magnetics and LED indicators.

The Green LED, shall be controlled to illuminate when a network connection is established, and will blink when there is activity on the line. The Yellow LED, shall be illuminated if the connection is established at 100Mbps and shall not be illuminated if connected at 10Mbps.

If the leds are not enable during the test

Network Port:

Check

- Yellow LED pad between 3.3 and U8B1#1 (P0AC) or this LED by itself, if it is 'off' means that the ICS1893 does not have a link
- Green LED pad between GND and U8B1#4 (P2LI) or this LED by itself, if it is 'off' means that there is not a link.

For both cases :

- The P1CL / indicates that the ICS1893 detects a collisions
- The P3TD / Transmit Data
- The P4RD / Receive Data
- 10_BIAS / Low 10Base TX or 100Base TX operation selected
- REF_IN /Frequency Reference input U8B1#47
- REF_OUT/Frequency Reference output , it must be left unconnected(46pin)
- RESET / System Reset drive by the PCI_RESET line
- COL/ Collision detect U8B1#43, this signal is asserted as part of the signal quality error.
- CRS / Carrier Sense, this signal is asserted when it detects either receive or transmit activity
- MDC / Management Data Clock for synchronize the transfer of management information between the ICS1893 and the Station Management Entity.
- MDIO Management Data input/Output , All the transfers and sampling are synchronous with the signal on the MDC pin

LED Status

Definitions:
Long flash = 600ms
Short flash = 200ms
Orange = Red + Green
Off = Neither Red nor Green

Short Orange, Short Off
Thermal Overload. This state is triggered when the SMC detects an over temperature situation, or assumes an over temp situation because communication with the thermal detect IC cannot be completed:

- **CPU die temperature exceeds the maximum allowed (80C)**
- **Connection to CPU sense diode is shorted or open**
- **Missing or incorrect pull-up resistors on SMbus clock or data lines**
- **Bad EEPROM**
- **Bad TV Encoder**
- **Bad MCPX**

Short Red, Short Green
Core Digital Logic Error. This state is triggered when the CPU does not respond to the SMC query for memory check results. This can indicate one of many core issues, such as:

- **Clock generator problem (No clock to MCPX, NV2B, Spread Spectrum IC, bad POWOK signal from PSU)**
- **MCPX problem**
- **Bad Flash image**
- **Open SMI line between SMC and NV2B**
- **CPU core voltage or AGTL voltage regulator bad**

LED Status

Short Red, Short Orange

System RAM error. This state is triggered when the CPU responds to the SMC query for memory check results and reports an illegal configuration or one or more malfunctioning RAM chips.

- **No MCLK to any of the four memory banks**
- **One or more bad memory chips.**
- **Memory core (V2P5) or termination voltage regulator bad**

Long Red, Short Green

Hard Drive Error. This state indicates an error detected on the hard drive:

- **Problem with IDE interface**
- **Problem with IDE cable**
- **Problem with HDD**
- **Bad image on HDD**
- **Problem with DVD that interferes with HDD data transactions**
- **Missing cable select resistor**
- **No 5V or 12V on HDD power cable**
- **HDD power cable incorrectly installed**
- **HDD jumper settings incorrect**

LED Status

Long Green, Short Red

DVD drive Error. This state indicates an error detected on DVD drive:

- **Problem with IDE interface**
- **Problem with IDE cable**
- **Problem with DVD drive**
- **Problem with HDD that interferes with DVD data transactions**
- **DVD control cable missing or incorrectly installed.**

Short Red, Short Orange, Short Green, Short Orange

USB Power Error. This state indicates that power to one or more Controller ports is low. Possible faults include:

- **Missing or open PTC for any of the four Controller Ports**
- **Short on USB daughter card**
- **USB Daughter card incorrectly installed**
- **USB daughter card shorts against EMI shield**
- **Short in controller port connector assembly**

Short Green, Short Orange

AV Pack is not attached. This state indicates no AV pack is detected on the AVIP connector. AV Packs are detect by shorting one or more of the three VMODE pins on the AVIP connector to ground. Possible faults include:

- **Bad AVIP connector**
- **Bad AV Pack cable**
- **Missing or incorrect series resistors between AVIP VMODE pins and the SMC**
- **Missing or incorrect pull-up resistor values on AVIP VMODE pins**