JUMPERS AND STUFF

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	KEYBOARD RESET	7
JP2	BLOB	CO VS. O8 ADDRESS MAP	2
JP3	BLOB	EXPANSION RAS SELECT	3
JP4	BLOB	BYPASS 2M-BYTE DECODER	3
JP7	BLOB	EXPANSION/TICK OPTION	6,8
JP8	BLOB	LIGHT PEN PORT SELECT	5
JP9	BLOB	ON-BOARD RTC BYPASS	8
JP10	BLOB	RS232 AUDIO I/O CUTOUT	5
JP11	BLOB	TTL VS RS170 COMP SYNC	4

CONNECTORS

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	MOUSE/JOYSTICK 1	5
CN2	DB9P	MOUSE/JOYSTICK 2	5
CN3	RCA-J	RIGHT AUDIO OUTPUT	5
CN4	RCA-J	LEFT AUDIO OUTPUT	5
CN5	DB23S	EXTERNAL FLOPPY	7
CN6	DB25P	RS232 SERIAL PORT	6
CN7	DB25S	PARALLEL PRINTER PORT	6
CN8	SQ DIN	POWER SUPPLY CONNECTOR	10
CN9	DB23P	VIDEO OUTPUT	4
CN10	RCA-J	COMPOSITE VIDEO	4
CN11	DIL-34	INTERNAL FLOPPY SIGNAL	7
CN12	SIL-4	INTERNAL FLOPPY POWER	7
CN13	SIL-8	KEYBOARD CONNECTOR	7
P1	EDGE86	EXPANSION CONNECTOR	9
P9	RA-56H	MEM. EXP. MAIN-BOARD	8

REVISION HISTORY

REV	DESCRIPTION	DATE	APRVL	MANAGER
-	FOR OLDER REVISION 3/5 BOARDS			
	SEE SCHEMATIC 312511-01			
-	FOR OLDER REVISION 6A/7 BOARDS			
	SEE SCHEMATIC 312007-01			
0	PCB RB ENGINEERING PROTOTYPE	04/13/91	GRR	
1	PCB RBA ADVANCED ENGINEERING RELEASE	06/20/91	GRR	

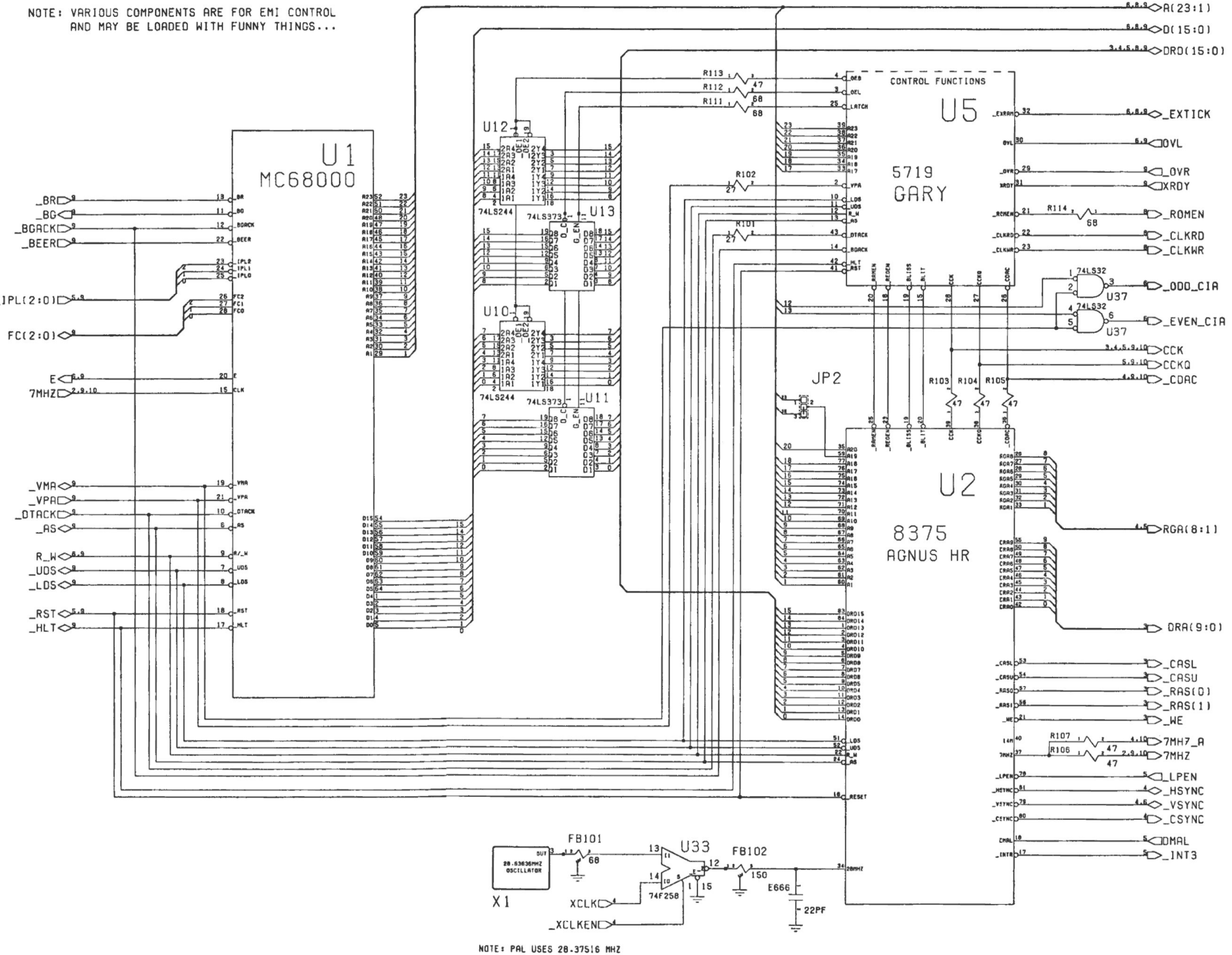
SIGNAL GLOSSARY

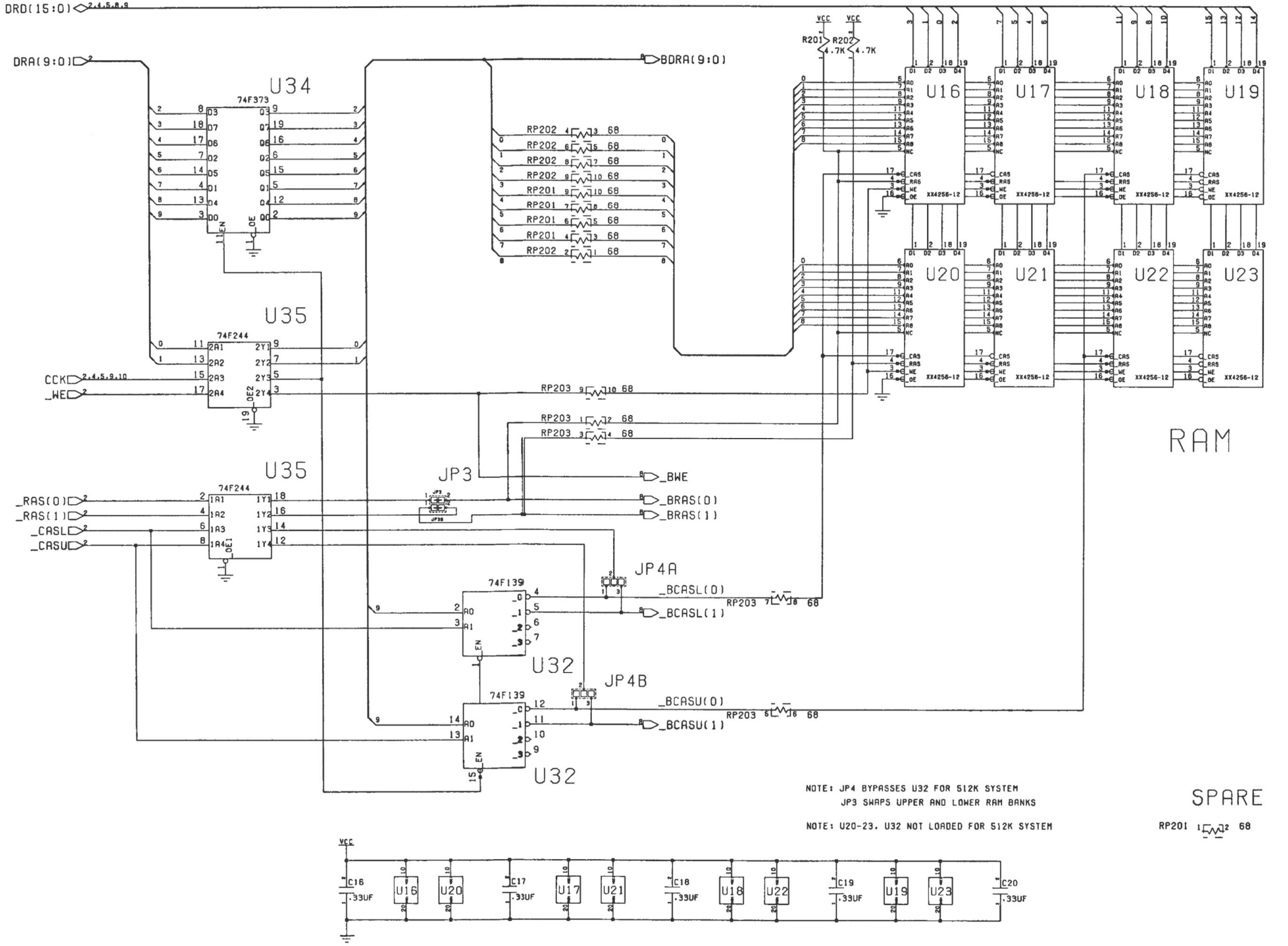
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHZ MASTER CLOCK	2
7MHZ	7.15909 MHZ PROCESSOR CLOCK	2,4,9,10
A[23:1]	PROCESSOR ADDRESS BUS (68000)	2,6,8,9
ACK	DATA ACKNOWLEDGE (PARALLEL PORT)	6
AS	ADDRESS STROBE (68000)	2,9
AUDIN	AUDIO INPUT (RS232 PORT)	5,6
AUDOUT	AUDIO OUTPUT (RS232 JACK)	5,6
BEER	BUS ERROR (68000)	2,9
BG	BUS GRANT (68000)	2,9
BGACK	BUS GRANT ACKNOWLEDGE (68000)	2,9
BLISS	BLITTER SLOWDOWN (CHIPS)	2
BLIT	CHIP MEMORY ACCESS (CHIPS)	2
BR	BUS REQUEST (68000)	2,9
BUSY	DEVICE BUSY (PARALLEL PORT)	6
CASL/U	COLUMN ADDRESS STROBE (DRAM)	2,3
CCK/CCKQ	COLOR CLOCK / QUADRATURE (CHIPS)	2-5,9,10
CDAC	7.15909 MHZ QUADRATURE CLOCK (CHIPS)	2,4,9,10
CHNG	MEDIA CHANGE (FLOPPY)	6,7
CLKRD/WR	READ-TIME CLOCK READ / WRITE (RTC)	2,8
COMP	MONOCHROME COMPOSITE VIDEO (VIDEO)	4
CSYNC	COMPOSITE SYNC (VIDEO)	2,4
CTS	CLEAR TO SEND (RS232 PORT)	6
D[15:0]	PROCESSOR DATA BUS (68000)	2,6,8,9
DIR	STEP DIRECTION (FLOPPY)	6,7
DKRD	DISK READ DATA (FLOPPY)	5,7
DKWD	DISK WRITE DATA (FLOPPY)	5,7
DKWE	DISK WRITE ENABLE (FLOPPY)	5,7
DMAL	CHIP DMA REQUEST LINE (CHIPS)	2,5
DRA[8:0]	DRAM ADDRESS BUS (DRAM)	2,3
DRD[15:0]	DRAM DATA BUS (DRAM)	2-5,8,9
DSR	DATA SET READY (RS232 PORT)	6
DTACK	DATA TRANSFER ACKNOWLEDGE (68000)	2,9
DTR	DATA TERMINAL READY (RS232 PORT)	6
E	PERIPHERAL ENABLE CLOCK (68000)	2,6,9
EXTICK	EXPANSION PRESENT / RTC TICK	2,6,8,9
FC[2:0]	FUNCTION CODE (68000)	2,9
FIRE0/1	FIRE BUTTON 0/1 (JOYSTICKS)	5,6
HLT	PROCESSOR HALT (68000)	2,9
HSYNC	HORIZONTAL SYNC (VIDEO)	2,4,6
INDEX	INDEX PULSE (FLOPPY)	6,7
INT[2,3,6]	INTERRUPT REQUEST (CHIPS)	2,5,6,9
IORESET	I/O RESET	6,7,9
IPL[2:0]	INTERRUPT PRIORITY LEVEL (68000)	2,5,9
KBCLOCK	KEYBOARD CLOCK (KEYBOARD)	6,7
KBDATA	KEYBOARD DATA (KEYBOARD)	6,7
KBRESET	KEYBOARD RESET (KEYBOARD)	7
LDS/UDS	UPPER / LOWER DATA STROBES (68000)	2,9
LED	POWER ON LED / AUDIO FILTER DISABLE	5,6,7
LEFT/RIGHT	LEFT RIGHT AUDIO (AUDIO)	5

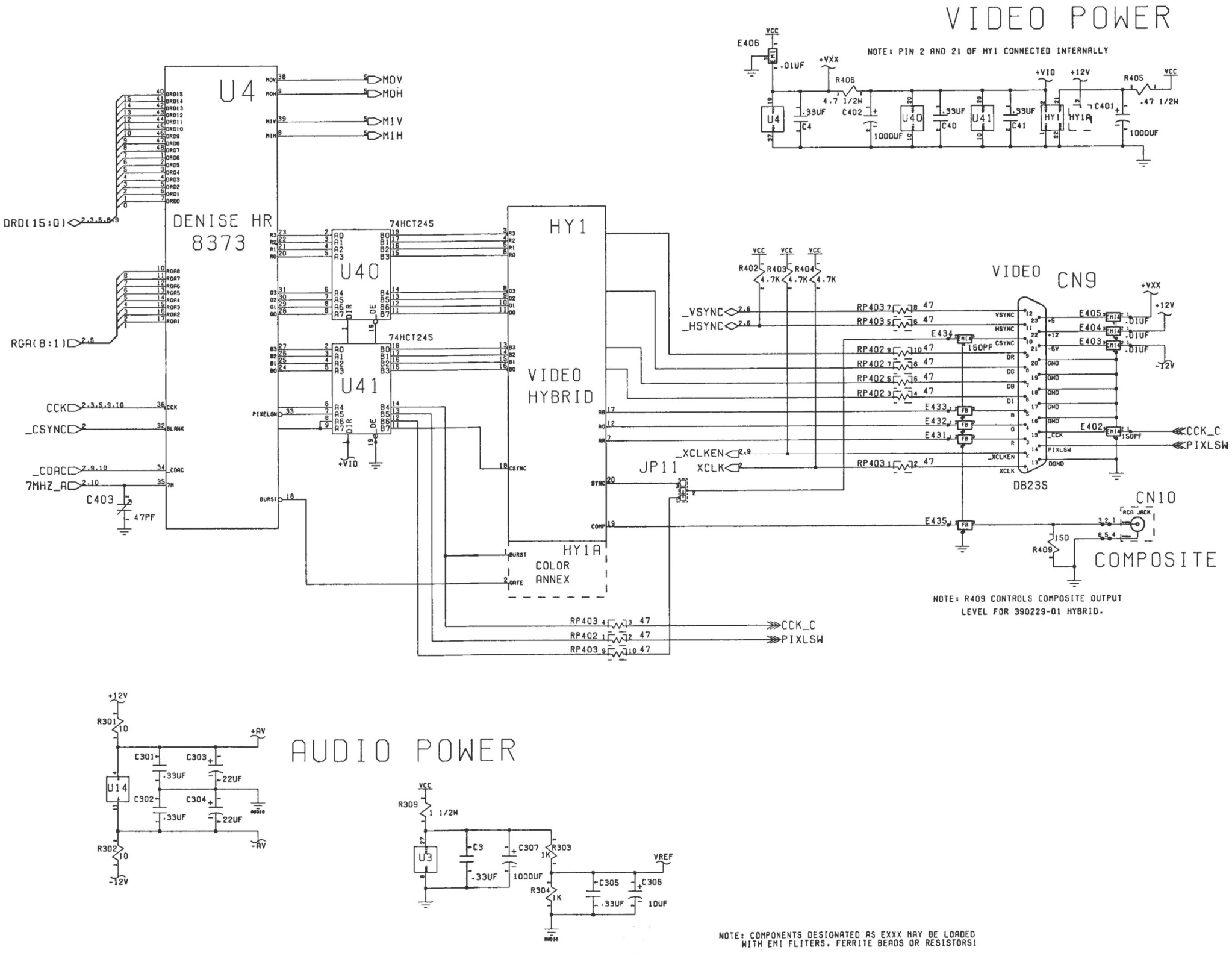
SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	LIGHT PEN TRIGGER (JOYSTICKS)	2,5
MTR	MOTOR ON (FLOPPY)	6,7
MTRQ	MOTOR ON - DRIVE Q (FLOPPY)	7
MOV/MOH	MOUSE 0 QUADRATURE V/H (JOYSTICKS)	4,5
M1V/M1H	MOUSE 1 QUADRATURE V/H (JOYSTICKS)	4,5
OVL	OVERLAY ROM OVER RAM	2,6,9
OVR	OVERRIDE SYSTEM DECODING	2,9
PIXELSW	GENLOCK PIXEL SWITCH (VIDEO)	4
POT0X/0Y	POT LINES 0 X/Y (JOYSTICKS)	5
POT1X/1Y	POT LINES 1 X/Y (JOYSTICKS)	5
POUT	PAPER OUT (PARALLEL PORT)	6
PPD[7:0]	PARALLEL PORT DATA (PARALLEL PORT)	6
RAMEN	RAM ENABLE (CHIPS)	2
REGEN	CHIP REGISTER ENABLE (CHIPS)	2
RAS0/1	ROW ADDRESS STROBE (DRAM)	2,3
RDY	DRIVE READY (FLOPPY)	6,7
RESET	GENERAL RESET	6,9
RGA[8:1]	REGISTER ADDRESS BUS (CHIPS)	2,4,5
R/G/B	RED / GREEN / BLUE (VIDEO)	4
RI	RING INDICATE (RS232 PORT)	6
ROMEN	ROM ENABLE (ROM)	2,8
RTS	REQUEST TO SEND (RS232 PORT)	6
RST	PROCESSOR RESET (68000)	2,5,9
RXD	RECEIVE DATA (RS232 PORT)	5,6
RW	PROCESSOR READ/WRITE (68000)	2,6,9
SEL	SELECT (PARALLEL PORT)	6
SEL[3:0]	DRIVE SELECT (FLOPPY)	6,7
SIDE	SIDE SELECT (FLOPPY)	6,7
STEP	STEP IN/OUT COMMAND (FLOPPY)	6,7
TRK0	TRACK ZERO SENSE (FLOPPY)	6,7
TXD	TRANSMIT DATA (RS232 PORT)	5,6
VMA	VALID MEMORY ADDRESS (68000)	2,9
VPA	VALID PERIPHERAL ADDRESS (68000)	2,9
VSYNC	VERTICAL SYNC (VIDEO)	2,4,6
WE	WRITE ENABLE (DRAM)	2,3
WPROT	WRITE PROTECT SENSE (FLOPPY)	6,7
XCLK	EXTERNAL GENLOCK CLOCK (VIDEO)	2,4
XCLKEN	EXTERNAL CLOCK ENABLE (VIDEO)	2,4,9
XRDY	EXTERNAL DATA READY	2,9

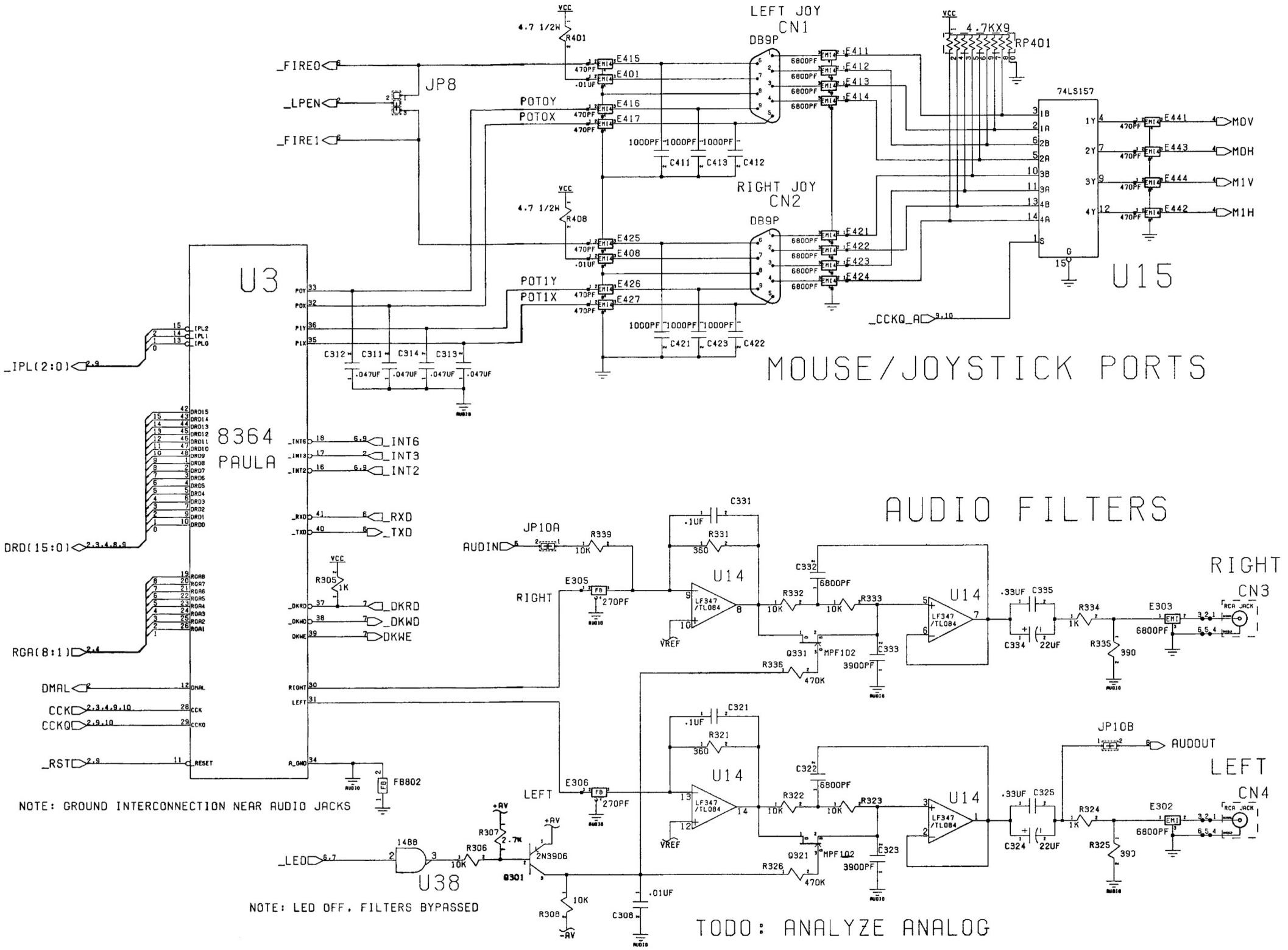
KEY COMPONENTS

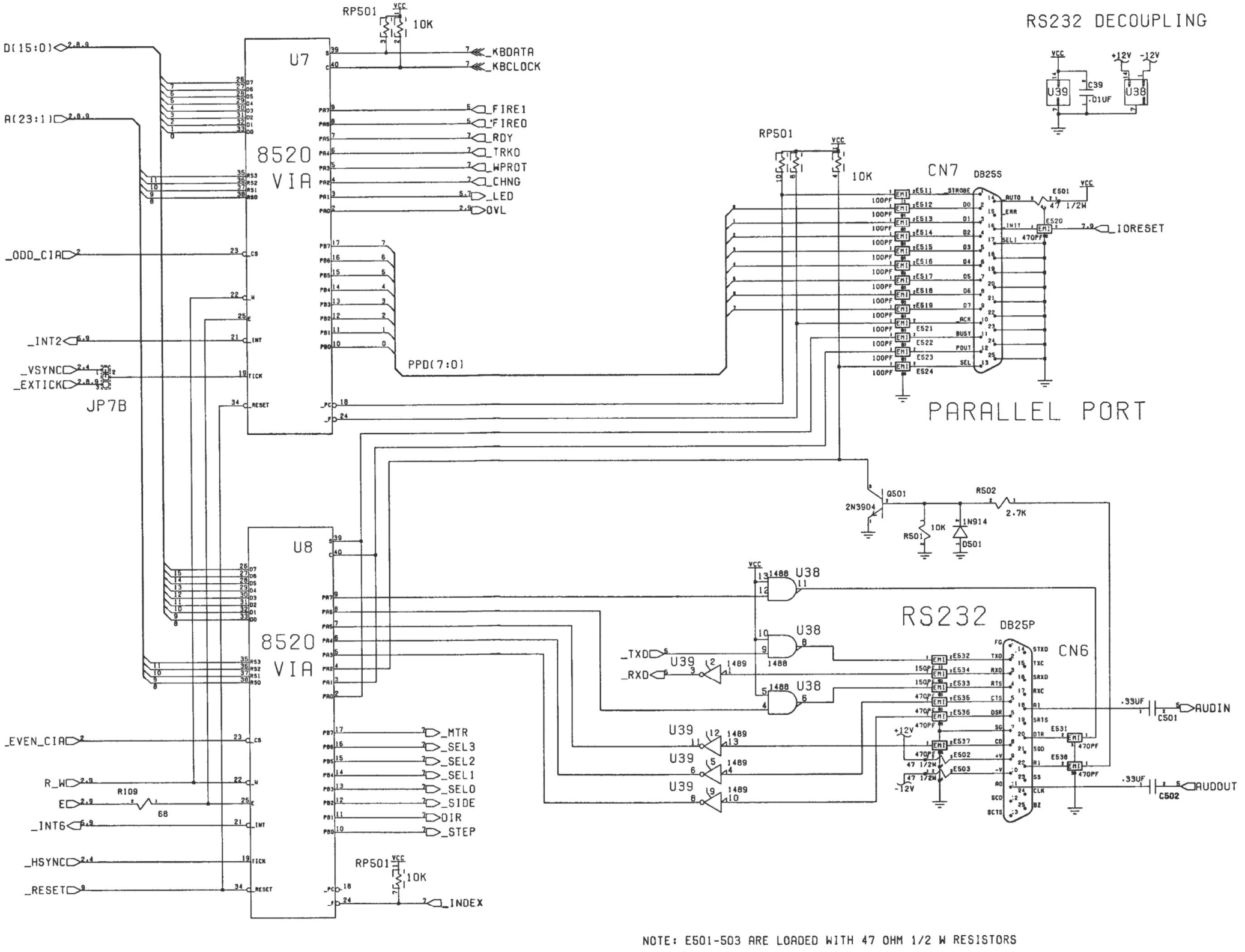
REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 PROCESSOR, 8MHZ	2
U2	8375	AGNUS HR	2
U3	8364	PAULA	5
U4	8373	DENISE HR	4
	8362	DENISE	OBS
U5	5719	GARY	2,7
U6	ASST	ROM 256KX16, 200 NS	8
U7-8	8520	AMIGA VIA, 1 MHZ	6
U9	6242	REAL TIME CLOCK	8
U14	LF347	BIMOS OP-AMP	5
	TL084	BIMOS OP-AMP	ALT
U38	1488	EIA LINE DRIVER	6
U39	1489	EIA LINE RECEIVER	6
U42	NE555	TIMER	7
U16-19	ASST	DRAM 256KX4, 120 NS	3
U20-23	ASST	DRAM 256KX4, 120 NS	3
X1	OSC	TTL 28.63636 MHZ NTSC	2
	OSC	TTL 28.37512 MHZ PAL	ALT
HY1	ASST	VIDEO HYBRID	4


NOTE: VARIOUS COMPONENTS ARE FOR EMI CONTROL
AND MAY BE LOADED WITH FUNNY THINGS...
U1
MC68000
U2
8375
AGNUS HR
U5
5719
GARY
CONTROL FUNCTIONS
U10
U11
U12
U13
74LS244
74LS373
U37
74LS32
JP2
U33
74F258
X1
28.63636MHZ
OSCILLATOR
NOTE: PAL USES 28.37516 MHZ

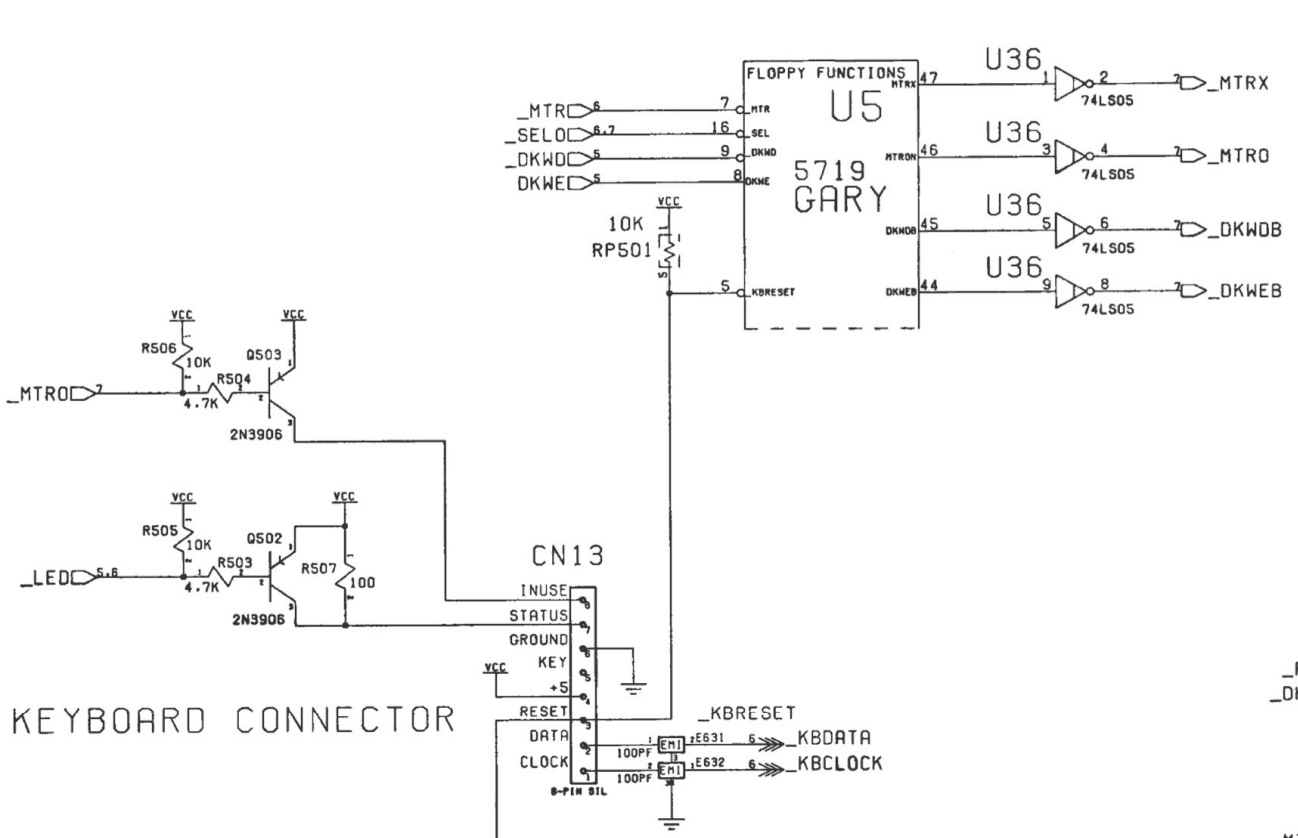

DRD(15:0)
DRA(9:0)
BDRA(9:0)
U34
74F373
U35
74F244
U35
74F244
CCK
_WE
_RAS(0)
_RAS(1)
_CASL
_CASU
JP3
JP4A
JP4B
74F139
U32
74F139
U32
R201 4.7K
R202 4.7K
RP202 68
RP201 68
RP203 68
U16
U17
U18
U19
U20
U21
U22
U23
XX4256-12
_BWE
_BRAS(0)
_BRAS(1)
_BCASL(0)
_BCASL(1)
_BCASU(0)
_BCASU(1)
RAM
SPARE
RP201 68
NOTE: JP4 BYPASSES U32 FOR 512K SYSTEM
JP3 SWAPS UPPER AND LOWER RAM BANKS
NOTE: U20-23, U32 NOT LOADED FOR 512K SYSTEM
VCC
C16 .33UF
C17 .33UF
C18 .33UF
C19 .33UF
C20 .33UF


VIDEO POWER
NOTE: PIN 2 AND 21 OF HY1 CONNECTED INTERNALLY
E406
.01UF
+VXX
R406
4.7 1/2W
C402
1000UF
U4
U40
U41
.33UF
C4
C40
C41
+VID
+12V
HY1
HY1A
C401
R405
.47 1/2W
U4
DENISE HR
8373
DRD(15:0)
RGA(8:1)
CCK
_CSYNC
_CDAC
7MHZ_A
C403
47PF
MOV
MOH
M1V
M1H
74HCT245
U40
U41
PIXELSW
BURST
+VID
CSYNC
HY1
VIDEO
HYBRID
HY1A
COLOR
ANNEX
_VSYNC
_HSYNC
R402
R403
R404
4.7K
JP11
_XCLKEN
XCLK
RP403
RP402
47
VIDEO
CN9
DB23S
E434
150PF
E433
E432
E431
E435
FB
E405
E404
E403
E402
.01UF
-6V
-12V
CCK_C
PIXLSW
CN10
RCA JACK
COMPOSITE
R409
150
NOTE: R409 CONTROLS COMPOSITE OUTPUT
LEVEL FOR 390229-01 HYBRID.
AUDIO POWER
+12V
R301
10
+AV
-AV
-12V
C301
C302
C303
C304
.33UF
22UF
U14
R302
R309
1 1/2W
U3
C3
C307
1000UF
R303
1K
R304
VREF
C305
C306
10UF
NOTE: COMPONENTS DESIGNATED AS EXXX MAY BE LOADED
WITH EMI FLITERS, FERRITE BEADS OR RESISTORS!

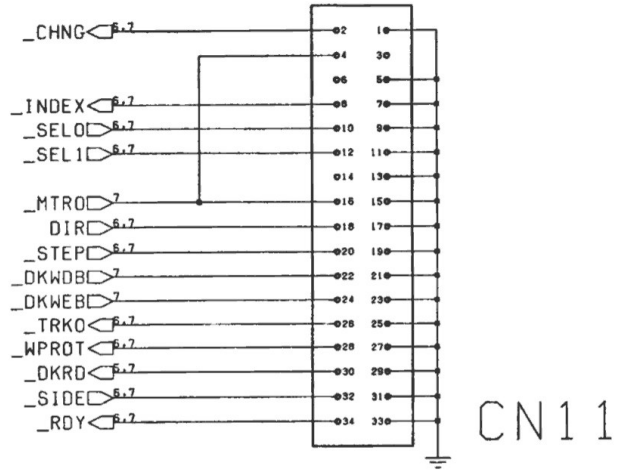

LEFT JOY
CN1
DB9P
RIGHT JOY
CN2
DB9P
4.7 1/2W
R401
R408
4.7KX9
RP401
74LS157
U15
JP8
_FIRE0
_LPEN
_FIRE1
POT0Y
POT0X
POT1Y
POT1X
_CCKQ_A
MOV
MOH
M1V
M1H
MOUSE/JOYSTICK PORTS
U3
8364
PAULA
_IPL(2:0)
DRD(15:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
_RXD
_TXD
_DKRD
_DKWD
DKWE
RIGHT
LEFT
A_GND
FB802
NOTE: GROUND INTERCONNECTION NEAR AUDIO JACKS
AUDIO FILTERS
JP10A
AUDIN
R339
10K
C331
.1UF
R331
360
U14
LF347
/TL084
VREF
C332
6800PF
R332
10K
R333
10K
Q331
MPF102
C333
3900PF
R336
470K
E305
270PF
C335
.33UF
C334
22UF
R334
1K
R335
390
E303
6800PF
RIGHT
CN3
RCA JACK
JP10B
AUDOUT
LEFT
CN4
C321
.1UF
R321
360
C322
6800PF
R322
10K
R323
10K
Q321
MPF102
C323
3900PF
R326
470K
E306
270PF
C325
.33UF
C324
22UF
R324
1K
R325
390
E302
6800PF
U38
1488
_LED
R306
10K
R307
2.7K
2N3906
Q301
R308
10K
C308
.01UF
+AV
-AV
NOTE: LED OFF, FILTERS BYPASSED
TODO: ANALYZE ANALOG


RS232 DECOUPLING
PARALLEL PORT
RS232
8520 VIA
U7
U8
CN7 DB25S
CN6 DB25P
RP501
10K
PPD(7:0)
JP7B
Q501
2N3904
R502
2.7K
R501
10K
D501
1N914
R109
68
C39
.01UF
.33UF
C501
C502
AUDIN
AUDOUT
IORESET
_KBDATA
_KBCLOCK
_FIRE1
_FIRE0
_RDY
_TRKO
_WPROT
_CHNG
_LED
_OVL
_MTR
_SEL3
_SEL2
_SEL1
_SEL0
_SIDE
_DIR
_STEP
_INDEX
_TXD
_RXD
_ODD_CIA
_EVEN_CIA
_INT2
_INT6
_VSYNC
_EXTICK
_HSYNC
_RESET
R_W
E
D(15:0)
A(23:1)
+12V
-12V
VCC
NOTE: E501-503 ARE LOADED WITH 47 OHM 1/2 W RESISTORS

FLOPPY LOGIC

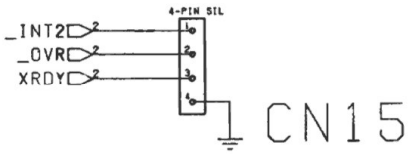


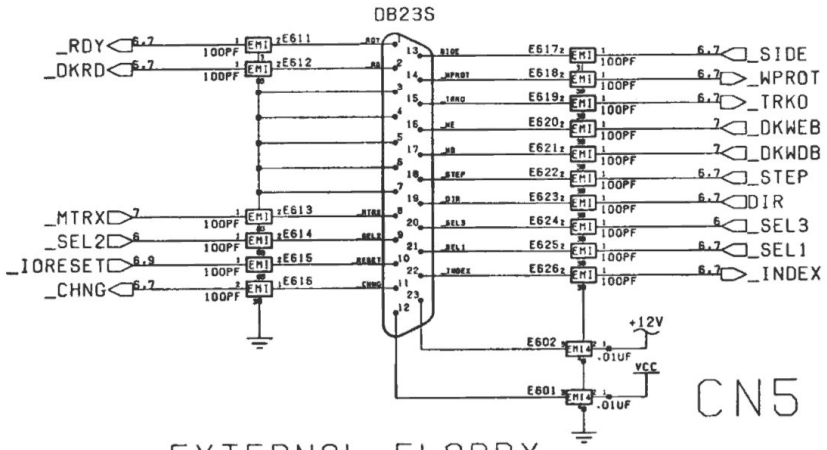
KEYBOARD CONNECTOR



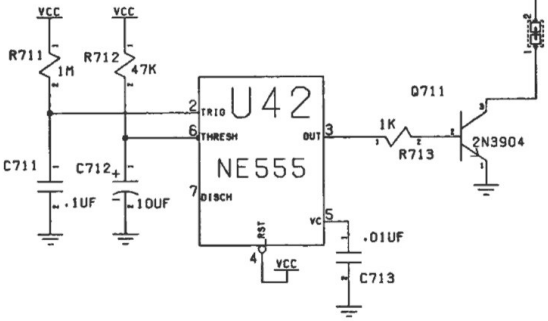
INTERNAL FLOPPY

IDE I/F



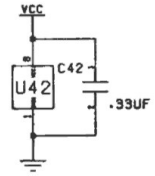


EXTERNAL FLOPPY



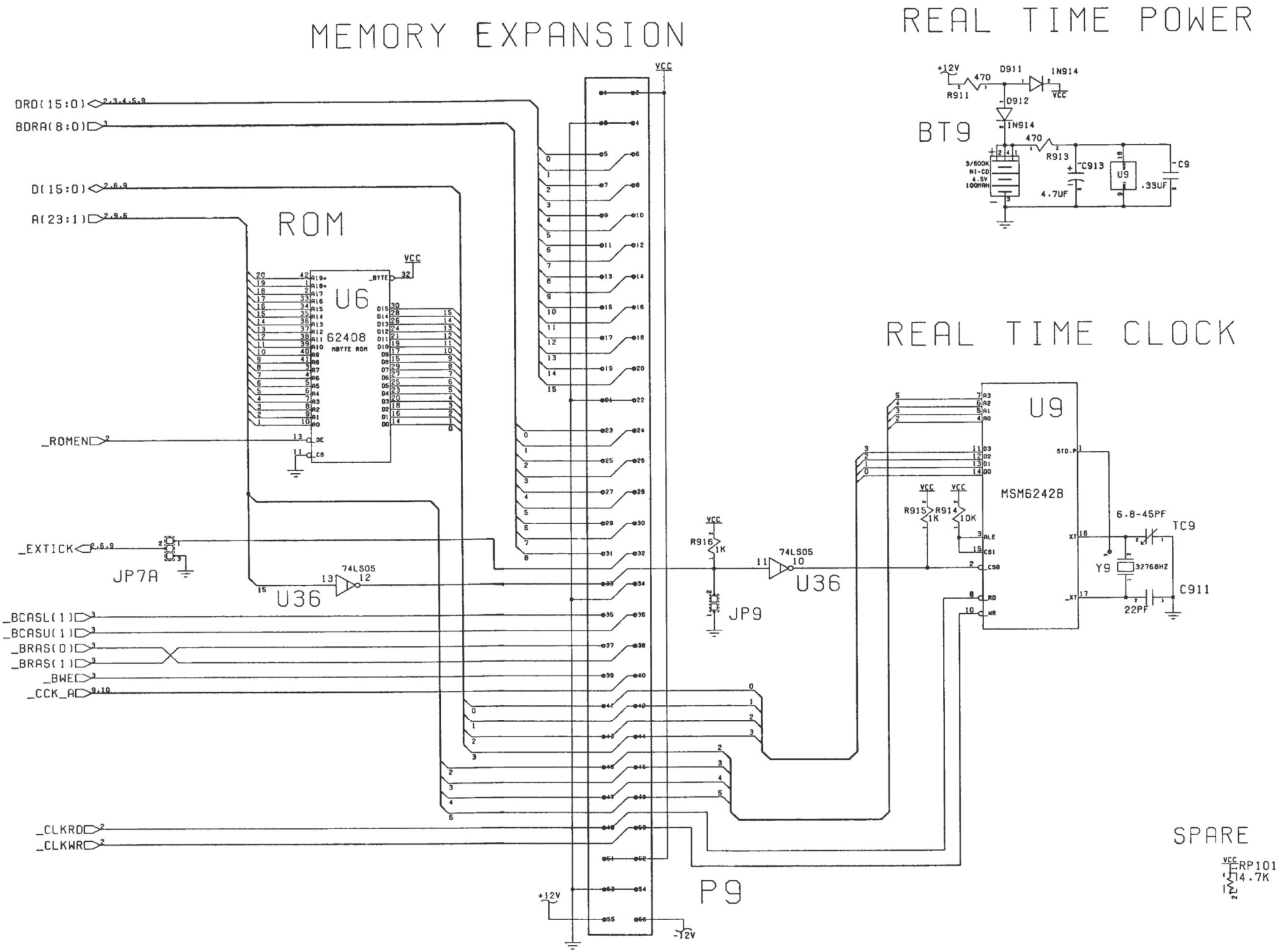
POWER UP RESET

IDE POWER FLOPPY POWER

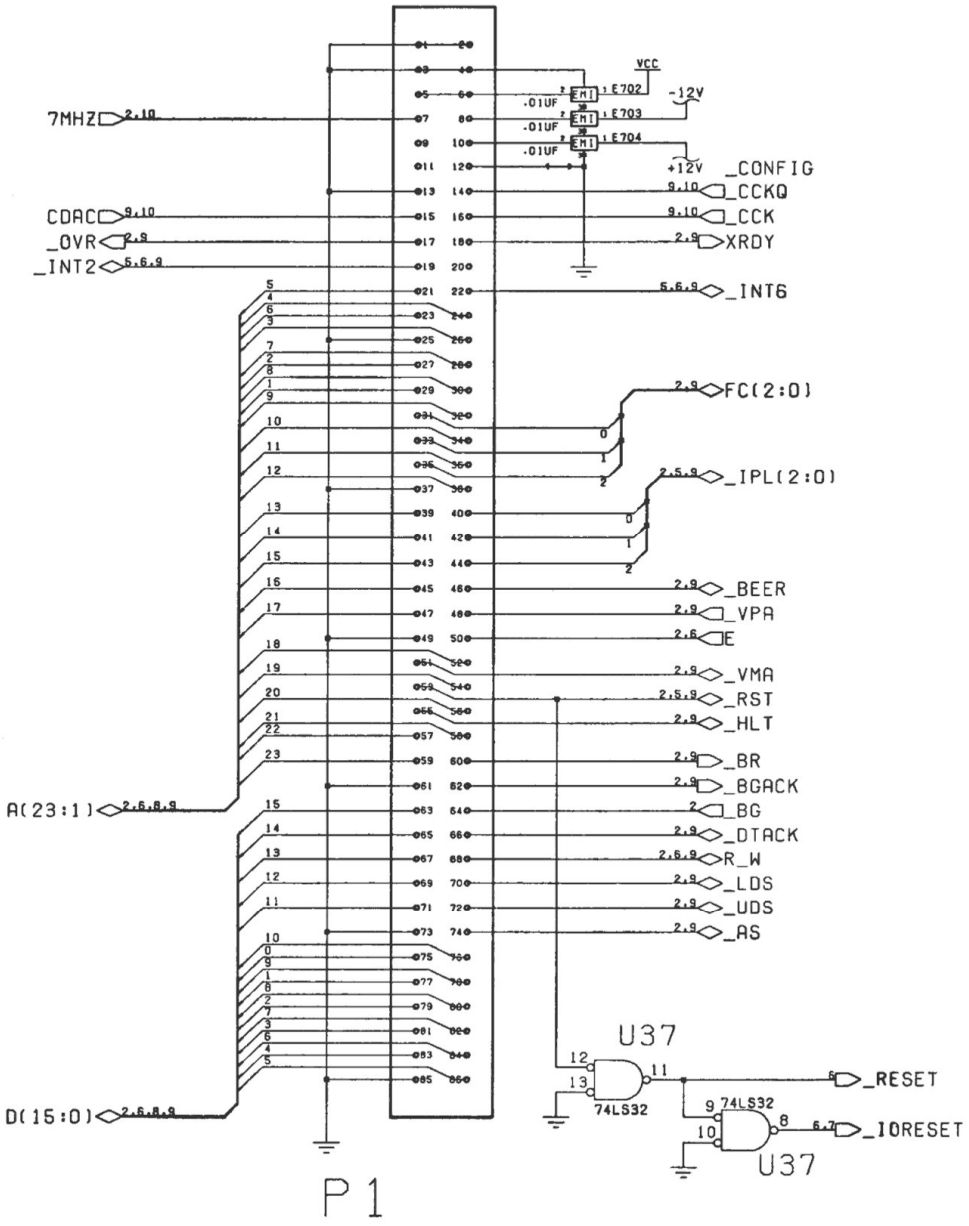


DECOUPLING

NOTE: SOME DRIVES ARE +5 ONLY...

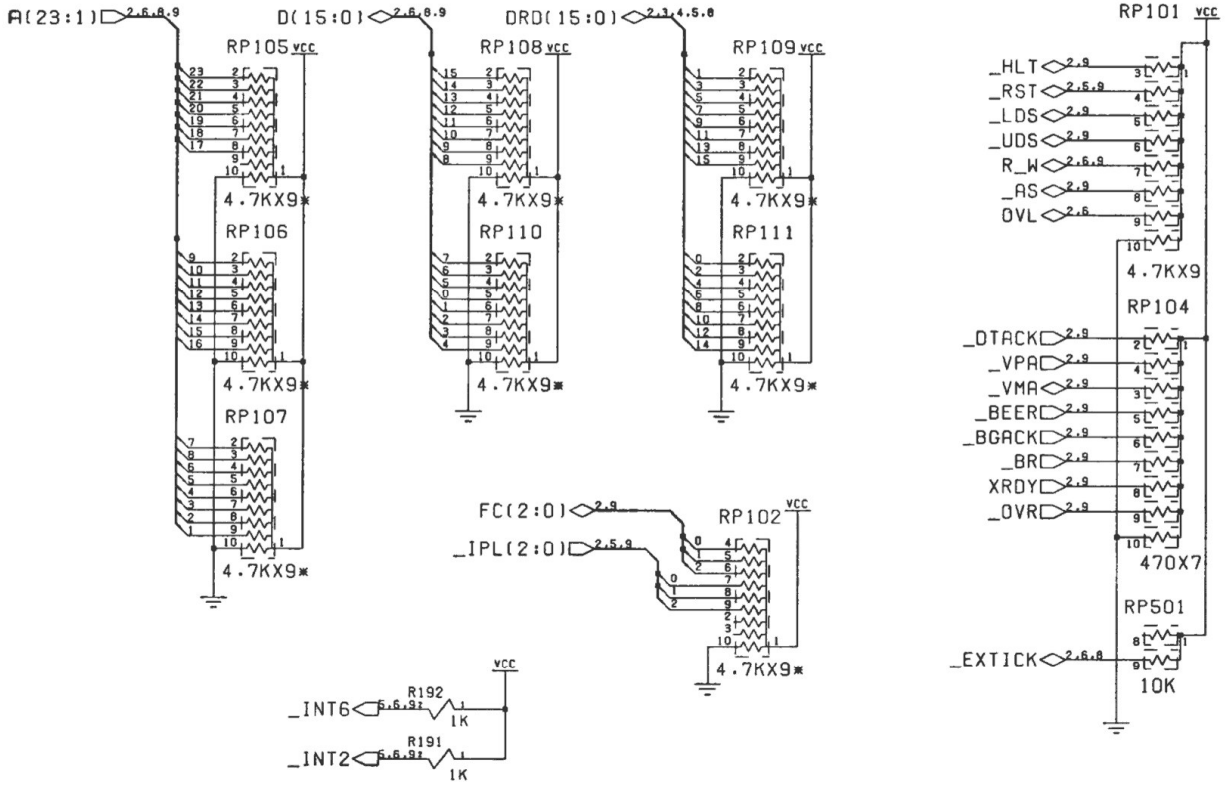

MEMORY EXPANSION
REAL TIME POWER
REAL TIME CLOCK
ROM
U6
62408
8BYTE ROM
U9
MSM6242B
U36
74LS05
JP7A
JP9
P9
BT9
3/600K
NI-CD
4.5V
100MAH
R911
470
D911
1N914
D912
R913
C913
4.7UF
.33UF
C9
R914
10K
R915
1K
R916
6.8-45PF
TC9
Y9
32768HZ
C911
22PF
SPARE
RP101
4.7K
DRD(15:0)
BDRA(8:0)
D(15:0)
A(23:1)
_ROMEN
_EXTICK
_BCASL(1)
_BCASU(1)
_BRAS(0)
_BRAS(1)
_BWE
_CCK_A
_CLKRD
_CLKWR
VCC
+12V
-12V
NOTE: ONLY 4/8 M-BIT ROM USES PIN 1 AND 42

EXPANSION BUS

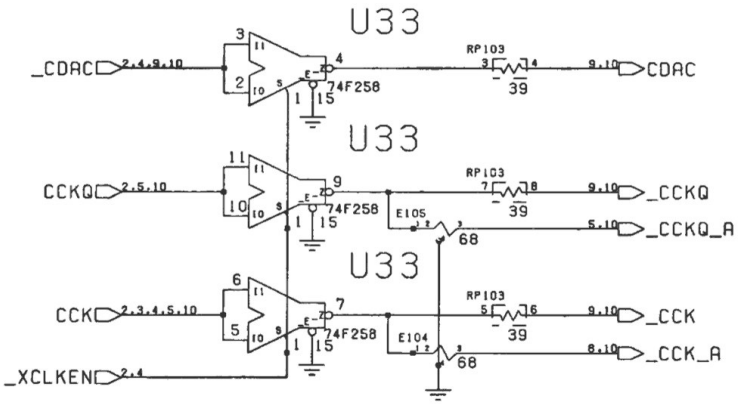


BUFFERED RESETS

EXPANSION BUS TERMINATION AND PULLUPS

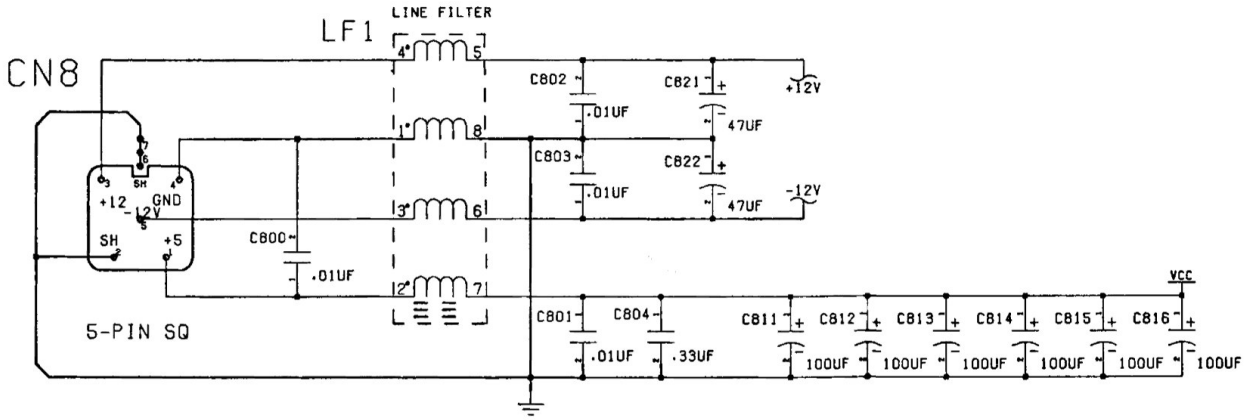


CLOCK DISTRIBUTION



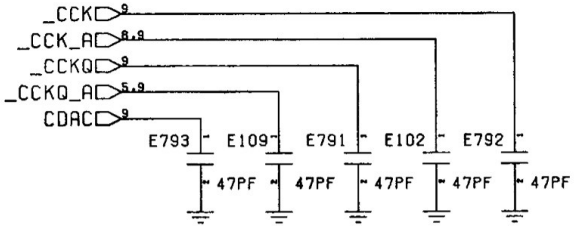
NOTE: RP105-RP111 ARE OPTIONAL INTERNAL BUS TERMINATION, AND ARE NOT NORMALLY LOADED.

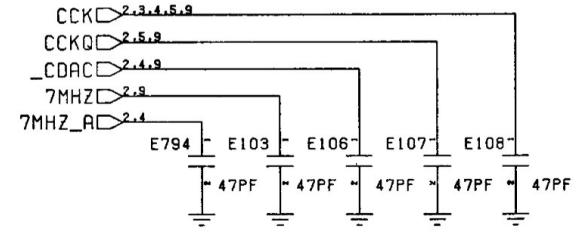
POWER INPUT

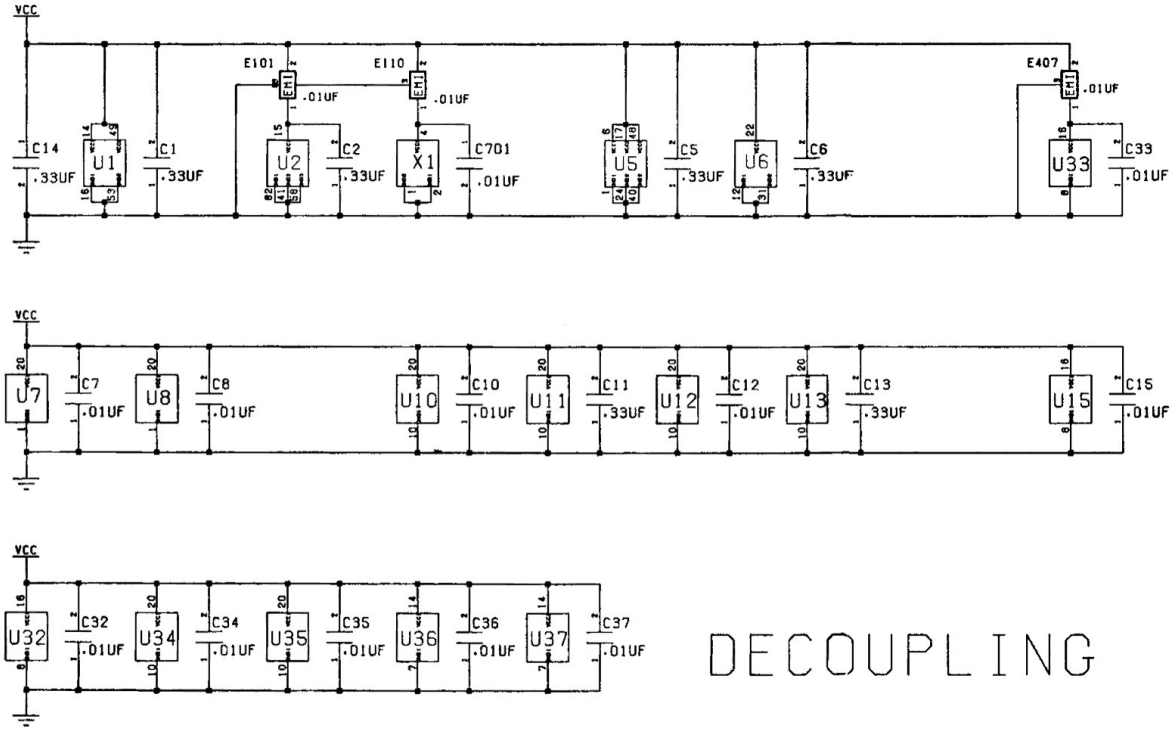


NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION

FCC GOOBERS

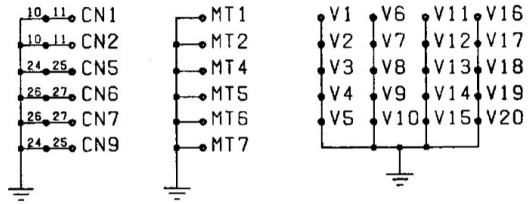




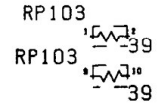


DECOUPLING

GROUNDED HOLES, &C.



SPARES



JUMPERS AND STUFF

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	MEMORY EXPANSION SENSE	3
JP2	BLOB	REFRESH KLUDGE BYPASS	2
JP3	BLOB	EXPANSION RAS SELECT	2
JP9	BLOB	RTC SELECT DISABLE	3

CONNECTORS

REF	TYPE	DESCRIPTION	PAGE
J9	56-RAFH	MEM. EXP. MAIN-BOARD	3

REVISION HISTORY

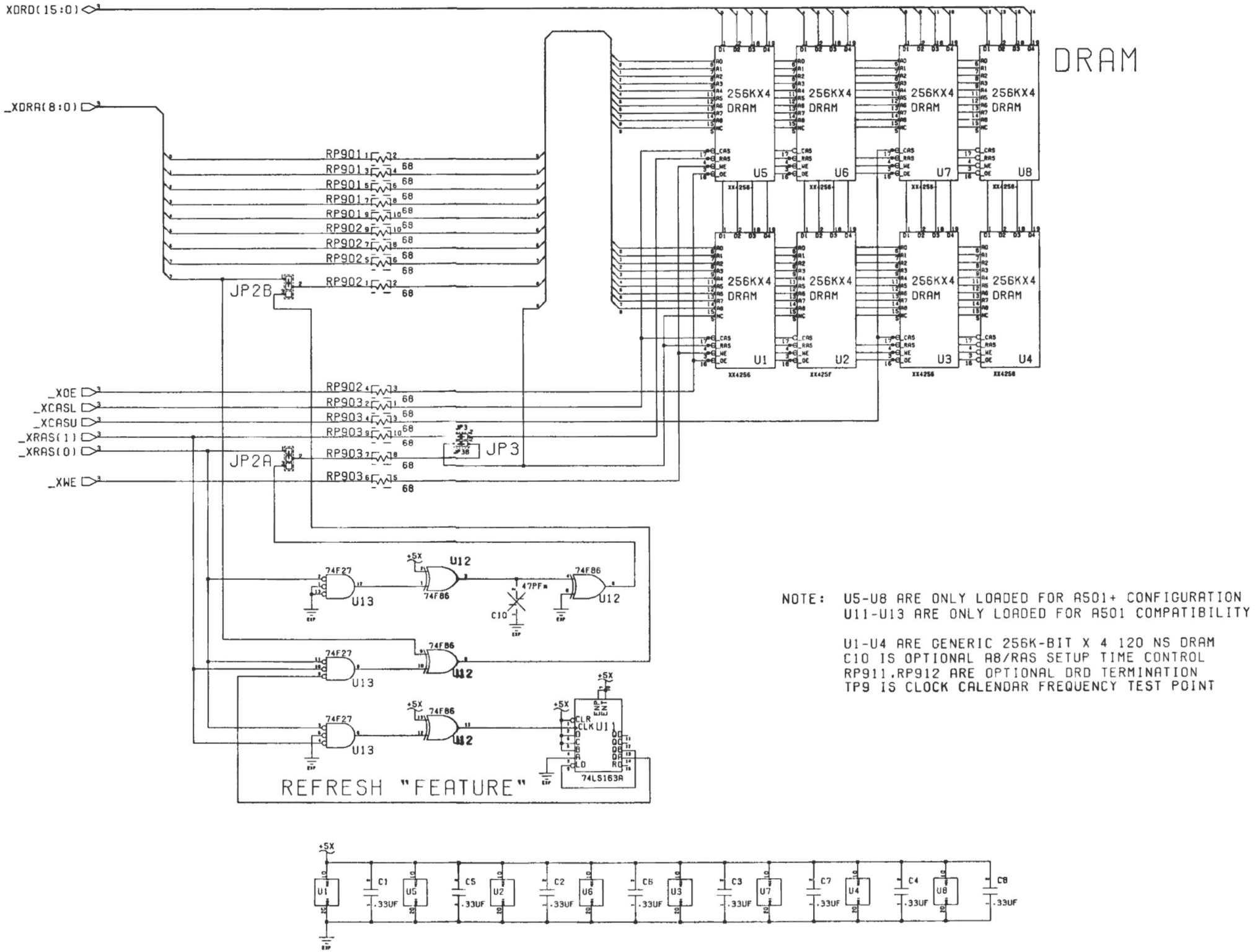
REV	DESCRIPTION	DATE	APRVL	MANAGER
-	FOR OLDER REVISION 3/5 BOARDS			
	SEE SCHEMATIC 312511-01			
-	FOR OLDER REVISION 6C BOARDS			
	SEE SCHEMATIC 312988-01			
0	PCB A501+ RB ENGINEERING PROTOTYPE	06/18/91	GRR	
1	ADVANCE ENGINEERING RELEASE	7/19/91	GRR	G.R.

SIGNAL GLOSSARY

SIGNAL	DESCRIPTION (AREA)	PAGES
A[23:1]	PROCESSOR ADDRESS BUS (68000)	3
D[15:0]	PROCESSOR DATA BUS (68000)	3
CASL/U	COLUMN ADDRESS STROBE (DRAM)	2,3
CCK/CCKQ	COLOR CLOCK / QUADRATURE (CHIPS)	3
CLKRD/WR	REAL TIME CLOCK READ / WRITE (RTC)	3
CLKCS	REAL TIME CLOCK CHIP SELECT (RTC)	3
DRA[8:0]	DRAM ADDRESS BUS (DRAM)	2,3
DRD[15:0]	DRAM DATA BUS (DRAM)	2,3
RASO/1	ROW ADDRESS STROBE (DRAM)	2,3

KEY COMPONENTS

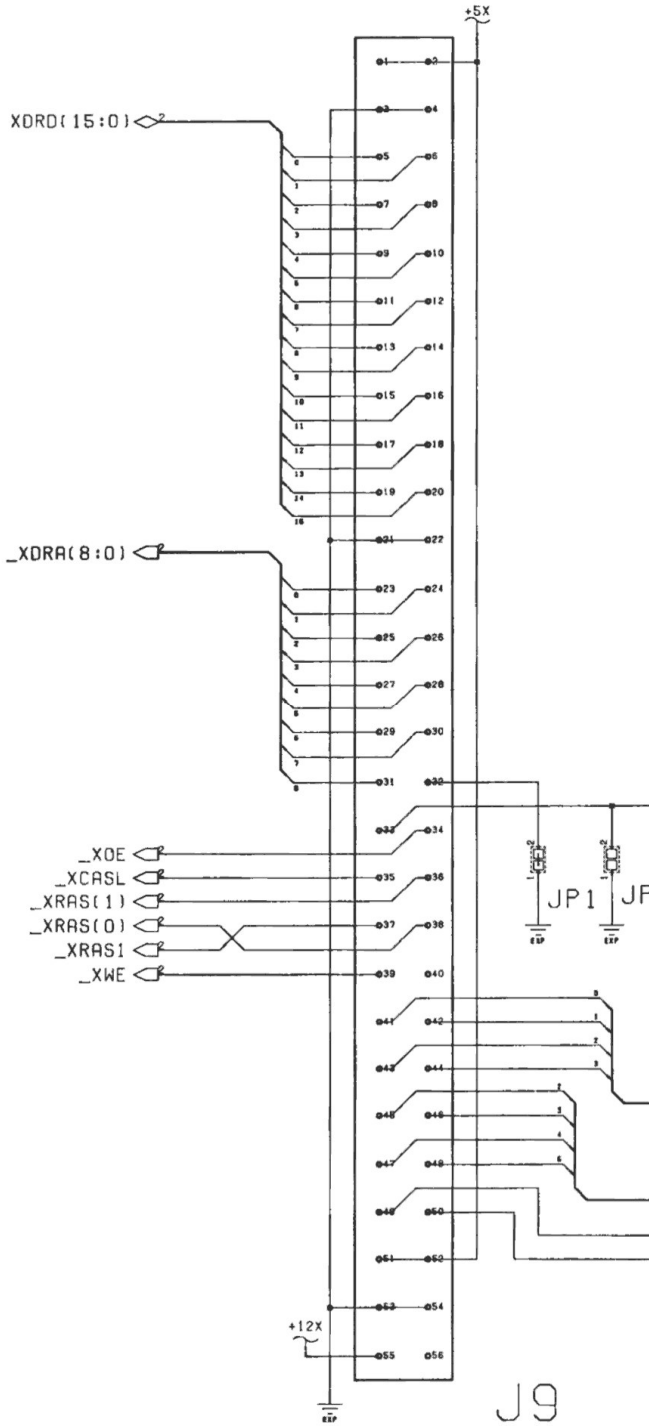
REF	CHIP	DESCRIPTION	PAGE
U1-U4	ASST	DRAM 256KX4, 120 NS	3
U5-U8	ASST	DRAM 256KX4, 120 NS	3
U9	6242	REAL TIME CLOCK	8
			5



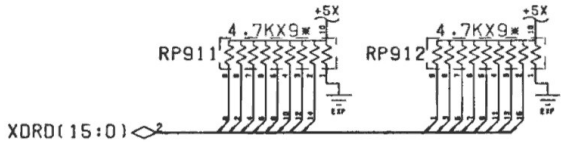
NOTE: U5-U8 ARE ONLY LOADED FOR A501+ CONFIGURATION
U11-U13 ARE ONLY LOADED FOR A501 COMPATIBILITY

U1-U4 ARE GENERIC 256K-BIT X 4 120 NS DRAM
C10 IS OPTIONAL A8/RAS SETUP TIME CONTROL
RP911,RP912 ARE OPTIONAL DRD TERMINATION
TP9 IS CLOCK CALENDAR FREQUENCY TEST POINT

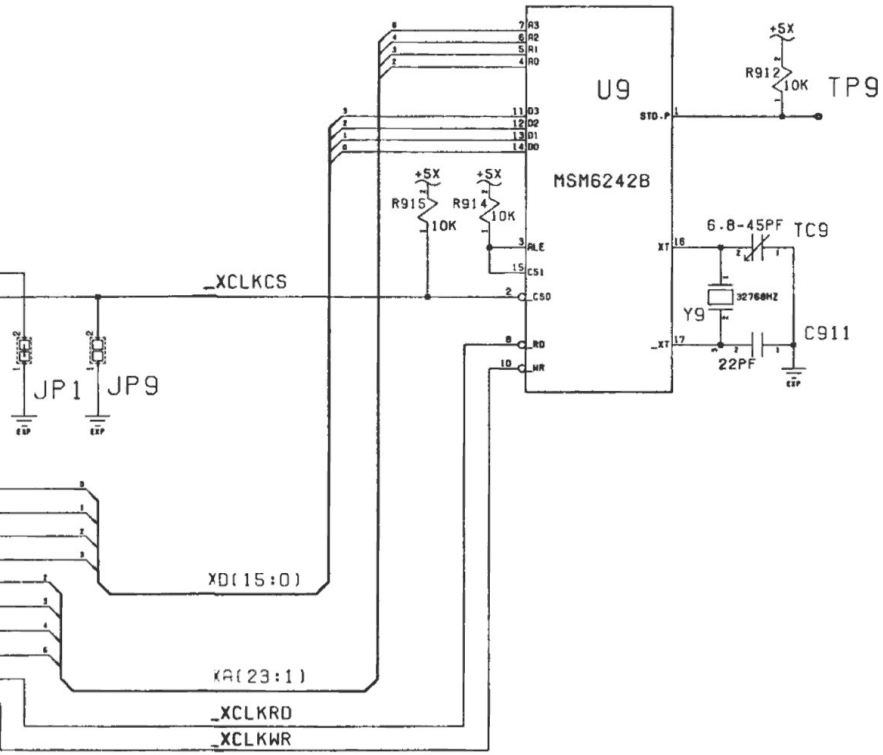
MEMORY EXPANSION



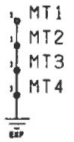
OPTIONAL TERMINATION



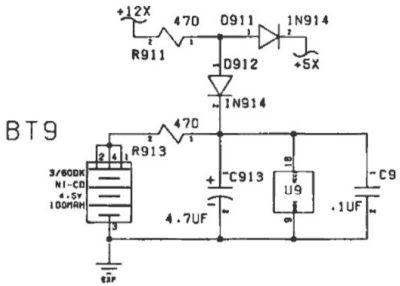
REAL TIME CLOCK



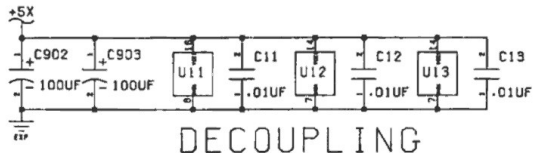
MOUNTING TABS



REAL TIME POWER



DECOUPLING



NOTE: REAL TIME CLOCK COMPONENTS ARE ONLY LOADED FOR A501 COMPATIBILITY