KINGSTON
REV 1.01
FAB G RETAIL

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[63]	MONITOR: VSOC1P8, VSOCPHY
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RULES: (APPLIED WHEN POSSIBLE)
1. MSB TO LSB IS TOP TO BOTTOM
2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5. LANED SIGNALS ARE GROUPED ON SYMBOLS
6. TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7. SUFFIX _V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8. SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10. SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12. SUFFIX _P FOR P JUNCTION
13. SUFFIX _EN FOR ENABLE
14. 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15. PWRGD FOR POWER GOOD
16. REV AND FAB ARE SET USING CUSTOM VARIABLES
TOOLS>OPTIONS>VARIABLES

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DRAWING
Mon Jan 18 12:03:57 2016

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	1/72	1/72	G	1.01

SOC:PCIEX,CLOCKS,VIDEO

NOTES:
1.TO SUPPORT A PCIE WIFI INTERFACE (J3C1), POPULATE C6P6 AND C6P7
2.SEE PAGE 32 FOR 100MHZ CLOCK ROUTING INFORMATION

SOC_BASE

U7E1 IC

PCIE
1 of 17

36	IN	PEX_WIFI_SOC_TP	AR19	P_UMI_RX3_P	P_UMI_TX3_P	AP20
36	IN	PEX_WIFI_SOC_TN	AR20	P_UMI_RX3_N	P_UMI_TX3_N	AP21
32	IN	PEX_ENET_SOC_TP_C	AN21	P_UMI_RX2_P	P_UMI_TX2_P	AP23
32	IN	PEX_ENET_SOC_TN_C	AN22	P_UMI_RX2_N	P_UMI_TX2_N	AP24
25	IN	PEX_L1_SB_SOC_TP_C	AV22	P_UMI_RX1_P	P_UMI_TX1_P	AU23
25	IN	PEX_L1_SB_SOC_TN_C	AV23	P_UMI_RX1_N	P_UMI_TX1_N	AU24
25	IN	PEX_L0_SB_SOC_TP_C	AT24	P_UMI_RX0_P	P_UMI_TX0_P	AV25
25	IN	PEX_L0_SB_SOC_TN_C	AT25	P_UMI_RX0_N	P_UMI_TX0_N	AV26
					P_RX_ZVDD_095	AN19
					P_TX_ZVDD_095	AN18

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P_UMI_TX3_P	AP20	PEX_SOC_WIFI_TP	OUT	36
P_UMI_TX3_N	AP21	PEX_SOC_WIFI_TN	OUT	36
P_UMI_TX2_P	AP23	PEX_SOC_ENET_TP	OUT	32
P_UMI_TX2_N	AP24	PEX_SOC_ENET_TN	OUT	32
P_UMI_TX1_P	AU23	PEX_L1_SOC_SB_TP	OUT	25
P_UMI_TX1_N	AU24	PEX_L1_SOC_SB_TN	OUT	25
P_UMI_TX0_P	AV25	PEX_L0_SOC_SB_TP	OUT	25
P_UMI_TX0_N	AV26	PEX_L0_SOC_SB_TN	OUT	25

C6P7 1 2 0.1 UF 10% 6.3 V EMPTY 402
C6P6 1 2 0.1 UF 10% 6.3 V EMPTY 402
C5T40 1 2 0.1 UF 10% 16 V XR5 402
C5T39 1 2 0.1 UF 10% 16 V XR5 402
C7E1 1 2 0.1 UF 10% 16 V XR5 402
C7E2 1 2 0.1 UF 10% 16 V XR5 402
C7E3 1 2 0.1 UF 10% 16 V XR5 402
C7E4 1 2 0.1 UF 10% 16 V XR5 402

R3T5 1 200 OHM 1% CH 402 2
R3T6 1 0 OHM 5% EMPTY 402 2
V_SOCPHY

V_SOCPHY
R4T21 1 510 OHM 5% 2 CH 402
2 IN TEST25_N
USED BY AMD FOR SOC PLL CHARACTERIZATION
2 IN TEST25_P
R4T22 1 510 OHM 5% 2 CH 402

U7E1 IC

VIDEO
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	BI	DP_CR_CLK	AP14	DP_CR_CLK
25	IN	DP_L0_SB_SOC_TP_C	AU18	DP1_RX0_P
25	IN	DP_L0_SB_SOC_TN_C	AU17	DP1_RX0_N
38	OUT	TMDS_TX_DP0	AU15	DP0_TX2_P
38	OUT	TMDS_TX_DN0	AU14	DP0_TX2_N
38	OUT	TMDS_TX_DP2	AV17	DP0_TX0_P
38	OUT	TMDS_TX_DN2	AV16	DP0_TX0_N
25	IN	DP_L1_SB_SOC_TP_C	AT19	DP1_RX1_P
25	IN	DP_L1_SB_SOC_TN_C	AT18	DP1_RX1_N
38	OUT	TMDS_TX_DP1	AT16	DP0_TX1_P
38	OUT	TMDS_TX_DN1	AT15	DP0_TX1_N
		DP_AUX_SOC_SB_TP	AT13	DP1_AUX_P
		DP_AUX_SOC_SB_TN	AT12	DP1_AUX_N
38	OUT	SOC_DDC_CLK	AR14	DP0_AUX_P
38	BI	SOC_DDC_DATA	AR13	DP0_AUX_N
38	OUT	TMDS_TX_CLKP	AV14	DP0_TX3_P
38	OUT	TMDS_TX_CLKN	AV13	DP0_TX3_N
			AP15	DP1_HPD
34	OUT	SPDIF_OUT	AP12	SPDIF_OUT
			AU12	DP0_HPD
		DP_TX_CALR	AM12	DP_TX_ZVSS
		DP_AUX_CALR	AR12	DP_AUX_ZVSS
		DP_RX_CALR	AN13	DP_RX_ZVSS

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25 IN DP_AUX_SB_SOC_TP_C — C3R25 1 2 0.1 UF 10% 16 V XR5 402
25 IN DP_AUX_SB_SOC_TN_C — C3R23 1 2 0.1 UF 10% 16 V XR5 402
25 OUT DP1_HPD
38 IN DP0_HPD
R5D15 1 100 KOHM 1% 2 CH 402
R3R6 1 0 OHM 5% 2 EMPTY 402
R3R11 1 150 OHMS 1% 2 CH 402
R3R13 1 200 OHM 1% 2 CH 402

U7E1 IC

CLOCKS
2 of 17

29	IN	SOC_NB_PEX_SS_100M_CLKP	AU26	CLKIN_NB_P
29	IN	SOC_NB_PEX_SS_100M_CLKN	AU27	CLKIN_NB_N
29	IN	SOC_SYNC_NS_100M_CLKP	AT21	DISP_CLKIN_P
29	IN	SOC_SYNC_NS_100M_CLKN	AT22	DISP_CLKIN_N
29	IN	SOC_AV_NS_100M_CLKP	AV19	AV_CLKIN_P
29	IN	SOC_AV_NS_100M_CLKN	AV20	AV_CLKIN_N
29	IN	SOC_PEX_SS_100M_CLKP	AU20	CLKIN_P
29	IN	SOC_PEX_SS_100M_CLKN	AU21	CLKIN_N
2	OUT	TEST25_P	AR23	TEST25_P
2	OUT	TEST25_N	AR22	TEST25_N

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DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X941293-001	IC	U7E1	ARLENE,TSMC,SHINKO,SPIL,AMD PENANG,TYPICAL,79W TDP+,A0,AKA ROUTE 1	ARLENE_SOC_R1
X941294-001	IC	U7E1	ARLENE,TSMC,IBIDEN,SPIL,AMD PENANG,TYPICAL,79W TDP+,A0,AKA ROUTE 2	ARLENE_SOC_R2
X941295-001	IC	U7E1	ARLENE,TSMC,UMTC,SPIL,AMD PENANG,TYPICAL,79W TDP+,A0,AKA ROUTE 3	ARLENE_SOC_R3
X941296-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FF,79W TDP+,A0	ARLENE_SOC_FF
X941297-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,FS,79W TDP+,A0	ARLENE_SOC_FS
X941298-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SF,79W TDP+,A0	ARLENE_SOC_SF
X941299-001	IC	U7E1	ARLENE,TSMC,NOT DEFINED,SPIL,AMD PENANG,SS,79W TDP+,A0	ARLENE_SOC_SS

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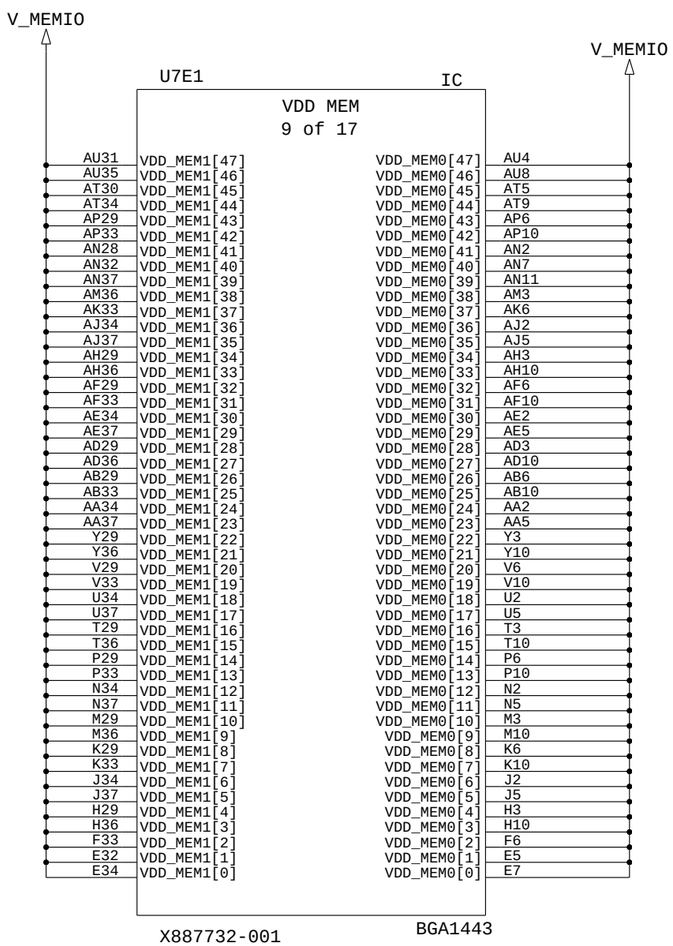
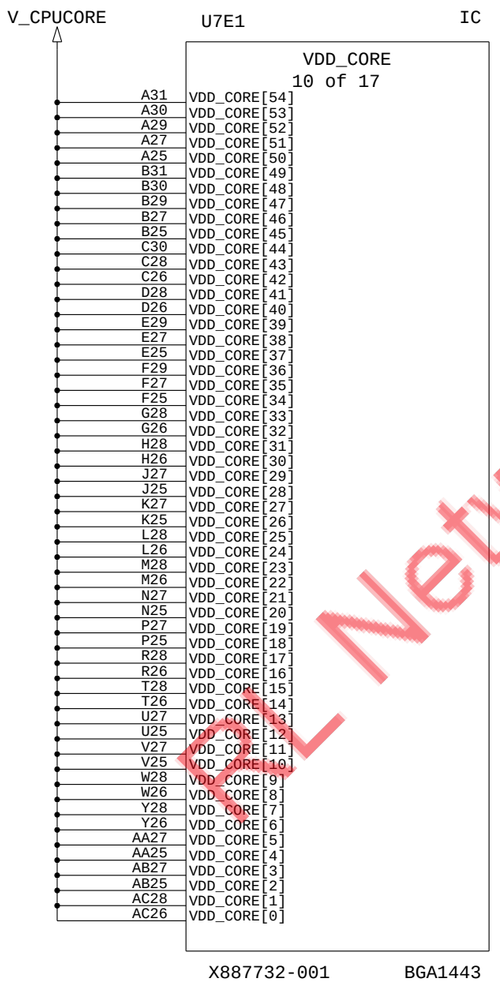
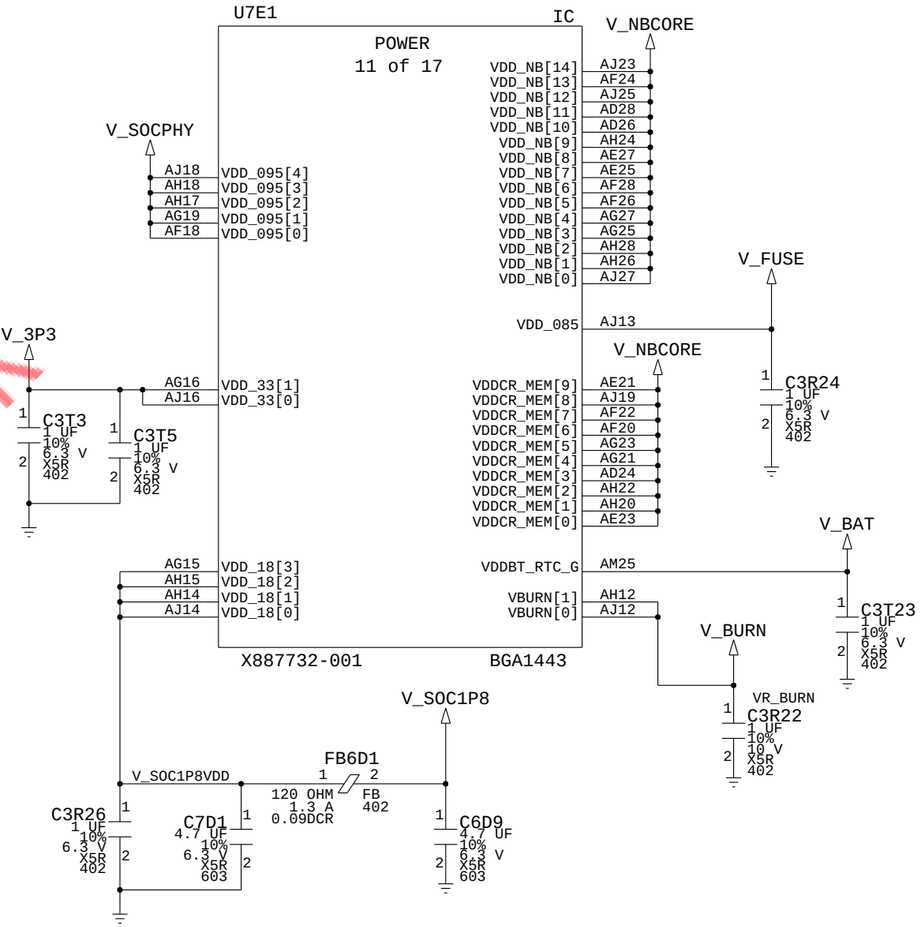
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	2/72	2/72	G	1.01

SOC: POWER: MEMIO,MEMCORE,CPUCORE,NBCORE,MISC



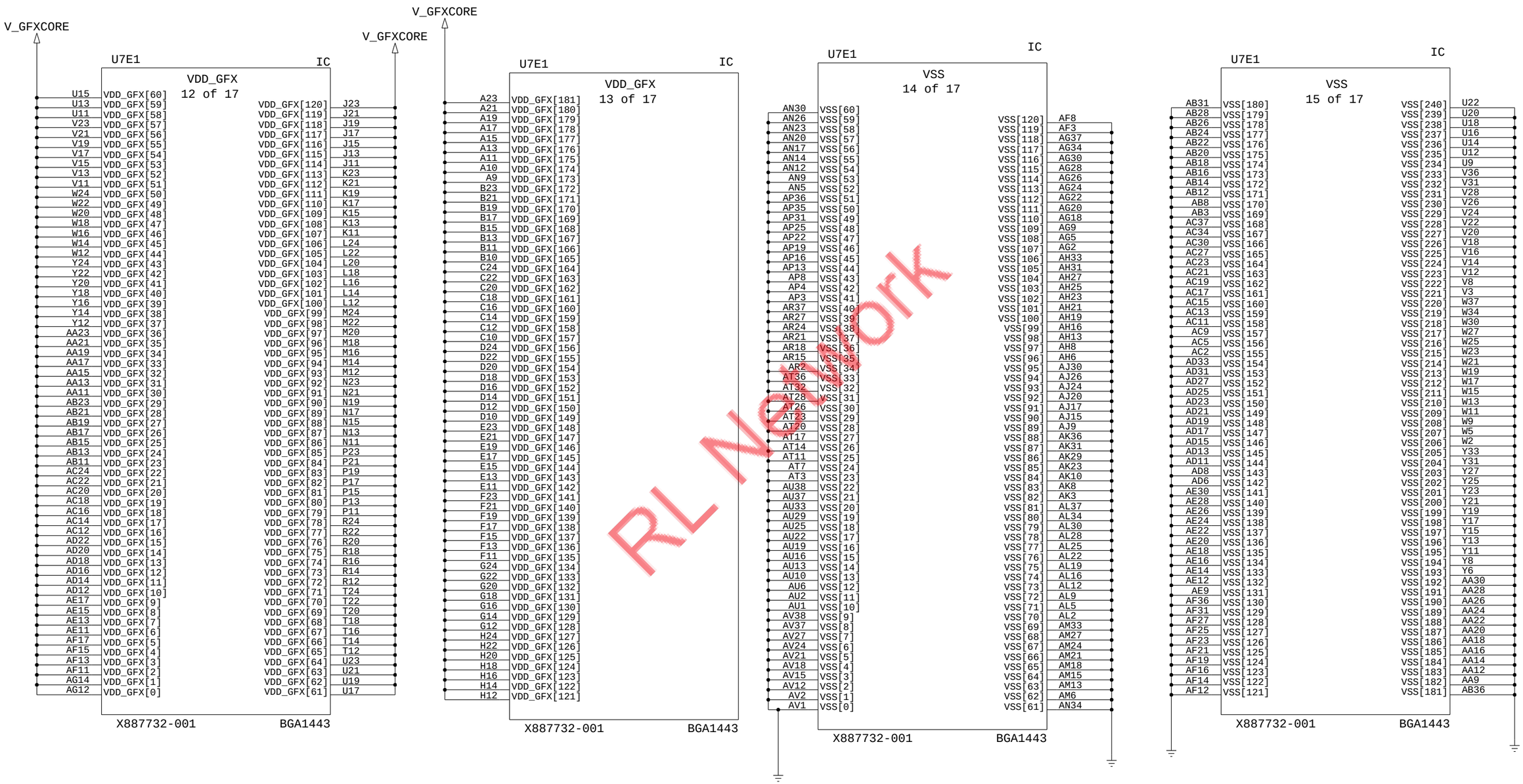




KKL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	3/72	3/72	G	1.01

SOC: POWER: V_GFXCORE,VSS



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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	4/72	4/72	G	1.01

SOC: MEMORY PARTITION C & D

U7E1 — IC — MEM CHANNEL D — 6 of 17

MD_DQ63	P2	MD_DQ63
MD_DQ62	W1	MD_DQ62
MD_DQ61	N4	MD_DQ61
MD_DQ60	V2	MD_DQ60
MD_DQ59	N1	MD_DQ59
MD_DQ58	W3	MD_DQ58
MD_DQ57	P1	MD_DQ57
MD_DQ56	W4	MD_DQ56
MD_DQ55	Y2	MD_DQ55
MD_DQ54	M2	MD_DQ54
MD_DQ53	Y1	MD_DQ53
MD_DQ52	M1	MD_DQ52
MD_DQ51	T1	MD_DQ51
MD_DQ50	N3	MD_DQ50
MD_DQ49	U3	MD_DQ49
MD_DQ48	R4	MD_DQ48
MD_DQ47	M7	MD_DQ47
MD_DQ46	R6	MD_DQ46
MD_DQ45	M5	MD_DQ45
MD_DQ44	P7	MD_DQ44
MD_DQ43	M4	MD_DQ43
MD_DQ42	R8	MD_DQ42
MD_DQ41	N6	MD_DQ41
MD_DQ40	T4	MD_DQ40
MD_DQ39	L4	MD_DQ39
MD_DQ38	H1	MD_DQ38
MD_DQ37	L3	MD_DQ37
MD_DQ36	G4	MD_DQ36
MD_DQ35	L1	MD_DQ35
MD_DQ34	H2	MD_DQ34
MD_DQ33	K1	MD_DQ33
MD_DQ32	J1	MD_DQ32
MD_DQ31	H5	MD_DQ31
MD_DQ30	K5	MD_DQ30
MD_DQ29	H4	MD_DQ29
MD_DQ28	K4	MD_DQ28
MD_DQ27	G8	MD_DQ27
MD_DQ26	L6	MD_DQ26
MD_DQ25	H7	MD_DQ25
MD_DQ24	L8	MD_DQ24
MD_DQ23	G3	MD_DQ23
MD_DQ22	C1	MD_DQ22
MD_DQ21	G1	MD_DQ21
MD_DQ20	C3	MD_DQ20
MD_DQ19	F1	MD_DQ19
MD_DQ18	D2	MD_DQ18
MD_DQ17	E1	MD_DQ17
MD_DQ16	D1	MD_DQ16
MD_DQ15	C8	MD_DQ15
MD_DQ14	D5	MD_DQ14
MD_DQ13	E8	MD_DQ13
MD_DQ12	G6	MD_DQ12
MD_DQ11	D9	MD_DQ11
MD_DQ10	F5	MD_DQ10
MD_DQ9	B7	MD_DQ9
MD_DQ8	F4	MD_DQ8
MD_DQ7	A3	MD_DQ7
MD_DQ6	D6	MD_DQ6
MD_DQ5	B3	MD_DQ5
MD_DQ4	A7	MD_DQ4
MD_DQ3	D4	MD_DQ3
MD_DQ2	C6	MD_DQ2
MD_DQ1	C4	MD_DQ1
MD_DQ0	A6	MD_DQ0
MD_DQSL_0_P	B5	MD_DQSL_0_P
MD_DQSL_0_N	A5	MD_DQSL_0_N
MD_DQSL_1_P	E3	MD_DQSL_1_P
MD_DQSL_1_N	E4	MD_DQSL_1_N
MD_DQSL_2_P	J3	MD_DQSL_2_P
MD_DQSL_2_N	J4	MD_DQSL_2_N
MD_DQSL_3_P	R1	MD_DQSL_3_P
MD_DQSL_3_N	T2	MD_DQSL_3_N
MD_DQSU_0_P	E6	MD_DQSU_0_P
MD_DQSU_0_N	F7	MD_DQSU_0_N
MD_DQSU_1_P	J8	MD_DQSU_1_P
MD_DQSU_1_N	K7	MD_DQSU_1_N
MD_DQSU_2_P	P4	MD_DQSU_2_P
MD_DQSU_2_N	P5	MD_DQSU_2_N
MD_DQSU_3_P	U1	MD_DQSU_3_P
MD_DQSU_3_N	V1	MD_DQSU_3_N
MD_DML_0	A4	MD_DML_0
MD_DMU_0	D7	MD_DMU_0
MD_DML_1	F2	MD_DML_1
MD_DMU_1	J6	MD_DMU_1
MD_DML_2	K2	MD_DML_2
MD_DMU_2	N8	MD_DMU_2
MD_DML_3	U4	MD_DML_3
MD_DMU_3	R3	MD_DMU_3

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V_MEMIO
R3R10 40.2 OHM 1% 2 EMPTY 402
R3R5 40.2 OHM 1% 2 EMPTY 402

MD_TEST	AG11	MD_TEST
MD_CLK0_DP	K9	MD_CLK0_DP
MD_CLK0_DN	J10	MD_CLK0_DN
MD_A15	V7	MD_A<15>
MD_A14	W10	MD_A<14>
MD_A13	U10	MD_A<13>
MD_A12	W6	MD_A<12>
MD_A11	Y5	MD_A<11>
MD_A10	N10	MD_A<10>
MD_A9	V9	MD_A<9>
MD_A8	W7	MD_A<8>
MD_A7	U7	MD_A<7>
MD_A6	Y7	MD_A<6>
MD_A5	V4	MD_A<5>
MD_A4	R10	MD_A<4>
MD_A3	U8	MD_A<3>
MD_A2	Y4	MD_A<2>
MD_A1	W8	MD_A<1>
MD_A0	T9	MD_A<0>
MD_BA0	T7	MD_BA<0>
MD_BA1	V5	MD_BA<1>
MD_BA2	U6	MD_BA<2>
MD_CKE0	N7	MD_CKE0
MD_CAS_N	L10	MD_CAS_N
MD_RAS_N	M9	MD_RAS_N
MD_CS0_N	R7	MD_CS0_N
MD_ODT0	T5	MD_ODT0
MD_WE_N	P9	MD_WE_N
MD_RESET	Y9	MD_RESET_N
MD_CKE1	H9	
MD_CS1_N	F9	
MD_ODT1	G10	
MD_VREFDQ	G7	MD_VREFDQ_MM
MD_ZVDDIO	J7	MD_ZVDDIO

R2R3 0 OHM 5% 402 EMPTY
R2R4 40.2 OHM 1% 2 CH 402

U7E1 — IC — MEM CHANNEL C — 5 of 17

MC_DQ63	AN8	MC_DQ63
MC_DQ62	AM11	MC_DQ62
MC_DQ61	AM8	MC_DQ61
MC_DQ60	AN10	MC_DQ60
MC_DQ59	AR7	MC_DQ59
MC_DQ58	AP11	MC_DQ58
MC_DQ57	AP9	MC_DQ57
MC_DQ56	AR11	MC_DQ56
MC_DQ55	AV11	MC_DQ55
MC_DQ54	AR8	MC_DQ54
MC_DQ53	AU11	MC_DQ53
MC_DQ52	AV7	MC_DQ52
MC_DQ51	AV10	MC_DQ51
MC_DQ50	AT8	MC_DQ50
MC_DQ49	AR10	MC_DQ49
MC_DQ48	AV8	MC_DQ48
MC_DQ47	AT2	MC_DQ47
MC_DQ46	AN6	MC_DQ46
MC_DQ45	AP2	MC_DQ45
MC_DQ44	AN4	MC_DQ44
MC_DQ43	AT1	MC_DQ43
MC_DQ42	AM7	MC_DQ42
MC_DQ41	AN3	MC_DQ41
MC_DQ40	AP7	MC_DQ40
MC_DQ39	AU7	MC_DQ39
MC_DQ38	AV3	MC_DQ38
MC_DQ37	AV6	MC_DQ37
MC_DQ36	AU3	MC_DQ36
MC_DQ35	AT6	MC_DQ35
MC_DQ34	AR4	MC_DQ34
MC_DQ33	AV5	MC_DQ33
MC_DQ32	AT4	MC_DQ32
MC_DQ31	AJ8	MC_DQ31
MC_DQ30	AL6	MC_DQ30
MC_DQ29	AH4	MC_DQ29
MC_DQ28	AL8	MC_DQ28
MC_DQ27	AH5	MC_DQ27
MC_DQ26	AM5	MC_DQ26
MC_DQ25	AJ6	MC_DQ25
MC_DQ24	AM4	MC_DQ24
MC_DQ23	AR1	MC_DQ23
MC_DQ22	AK1	MC_DQ22
MC_DQ21	AP1	MC_DQ21
MC_DQ20	AJ4	MC_DQ20
MC_DQ19	AN1	MC_DQ19
MC_DQ18	AK2	MC_DQ18
MC_DQ17	AM1	MC_DQ17
MC_DQ16	AL1	MC_DQ16
MC_DQ15	AC1	MC_DQ15
MC_DQ14	AG4	MC_DQ14
MC_DQ13	AB2	MC_DQ13
MC_DQ12	AG3	MC_DQ12
MC_DQ11	AB1	MC_DQ11
MC_DQ10	AH1	MC_DQ10
MC_DQ9	AC3	MC_DQ9
MC_DQ8	AH2	MC_DQ8
MC_DQ7	AJ3	MC_DQ7
MC_DQ6	AA3	MC_DQ6
MC_DQ5	AJ1	MC_DQ5
MC_DQ4	AA1	MC_DQ4
MC_DQ3	AE3	MC_DQ3
MC_DQ2	AA4	MC_DQ2
MC_DQ1	AE4	MC_DQ1
MC_DQ0	AD1	MC_DQ0
MC_DQSL_0_P	AD2	MC_DQSL_0_P
MC_DQSL_0_N	AE1	MC_DQSL_0_N
MC_DQSL_1_P	AL3	MC_DQSL_1_P
MC_DQSL_1_N	AL4	MC_DQSL_1_N
MC_DQSL_2_P	AV4	MC_DQSL_2_P
MC_DQSL_2_N	AU5	MC_DQSL_2_N
MC_DQSL_3_P	AU9	MC_DQSL_3_P
MC_DQSL_3_N	AV9	MC_DQSL_3_N
MC_DQSU_0_P	AF2	MC_DQSU_0_P
MC_DQSU_0_N	AG1	MC_DQSU_0_N
MC_DQSU_1_P	AK4	MC_DQSU_1_P
MC_DQSU_1_N	AK5	MC_DQSU_1_N
MC_DQSU_2_P	AP5	MC_DQSU_2_P
MC_DQSU_2_N	AR5	MC_DQSU_2_N
MC_DQSU_3_P	AM9	MC_DQSU_3_P
MC_DQSU_3_N	AM10	MC_DQSU_3_N
MC_DML_0	AF1	MC_DML_0
MC_DMU_0	AC4	MC_DMU_0
MC_DML_1	AM2	MC_DML_1
MC_DMU_1	AK7	MC_DMU_1
MC_DML_2	AR6	MC_DML_2
MC_DMU_2	AR3	MC_DMU_2
MC_DML_3	AT10	MC_DML_3
MC_DMU_3	AR9	MC_DMU_3

X887732-001 BGA1443

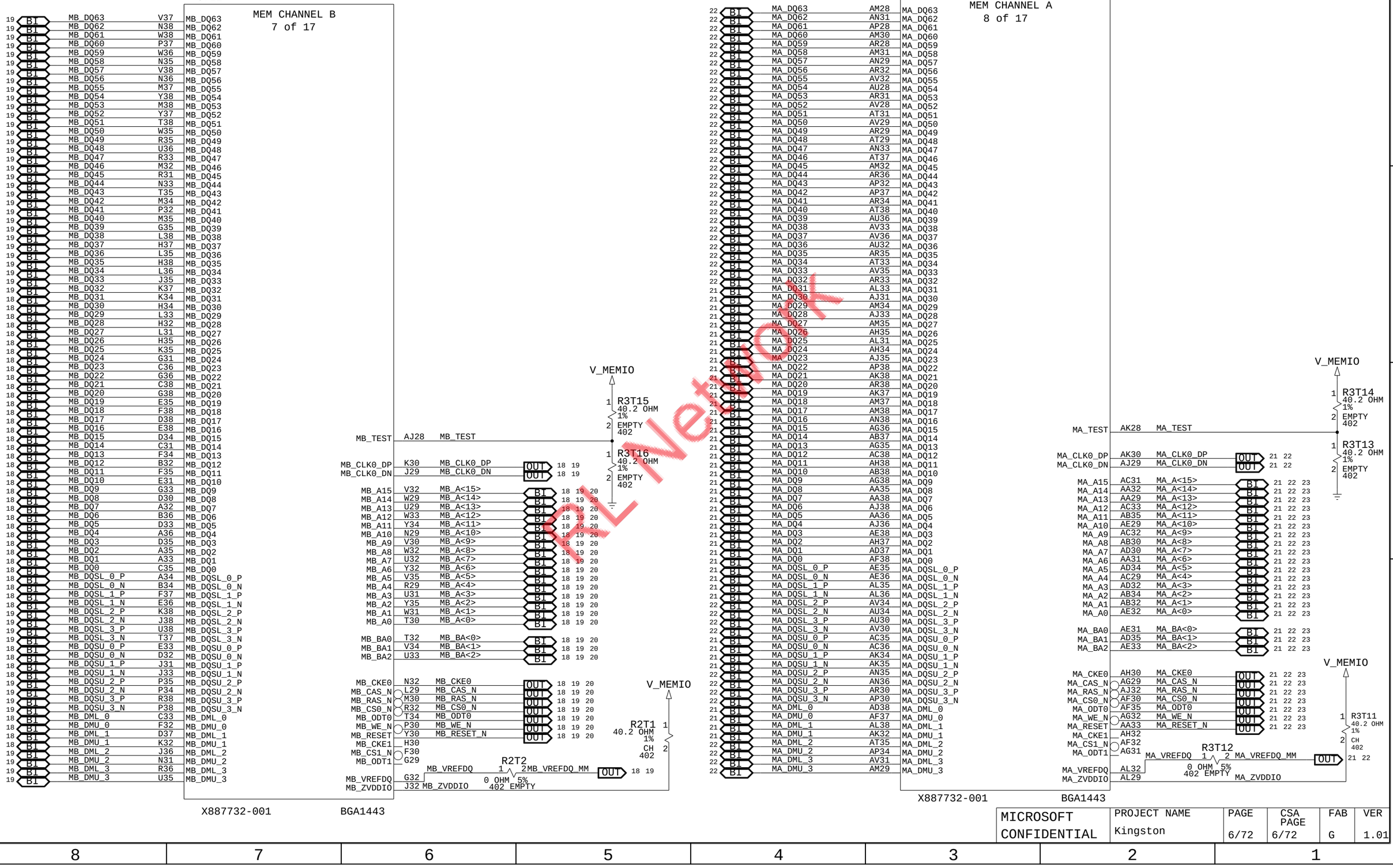
V_MEMIO
R3R9 40.2 OHM 1% 2 EMPTY 402
R3R4 40.2 OHM 1% 2 EMPTY 402

MC_TEST	AJ11	MC_TEST
MC_CLK0_DP	AK9	MC_CLK0_DP
MC_CLK0_DN	AJ10	MC_CLK0_DN
MC_A15	AC8	MC_A<15>
MC_A14	AA7	MC_A<14>
MC_A13	AA10	MC_A<13>
MC_A12	AC6	MC_A<12>
MC_A11	AB4	MC_A<11>
MC_A10	AE10	MC_A<10>
MC_A9	AC7	MC_A<9>
MC_A8	AB9	MC_A<8>
MC_A7	AD9	MC_A<7>
MC_A6	AA8	MC_A<6>
MC_A5	AD5	MC_A<5>
MC_A4	AC10	MC_A<4>
MC_A3	AD7	MC_A<3>
MC_A2	AB5	MC_A<2>
MC_A1	AB7	MC_A<1>
MC_A0	AE7	MC_A<0>
MC_BA0	AE8	MC_BA<0>
MC_BA1	AD4	MC_BA<1>
MC_BA2	AE6	MC_BA<2>
MC_CKE0	AH9	MC_CKE0
MC_CAS_N	AG10	MC_CAS_N
MC_RAS_N	AJ7	MC_RAS_N
MC_CS0_N	AF9	MC_CS0_N
MC_ODT0	AF4	MC_ODT0
MC_WE_N	AG7	MC_WE_N
MC_RESET	AA6	MC_RESET_N
MC_CKE1	AH7	
MC_CS1_N	AF7	
MC_ODT1	AG8	
MC_VREFDQ	AL7	MC_VREFDQ_MM
MC_ZVDDIO	AL10	MC_ZVDDIO

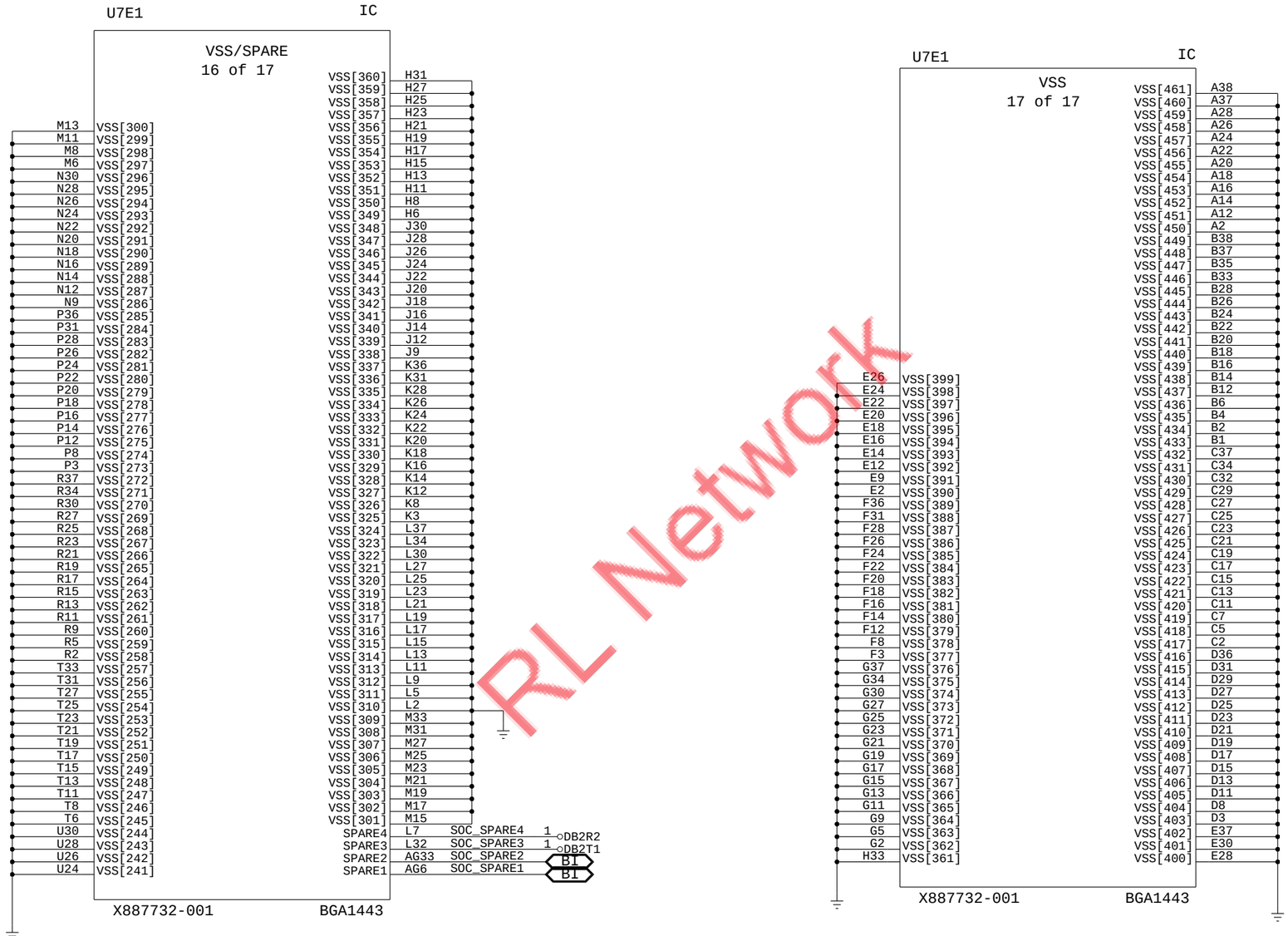
R3R1 0 OHM 5% 402 EMPTY
R3R7 40.2 OHM 1% 2 CH 402

MICROSOFT CONFIDENTIAL	PROJECT NAME Kingston	PAGE 5/72	CSA PAGE 5/72	FAB G	VER 1.01

SOC: MEMORY PARTITION A & B



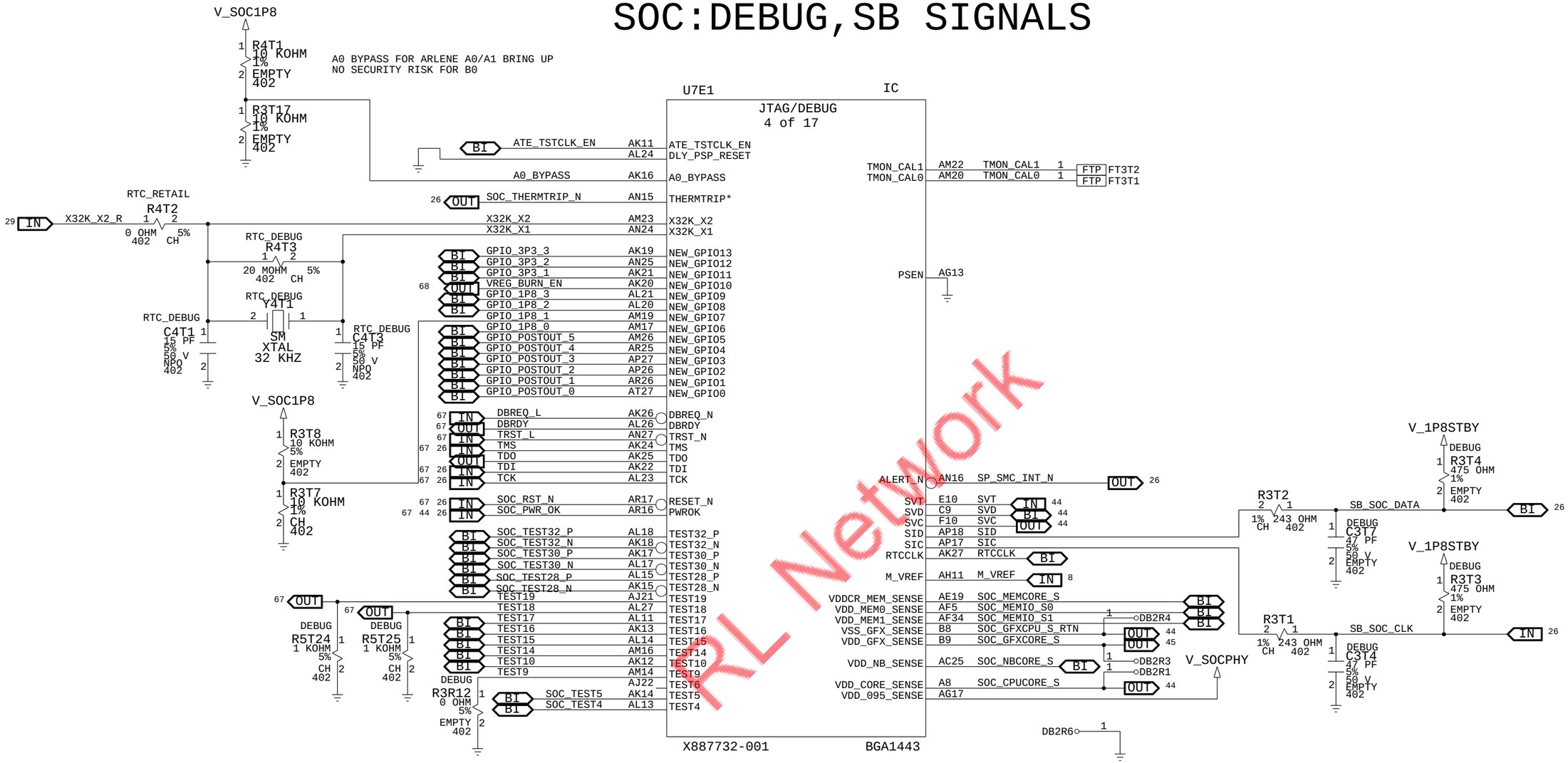
SOC: VSS,SPARE



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	7/72	7/72	G	1.01

SOC:DEBUG,SB SIGNALS



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	8/72	8/72	G	1.01

SOC: DECOUPLING

V_GFXCORE 29 0805 22UF

C2T35 1 2 22 UF 20% 6.3 V X5R 805
C2R38 1 2 22 UF 20% 6.3 V X5R 805
C2T15 1 2 22 UF 20% 6.3 V X5R 805
C2R11 1 2 22 UF 20% 6.3 V X5R 805
C2R12 1 2 22 UF 20% 6.3 V X5R 805

C2R37 1 2 22 UF 20% 6.3 V X5R 805
C2R33 1 2 22 UF 20% 6.3 V EMPTY 805
C2T14 1 2 22 UF 20% 6.3 V X5R 805
C2R21 1 2 22 UF 20% 6.3 V X5R 805
C2T12 1 2 22 UF 20% 6.3 V X5R 805
C2R19 1 2 22 UF 20% 6.3 V X5R 805
C2R18 1 2 22 UF 20% 6.3 V X5R 805

C2T31 1 2 22 UF 20% 6.3 V EMPTY 805
C2R10 1 2 22 UF 20% 6.3 V EMPTY 805
C2T11 1 2 22 UF 20% 6.3 V EMPTY 805
C2T33 1 2 22 UF 20% 6.3 V X5R 805
C2R36 1 2 22 UF 20% 6.3 V X5R 805
C2T13 1 2 22 UF 20% 6.3 V X5R 805
C2T30 1 2 22 UF 20% 6.3 V EMPTY 805
C2R13 1 2 22 UF 20% 6.3 V X5R 805

C2R17 1 2 22 UF 20% 6.3 V EMPTY 805
C2R16 1 2 22 UF 20% 6.3 V EMPTY 805
C2T34 1 2 22 UF 20% 6.3 V X5R 805
C2T10 1 2 22 UF 20% 6.3 V EMPTY 805
C2R34 1 2 22 UF 20% 6.3 V EMPTY 805
C2R35 1 2 22 UF 20% 6.3 V X5R 805
C2T32 1 2 22 UF 20% 6.3 V X5R 805
C2R9 1 2 22 UF 20% 6.3 V EMPTY 805
C2R20 1 2 22 UF 20% 6.3 V X5R 805

V_GFXCORE 44 0805 10UF

C3R17 1 2 10 UF 10% 6.3 V X5R 805
C2T6 1 2 10 UF 10% 6.3 V X5R 805
C2T7 1 2 10 UF 10% 6.3 V X5R 805
C2T8 1 2 10 UF 10% 6.3 V X5R 805
C2T9 1 2 10 UF 10% 6.3 V X5R 805
C3T2 1 2 10 UF 10% 6.3 V X5R 805
C3R18 1 2 10 UF 10% 6.3 V X5R 805
C3R19 1 2 10 UF 10% 6.3 V X5R 805
C2T40 1 2 10 UF 10% 6.3 V X5R 805

C3R20 1 2 10 UF 10% 6.3 V X5R 805
C2T1 1 2 10 UF 10% 6.3 V X5R 805
C2T2 1 2 10 UF 10% 6.3 V X5R 805
C2T41 1 2 10 UF 10% 6.3 V X5R 805
C2T16 1 2 10 UF 10% 6.3 V X5R 805
C3T1 1 2 10 UF 10% 6.3 V X5R 805
C2R24 1 2 10 UF 10% 6.3 V X5R 805
C2R25 1 2 10 UF 10% 6.3 V X5R 805
C2R26 1 2 10 UF 10% 6.3 V X5R 805
C2R27 1 2 10 UF 10% 6.3 V X5R 805

C2R28 1 2 10 UF 10% 6.3 V X5R 805
C2R29 1 2 10 UF 10% 6.3 V X5R 805
C2R30 1 2 10 UF 10% 6.3 V X5R 805
C2R31 1 2 10 UF 10% 6.3 V X5R 805
C2R32 1 2 10 UF 10% 6.3 V X5R 805
C2T5 1 2 10 UF 10% 6.3 V X5R 805
C2T4 1 2 10 UF 10% 6.3 V X5R 805
C2T3 1 2 10 UF 10% 6.3 V X5R 805
C2T17 1 2 10 UF 10% 6.3 V X5R 805
C2T18 1 2 10 UF 10% 6.3 V X5R 805

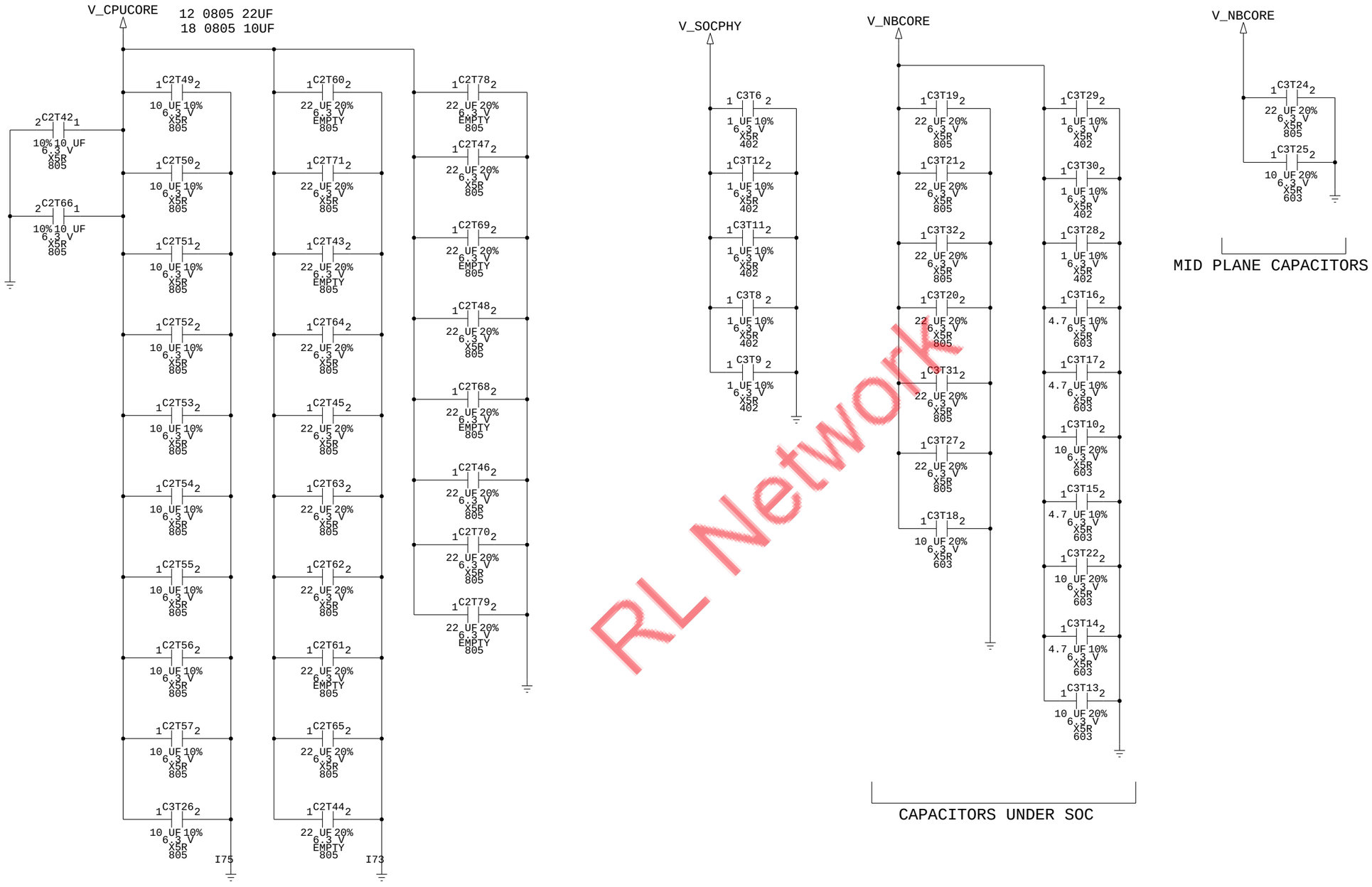
C2T19 1 2 10 UF 10% 6.3 V X5R 805
C2T20 1 2 10 UF 10% 6.3 V X5R 805
C2T21 1 2 10 UF 10% 6.3 V X5R 805
C2T22 1 2 10 UF 10% 6.3 V X5R 805
C2T36 1 2 10 UF 10% 6.3 V X5R 805
C2T38 1 2 10 UF 10% 6.3 V X5R 805
C2T23 1 2 10 UF 10% 6.3 V X5R 805
C2T24 1 2 10 UF 10% 6.3 V X5R 805
C2T25 1 2 10 UF 10% 6.3 V X5R 805
C2T26 1 2 10 UF 10% 6.3 V X5R 805

C2T28 1 2 10 UF 10% 6.3 V X5R 805
C2T29 1 2 10 UF 10% 6.3 V X5R 805
C2T37 1 2 10 UF 10% 6.3 V X5R 805
C2T39 1 2 10 UF 10% 6.3 V X5R 805
C2T27 1 2 10 UF 10% 6.3 V X5R 805

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	9/72	9/72	G	1.01

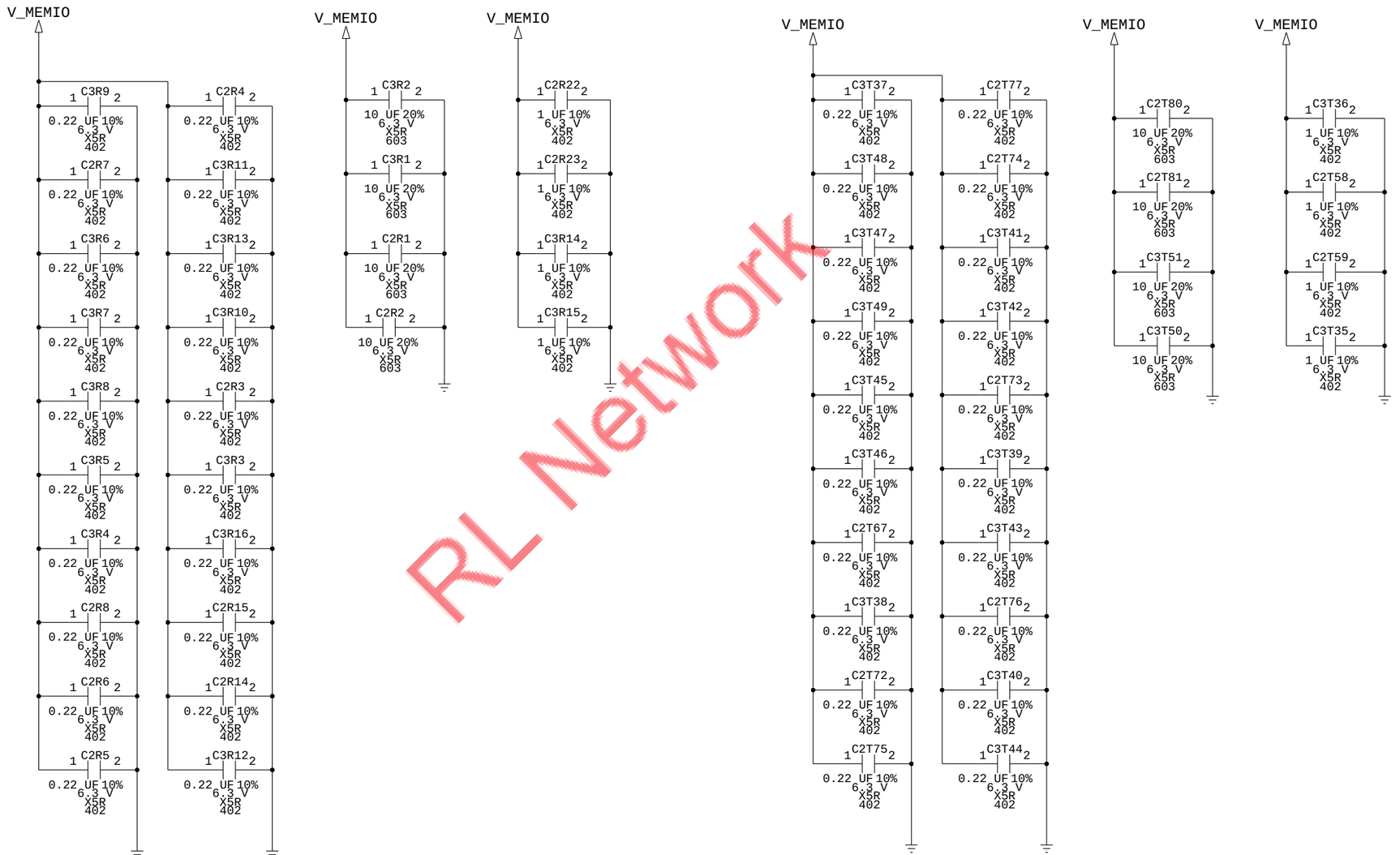
SOC: DECOUPLING



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	10/72	10/72	G	1.01

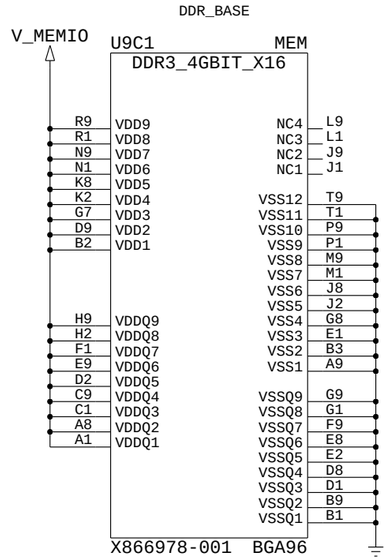
SOC: DECOUPLING



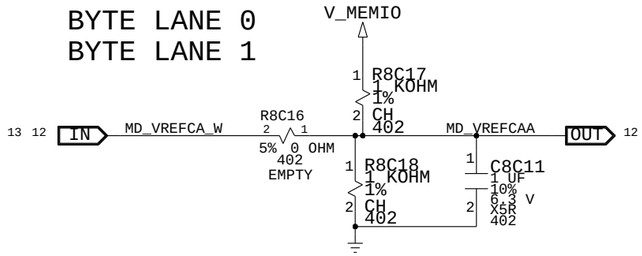
RL Network

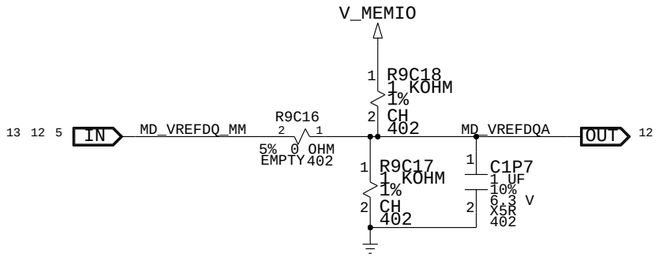
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	11/72	11/72	G	1.01

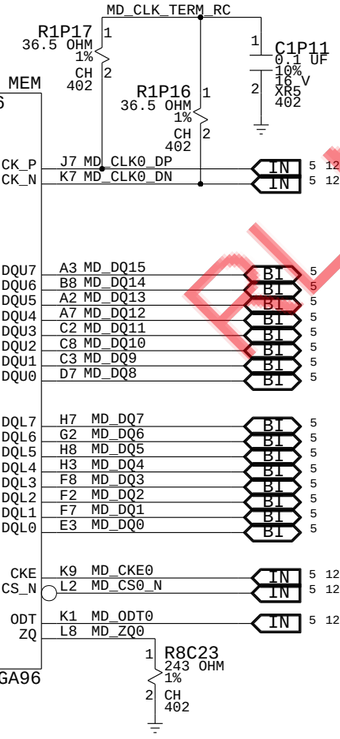
MEMORY: CHANNEL D



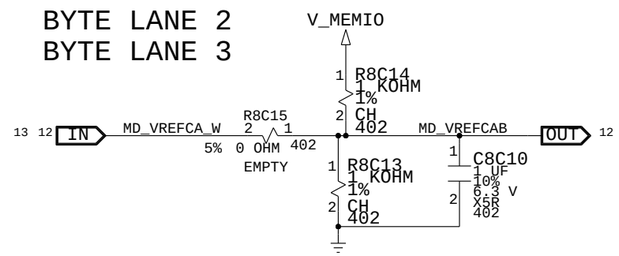
BYTE LANE 0
BYTE LANE 1

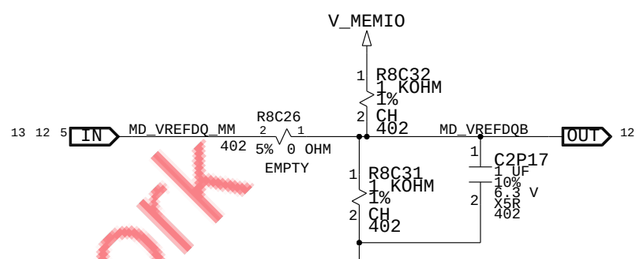


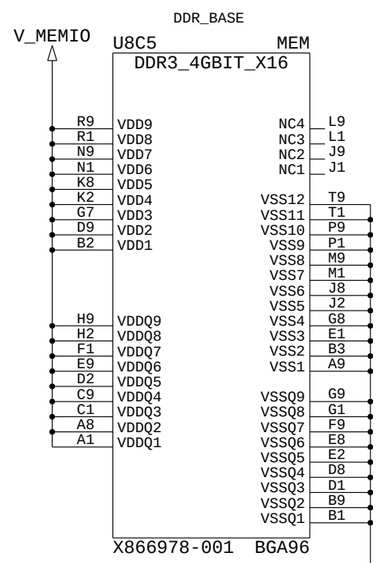


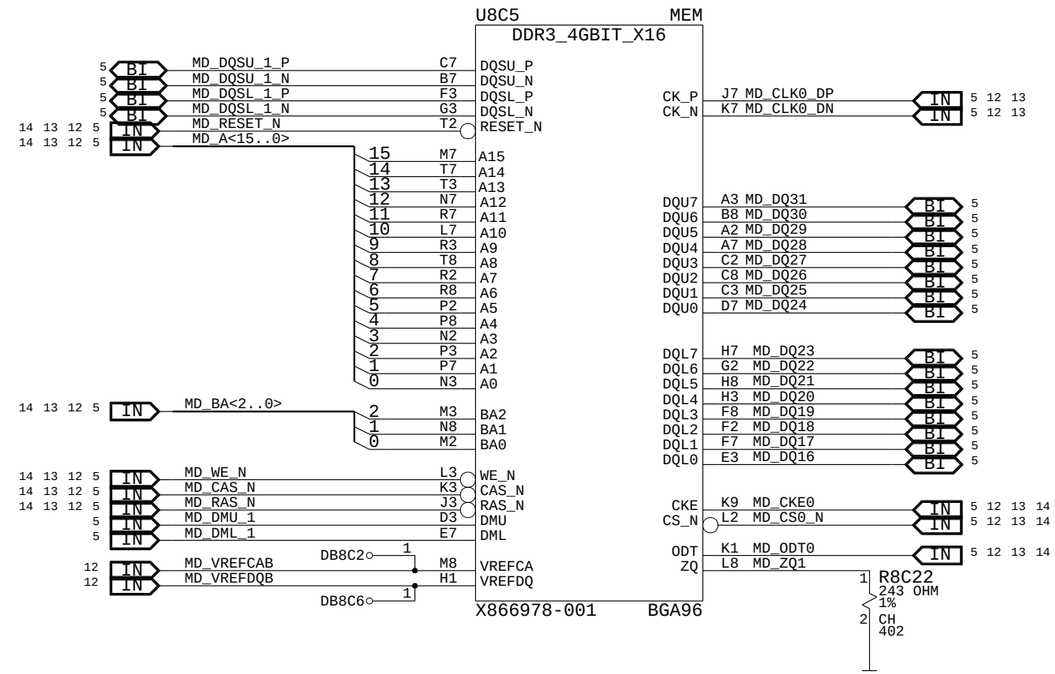


BYTE LANE 2
BYTE LANE 3









BL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	12/72	12/72	G	1.01

MEMORY: CHANNEL D

DDR_BASE

V_MEMIO

U8C4 MEM
DDR3_4GBIT_X16

R9	VDD9	NC4	L9
R1	VDD8	NC3	L1
N9	VDD7	NC2	J9
N1	VDD6	NC1	J1
K8	VDD5		
K2	VDD4	VSS12	T9
G7	VDD3	VSS11	T1
D9	VDD2	VSS10	P9
B2	VDD1	VSS9	P1
		VSS8	M9
		VSS7	M1
		VSS6	J8
		VSS5	J2
H9	VDDQ9	VSS4	G8
H2	VDDQ8	VSS3	E1
F1	VDDQ7	VSS2	B3
E9	VDDQ6	VSS1	A9
D2	VDDQ5		
C9	VDDQ4	VSSQ9	G9
C1	VDDQ3	VSSQ8	G1
A8	VDDQ2	VSSQ7	F9
A1	VDDQ1	VSSQ6	E8
		VSSQ5	E2
		VSSQ4	D8
		VSSQ3	D1
		VSSQ2	B9
		VSSQ1	B1

X866978-001 BGA96

BYTE LANE 4
BYTE LANE 5

V_MEMIO

13 12 IN MD_VREFCA_W — R8C12 2 1 5% 0 OHM EMPTY 402 — MD_VREFCAC OUT 13

R8C11 1 KOHM 1% CH 402

R8C10 1 KOHM 1% CH 402

C8C9 1 UF 10% 6.3 V X5R 402

V_MEMIO

13 12 5 IN MD_VREFDQ_MM — R8C25 2 1 5% 0 OHM EMPTY402 — MD_VREFDQC OUT 13

R8C30 1 KOHM 1% CH 402

R8C29 1 KOHM 1% CH 402

C2P18 1 UF 10% 6.3 V X5R 402

BYTE LANE 6
BYTE LANE 7

V_MEMIO

13 12 IN MD_VREFCA_W — R7C11 2 1 5% 0 OHM EMPTY 402 — MD_VREFCAD OUT 13

R7C10 1 KOHM 1% CH 402

R7C9 1 KOHM 1% CH 402

C7C15 1 UF 10% 6.3 V X5R 402

V_MEMIO

13 12 5 IN MD_VREFDQ_MM — R8C24 2 1 5% 0 OHM EMPTY 402 — MD_VREFDQD OUT 13

R8C28 1 KOHM 1% CH 402

R8C27 1 KOHM 1% CH 402

C2P19 1 UF 10% 6.3 V X5R 402

DDR_BASE

V_MEMIO

U8C3 MEM
DDR3_4GBIT_X16

R9	VDD9	NC4	L9
R1	VDD8	NC3	L1
N9	VDD7	NC2	J9
N1	VDD6	NC1	J1
K8	VDD5		
K2	VDD4	VSS12	T9
G7	VDD3	VSS11	T1
D9	VDD2	VSS10	P9
B2	VDD1	VSS9	P1
		VSS8	M9
		VSS7	M1
		VSS6	J8
		VSS5	J2
H9	VDDQ9	VSS4	G8
H2	VDDQ8	VSS3	E1
F1	VDDQ7	VSS2	B3
E9	VDDQ6	VSS1	A9
D2	VDDQ5		
C9	VDDQ4	VSSQ9	G9
C1	VDDQ3	VSSQ8	G1
A8	VDDQ2	VSSQ7	F9
A1	VDDQ1	VSSQ6	E8
		VSSQ5	E2
		VSSQ4	D8
		VSSQ3	D1
		VSSQ2	B9
		VSSQ1	B1

X866978-001 BGA96

U8C4 MEM
DDR3_4GBIT_X16

5 BI	MD_DQSU_2_P	C7	DQSU_P	
5 BI	MD_DQSU_2_N	B7	DQSU_N	
5 BI	MD_DQSL_2_P	F3	DQSL_P	
5 BI	MD_DQSL_2_N	G3	DQSL_N	
14 13 12 5 IN	MD_RESET_N	T2	RESET_N	
14 13 12 5 IN	MD_A<15..0>			
	15	M7	A15	
	14	T7	A14	
	13	T3	A13	
	12	N7	A12	
	11	R7	A11	
	10	L7	A10	
	9	R3	A9	
	8	T8	A8	
	7	R2	A7	
	6	R8	A6	
	5	P2	A5	
	4	P8	A4	
	3	N2	A3	
	2	P3	A2	
	1	P7	A1	
	0	N3	A0	
14 13 12 5 IN	MD_BA<2..0>			
	2	M3	BA2	
	1	N8	BA1	
	0	M2	BA0	
14 13 12 5 IN	MD_WE_N	L3	WE_N	
14 13 12 5 IN	MD_CAS_N	K3	CAS_N	
14 13 12 5 IN	MD_RAS_N	J3	RAS_N	
5 IN	MD_DMU_2	D3	DMU	
5 IN	MD_DML_2	E7	DML	
DB8C1 1				
13 IN	MD_VREFCAC	M8	VREFCA	
13 IN	MD_VREFDQC	H1	VREFDQ	
DB8C4 1				

	CK_P	J7	MD_CLK0_DP	5 12 13
	CK_N	K7	MD_CLK0_DN	5 12 13
DQU7	A3	MD_DQ47	BI	5
DQU6	B8	MD_DQ46	BI	5
DQU5	A2	MD_DQ45	BI	5
DQU4	A7	MD_DQ44	BI	5
DQU3	C2	MD_DQ43	BI	5
DQU2	C8	MD_DQ42	BI	5
DQU1	C3	MD_DQ41	BI	5
DQU0	D7	MD_DQ40	BI	5
DQL7	H7	MD_DQ39	BI	5
DQL6	G2	MD_DQ38	BI	5
DQL5	H8	MD_DQ37	BI	5
DQL4	H3	MD_DQ36	BI	5
DQL3	F8	MD_DQ35	BI	5
DQL2	F2	MD_DQ34	BI	5
DQL1	F7	MD_DQ33	BI	5
DQL0	E3	MD_DQ32	BI	5
CKE	K9	MD_CKE0	IN	5 12 13 14
CS_N	L2	MD_CS0_N	IN	5 12 13 14
ODT	K1	MD_ODT0	IN	5 12 13 14
ZQ	L8	MD_ZQ2	IN	5 12 13 14

R8C21 1 243 OHM 1% 2 CH 402

U8C3 MEM
DDR3_4GBIT_X16

5 BI	MD_DQSU_3_P	C7	DQSU_P	
5 BI	MD_DQSU_3_N	B7	DQSU_N	
5 BI	MD_DQSL_3_P	F3	DQSL_P	
5 BI	MD_DQSL_3_N	G3	DQSL_N	
14 13 12 5 IN	MD_RESET_N	T2	RESET_N	
14 13 12 5 IN	MD_A<15..0>			
	15	M7	A15	
	14	T7	A14	
	13	T3	A13	
	12	N7	A12	
	11	R7	A11	
	10	L7	A10	
	9	R3	A9	
	8	T8	A8	
	7	R2	A7	
	6	R8	A6	
	5	P2	A5	
	4	P8	A4	
	3	N2	A3	
	2	P3	A2	
	1	P7	A1	
	0	N3	A0	
14 13 12 5 IN	MD_BA<2..0>			
	2	M3	BA2	
	1	N8	BA1	
	0	M2	BA0	
14 13 12 5 IN	MD_WE_N	L3	WE_N	
14 13 12 5 IN	MD_CAS_N	K3	CAS_N	
14 13 12 5 IN	MD_RAS_N	J3	RAS_N	
5 IN	MD_DMU_3	D3	DMU	
5 IN	MD_DML_3	E7	DML	
DB7C3 1				
13 IN	MD_VREFCAD	M8	VREFCA	
13 IN	MD_VREFDQD	H1	VREFDQ	
DB8C5 1				

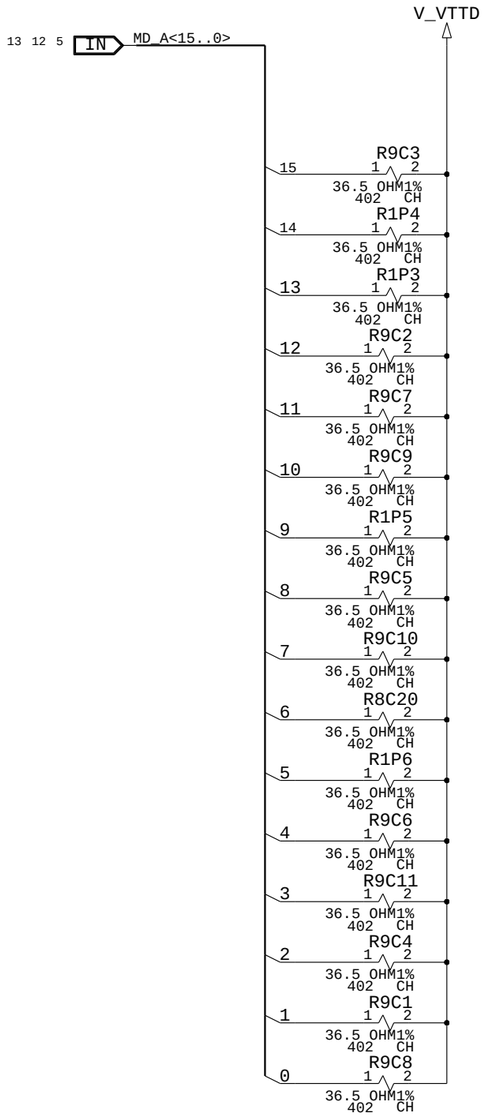
	CK_P	J7	MD_CLK0_DP	5 12 13
	CK_N	K7	MD_CLK0_DN	5 12 13
DQU7	A3	MD_DQ63	BI	5
DQU6	B8	MD_DQ62	BI	5
DQU5	A2	MD_DQ61	BI	5
DQU4	A7	MD_DQ60	BI	5
DQU3	C2	MD_DQ59	BI	5
DQU2	C8	MD_DQ58	BI	5
DQU1	C3	MD_DQ57	BI	5
DQU0	D7	MD_DQ56	BI	5
DQL7	H7	MD_DQ55	BI	5
DQL6	G2	MD_DQ54	BI	5
DQL5	H8	MD_DQ53	BI	5
DQL4	H3	MD_DQ52	BI	5
DQL3	F8	MD_DQ51	BI	5
DQL2	F2	MD_DQ50	BI	5
DQL1	F7	MD_DQ49	BI	5
DQL0	E3	MD_DQ48	BI	5
CKE	K9	MD_CKE0	IN	5 12 13 14
CS_N	L2	MD_CS0_N	IN	5 12 13 14
ODT	K1	MD_ODT0	IN	5 12 13 14
ZQ	L8	MD_ZQ3	IN	5 12 13 14

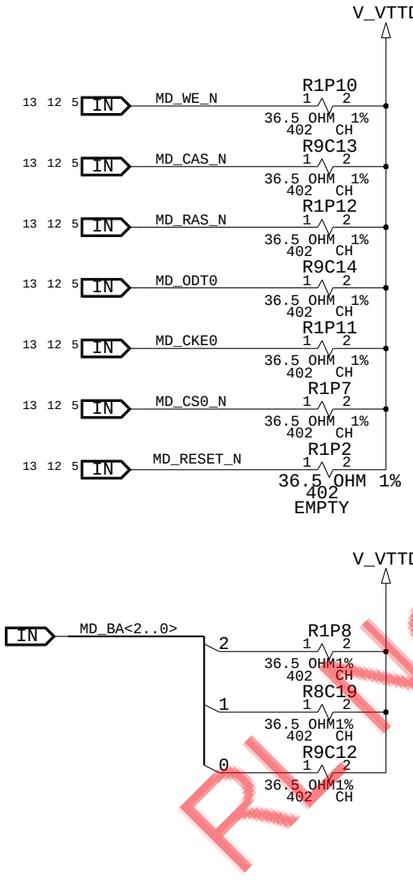
R7C12 1 243 OHM 1% 2 CH 402

BL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	13/72	13/72	G	1.01

MEMORY: CHANNEL D,DECOUPLING & TERMINATION





MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
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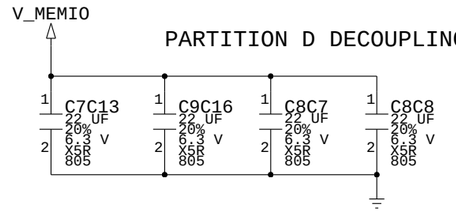
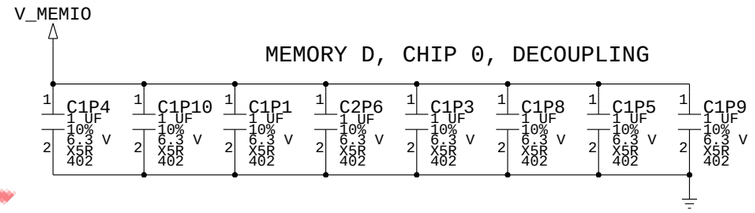
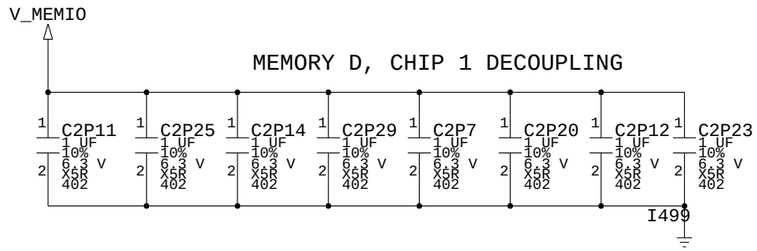
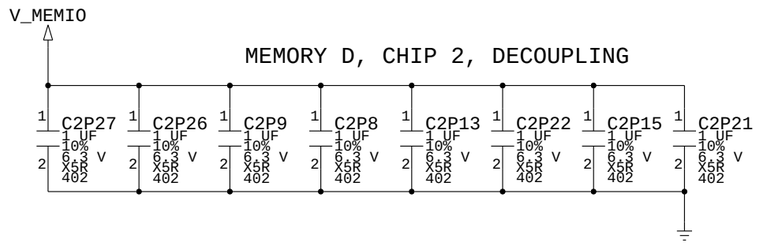
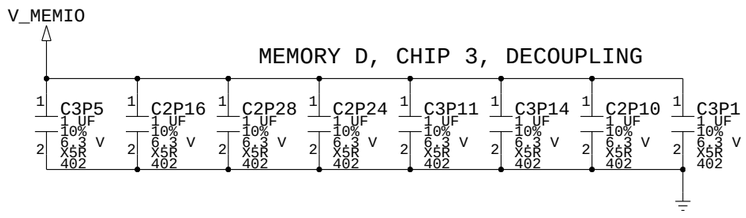
X903915-001	IC	U9F5,U8F3,U8F2,U8F1,U7F2,U7F1,U6E5,U6E3	MEM,SM,4GB,DDR3,E-DIE,20NM,2133MHZ,96FBGA,K4W4G1646E-BC1A,TYP,SAMSUNG	DDR_SAMSUNG
X903814-001	IC	U9C1,U8C5,U8C4,U8C3,U7C2,U7C1,U6D2,U6D3	MEM,SM,4GB,DDR3,POLARIS,25NM,2133MHZ,FBGA96,H5TQ4G63CFR-TEC,TYP,HYNIX	DDR_HYNIX_25NM
X903814-001	IC	U9F5,U8F3,U8F2,U8F1,U7F2,U7F1,U6E5,U6E3	MEM,SM,4GB,DDR3,POLARIS,25NM,2133MHZ,FBGA96,H5TQ4G63CFR-TEC,TYP,HYNIX	DDR_HYNIX_25NM
X945095-001	IC	U9C1,U8C5,U8C4,U8C3,U7C2,U7C1,U6D2,U6D3	MEM,SM,4GB,256X16,DDR3,96 FBGA,NT5CB256M16DP-FL,TYP	DDR_NANYA_30NM
X945095-001	IC	U9F5,U8F3,U8F2,U8F1,U7F2,U7F1,U6E5,U6E3	MEM,SM,4GB,256X16,DDR3,96 FBGA,NT5CB256M16DP-FL,TYP	DDR_NANYA_30NM











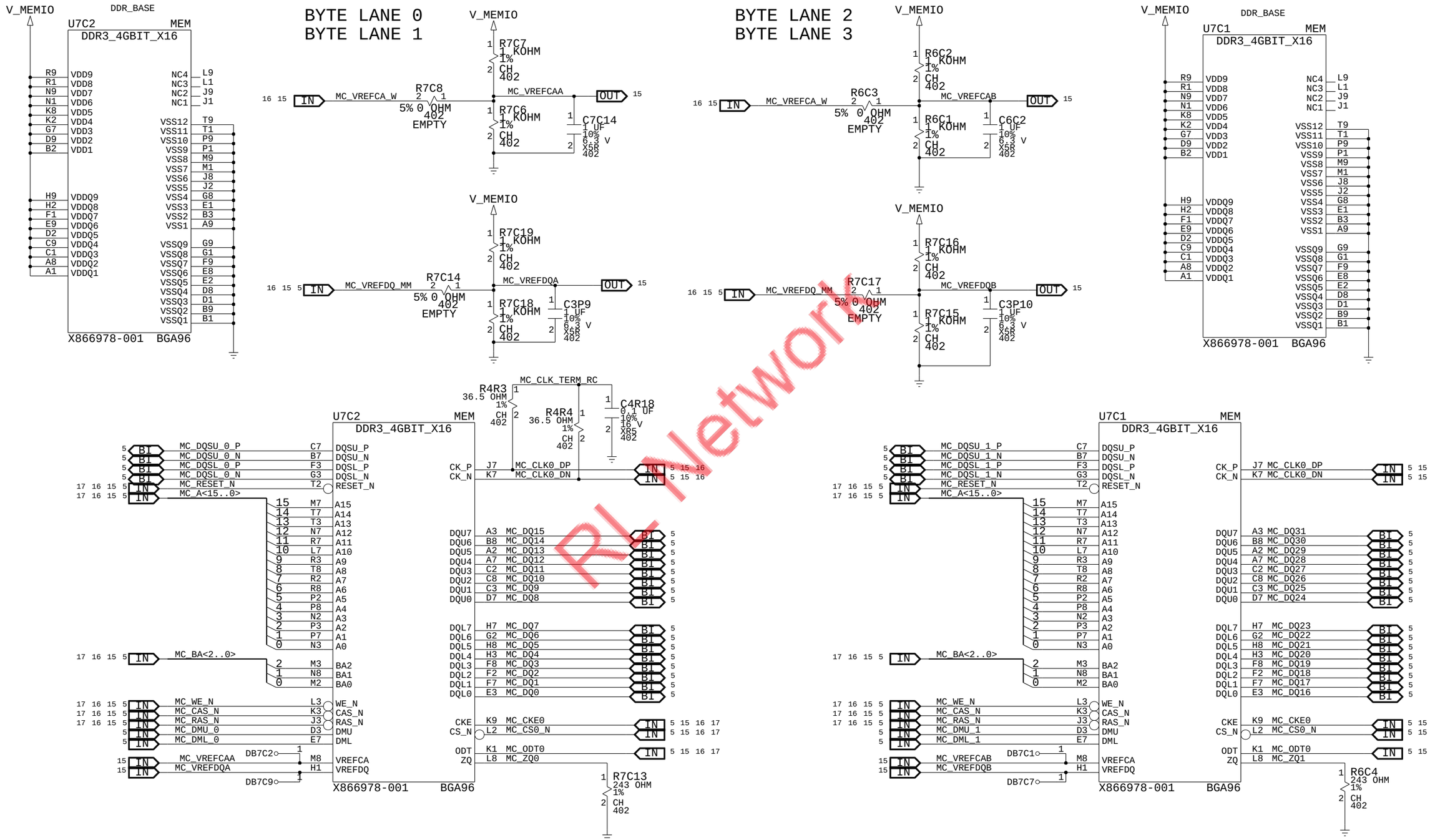
RU Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	14/72	14/72	G	1.01

MEMORY: CHANNEL C

BYTE LANE 0
BYTE LANE 1

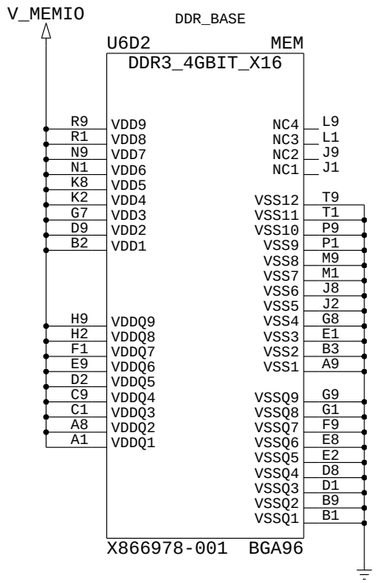
BYTE LANE 2
BYTE LANE 3



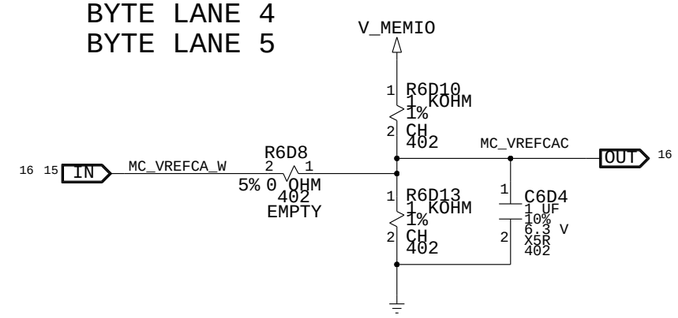
RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	15/72	15/72	G	1.01

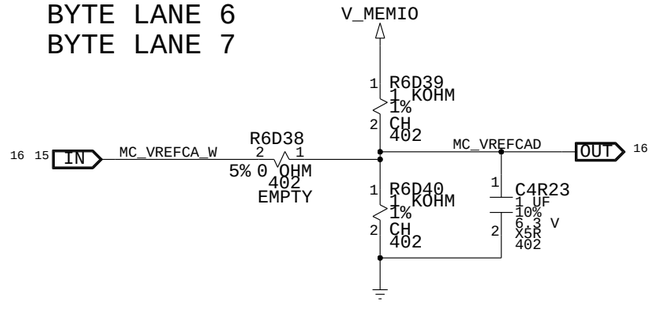
MEMORY: CHANNEL C

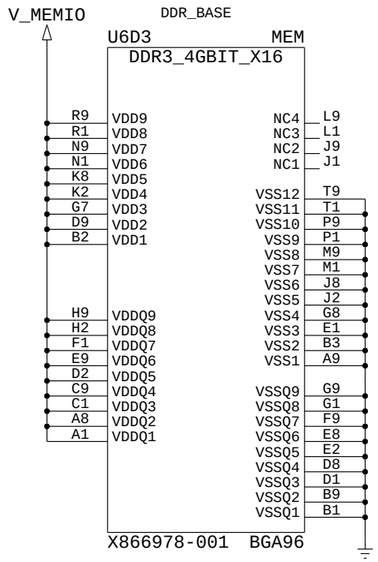


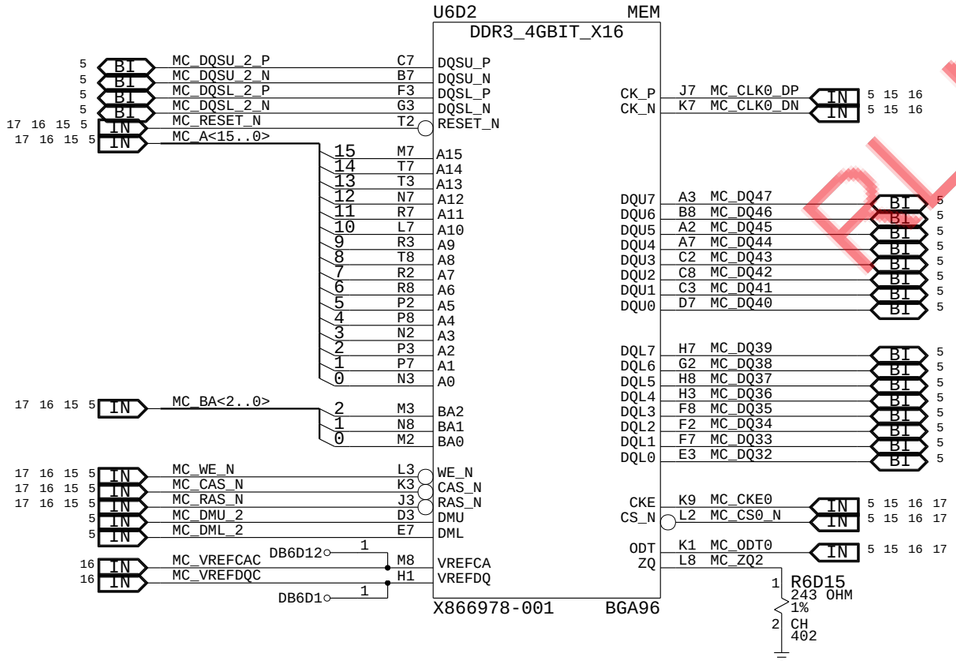
BYTE LANE 4
BYTE LANE 5

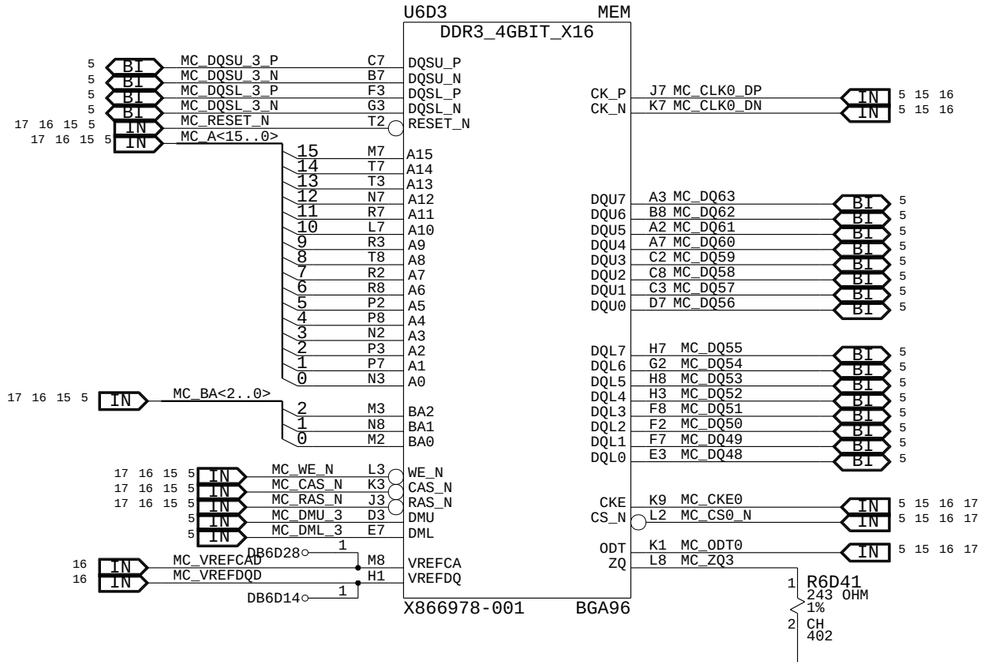


BYTE LANE 6
BYTE LANE 7





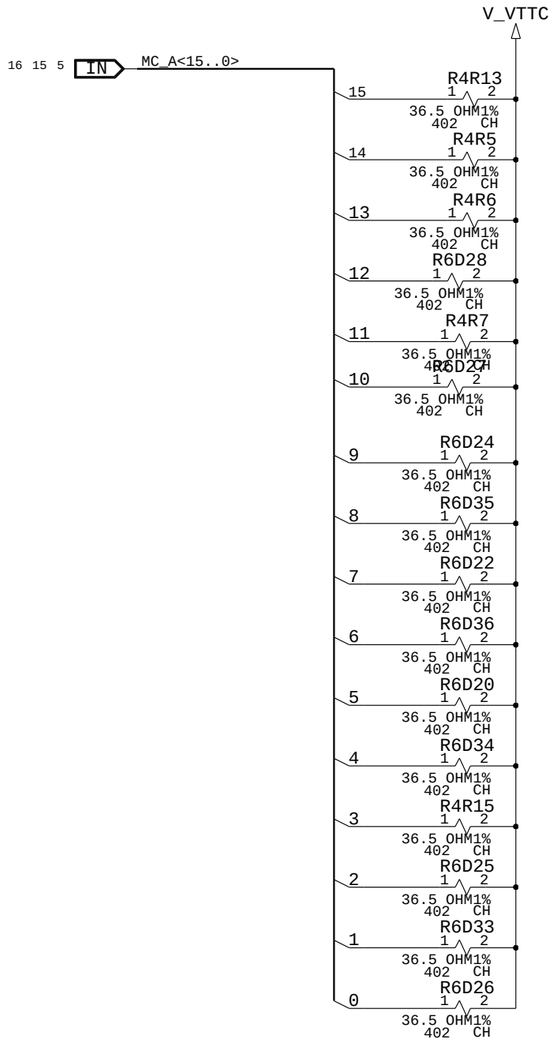


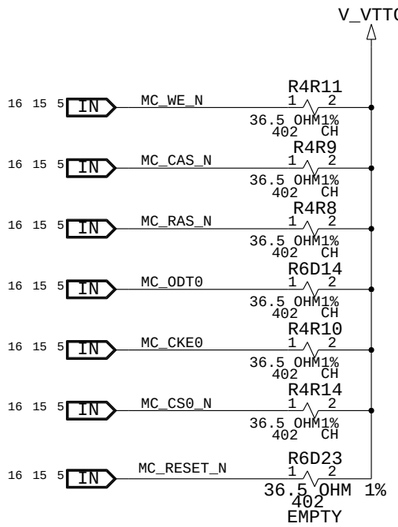


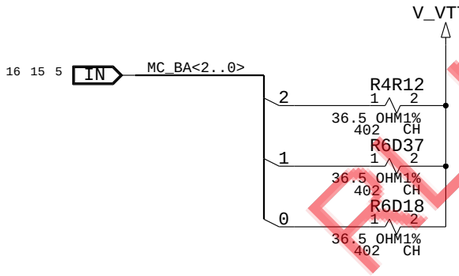
RL Network

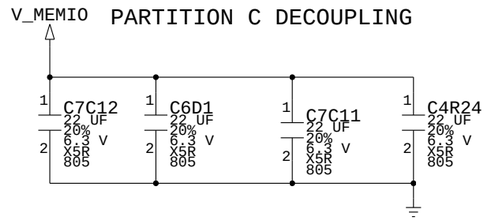
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	16/72	16/72	G	1.01

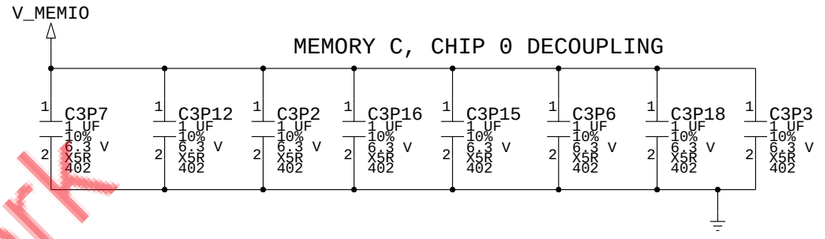
MEMORY: CHANNEL C,DECOUPLING & TERMINATION

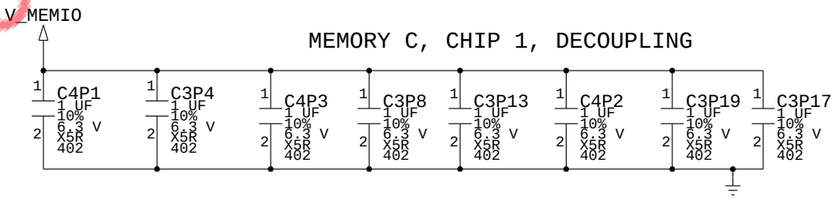


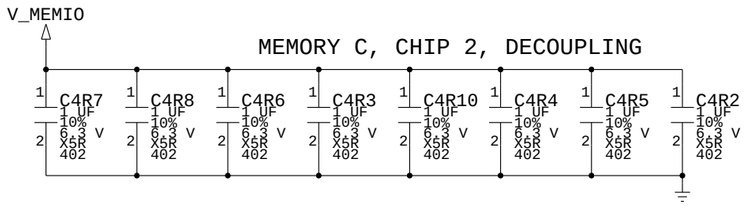


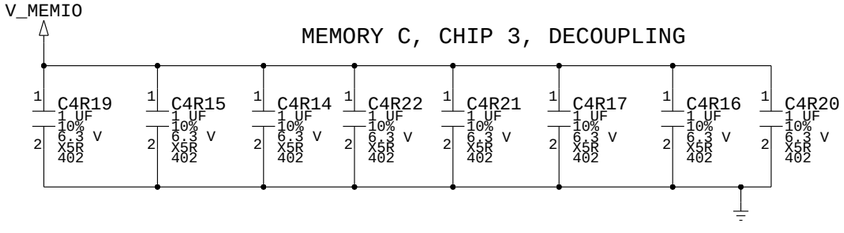












FE Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	17/72	17/72	G	1.01

MEMORY: CHANNEL B

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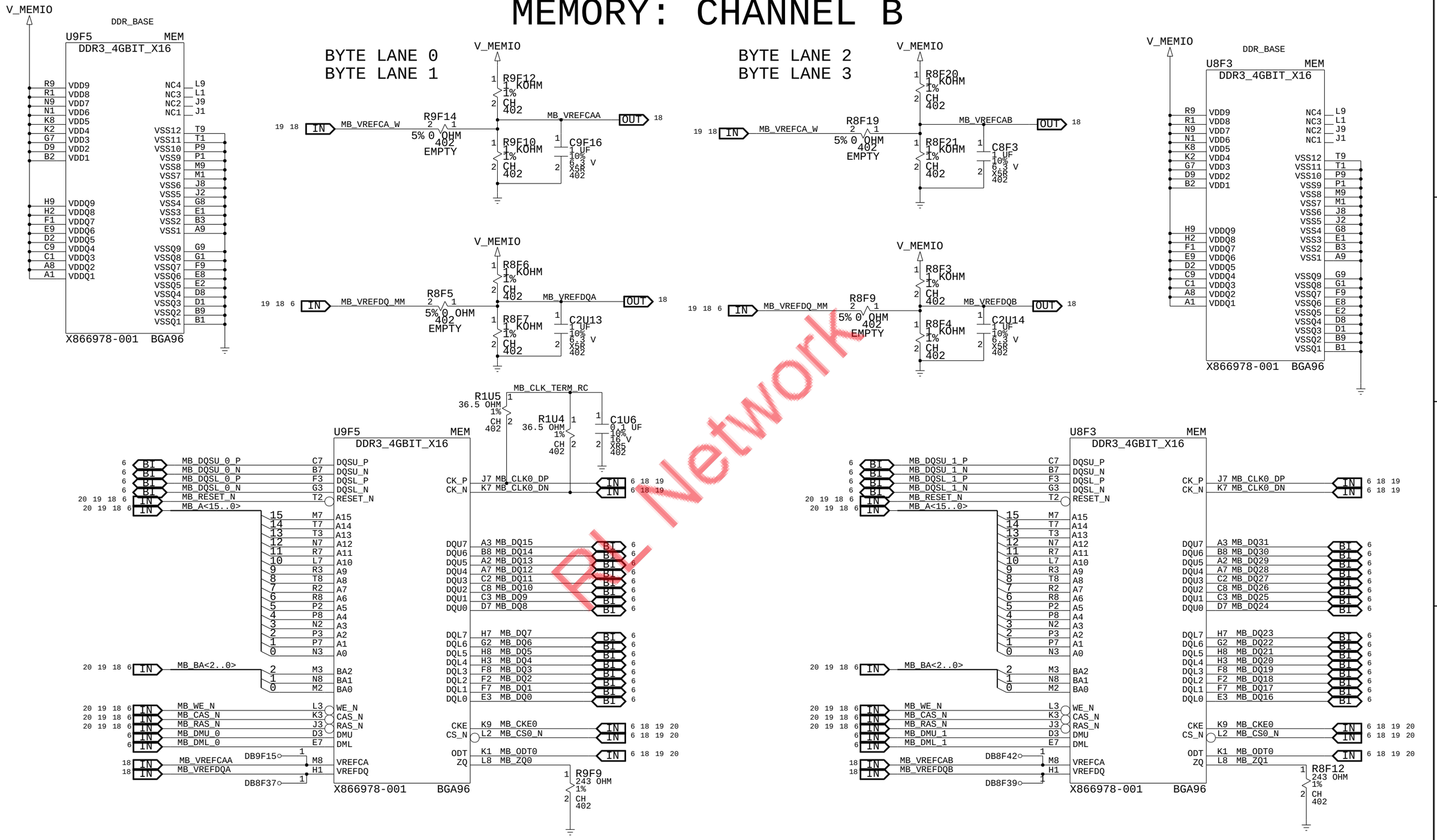
BYTE LANE 1

BYTE LANE 2
BYTE LANE 3

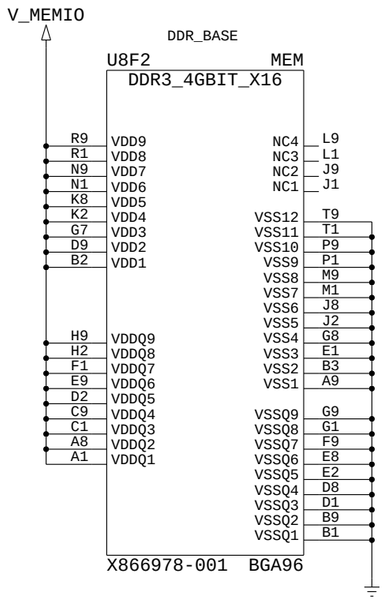


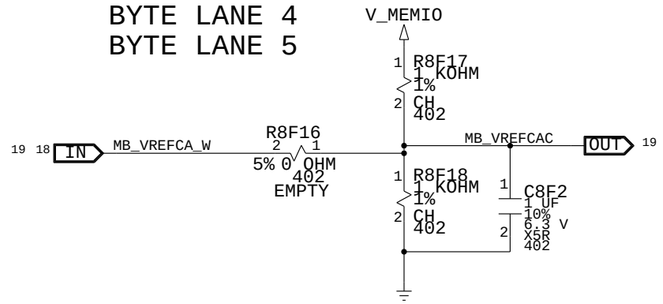
Boardview Network

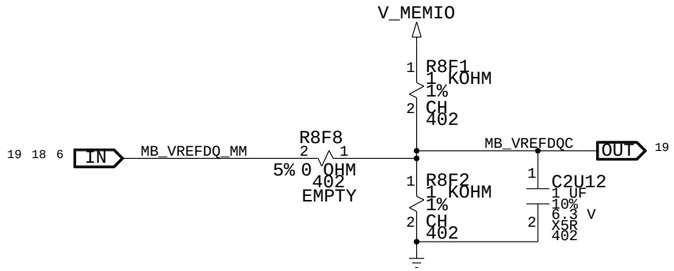
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	18/72	18/72	G	1.01

MEMORY: CHANNEL B

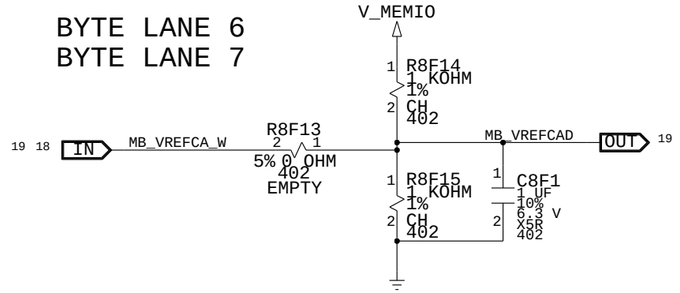
BYTE LANE 4
BYTE LANE 5

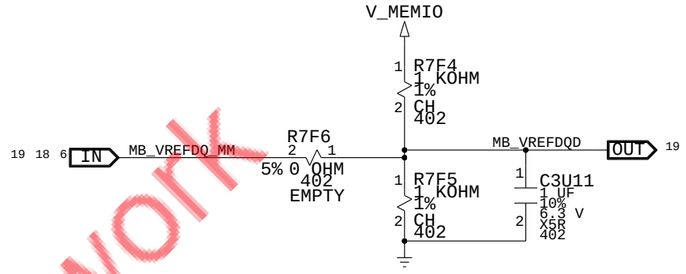


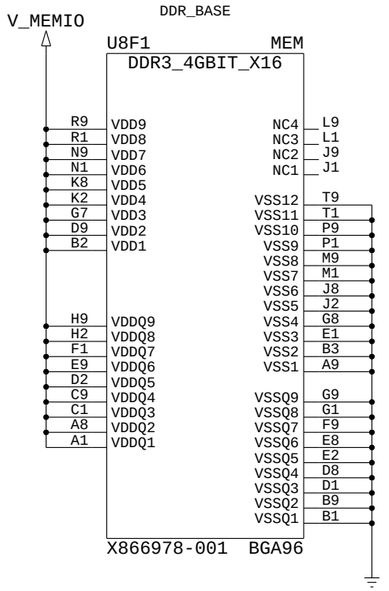


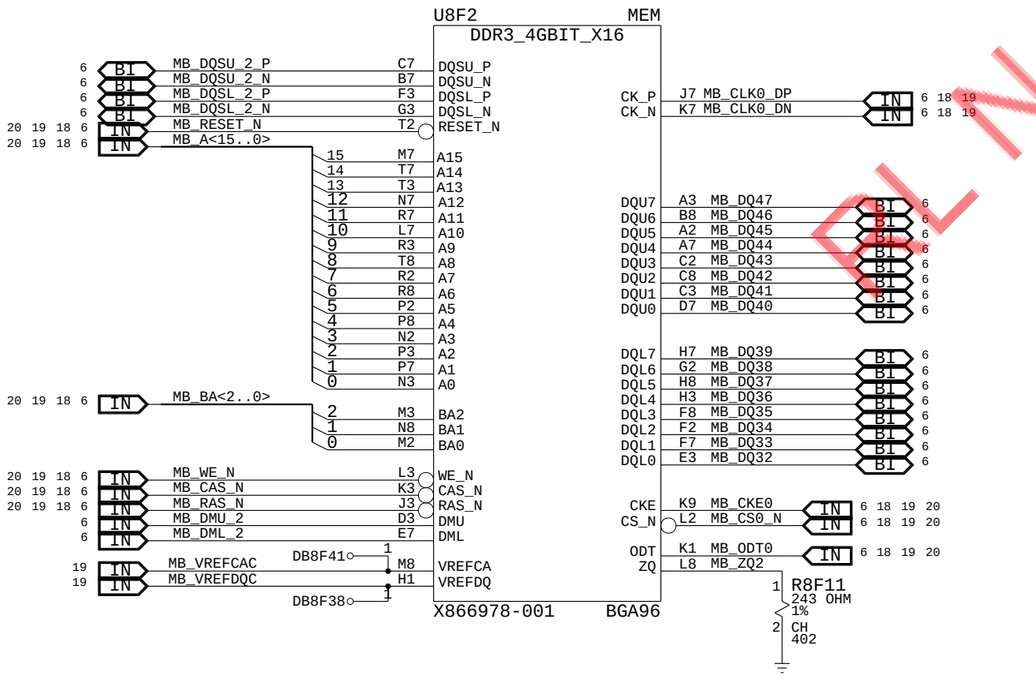


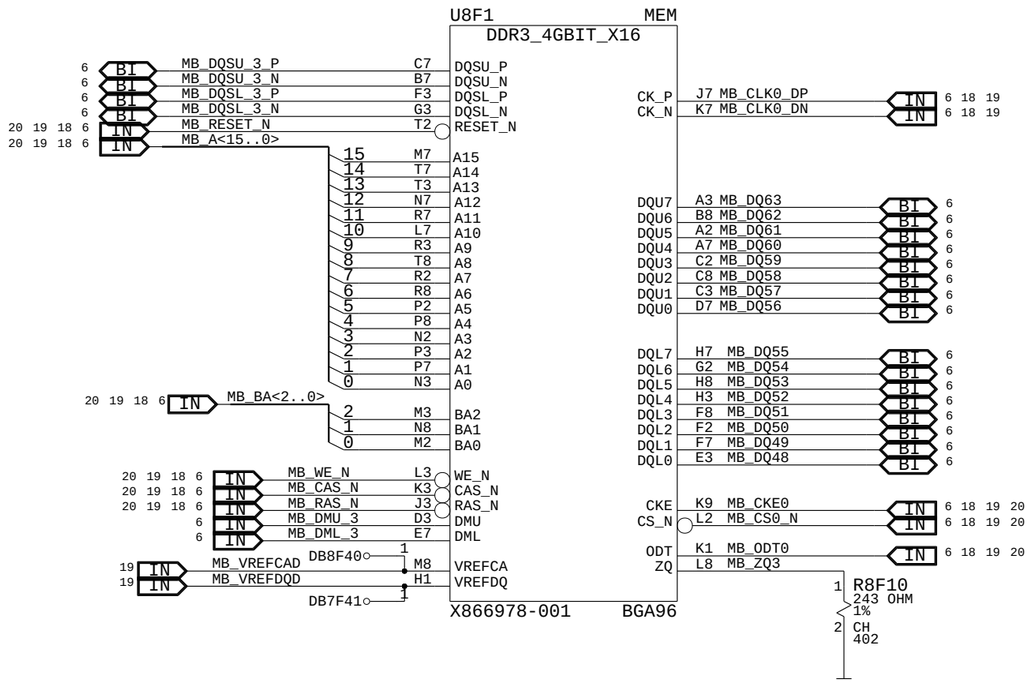
BYTE LANE 6
BYTE LANE 7







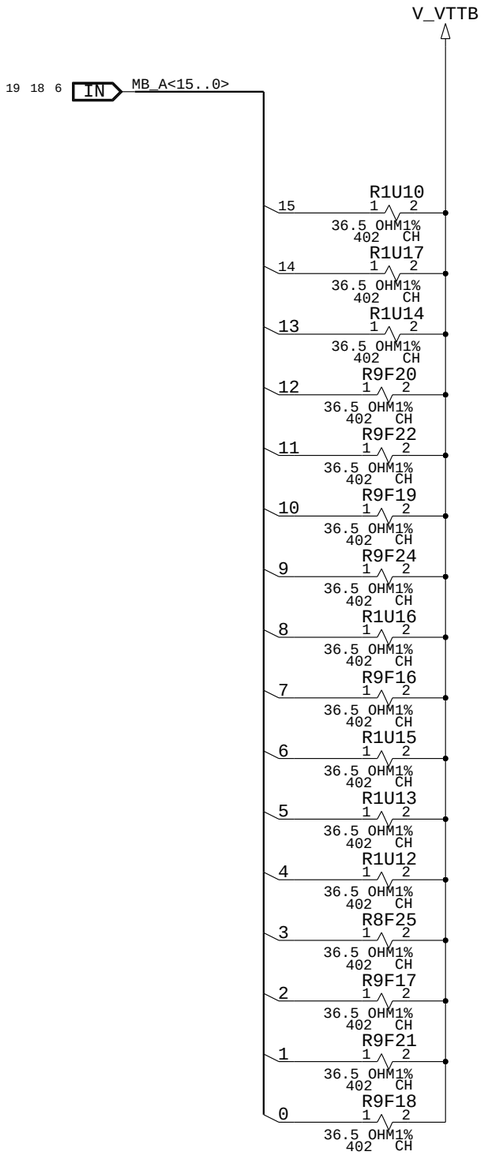


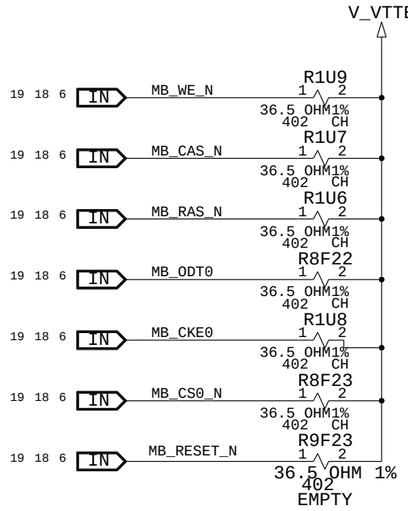


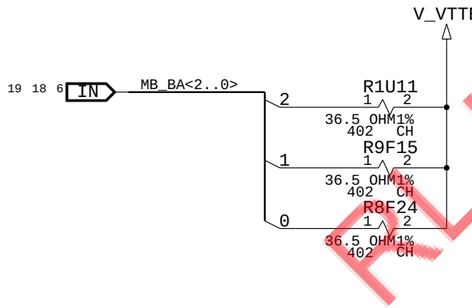
EL Network

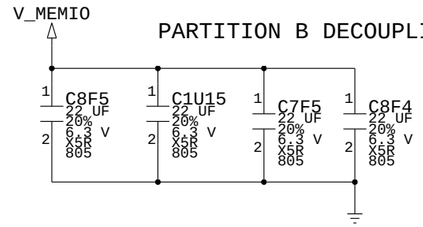
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	19/72	19/72	G	1.01

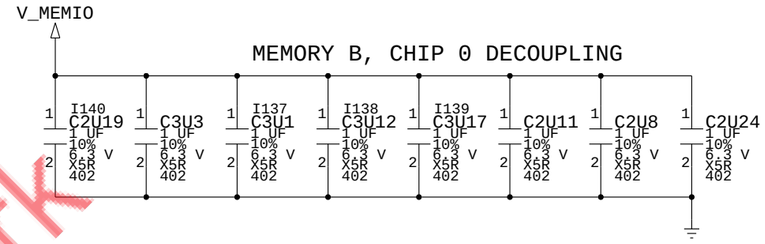
MEMORY: CHANNEL B,DECOUPLING & TERMINATION

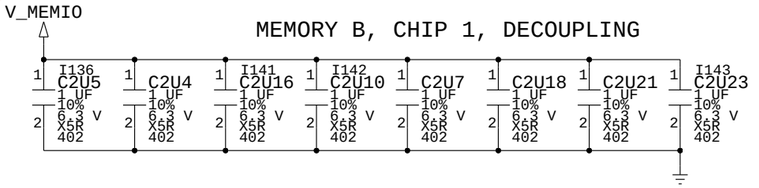


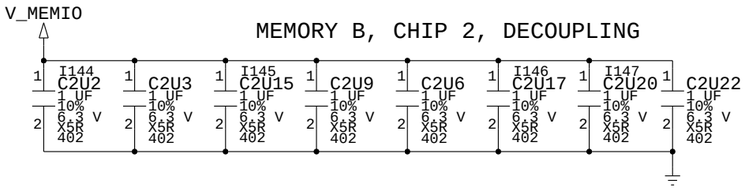


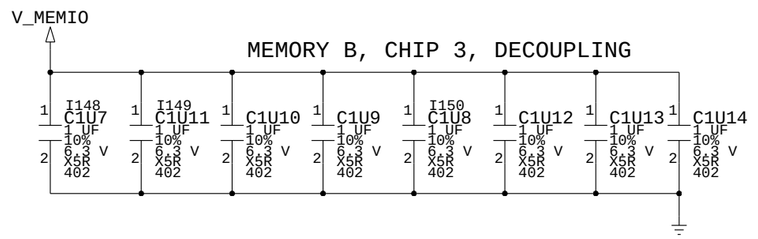












RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	20/72	20/72	G	1.01

MEMORY: CHANNEL A

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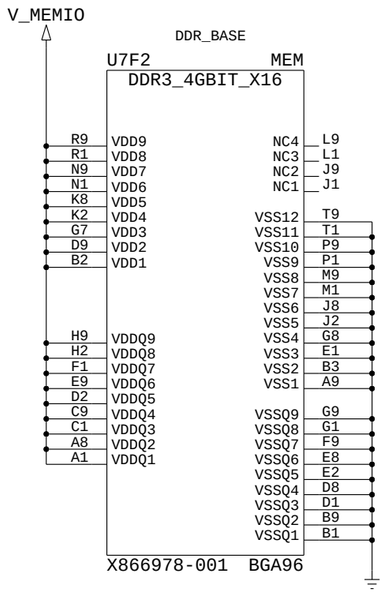
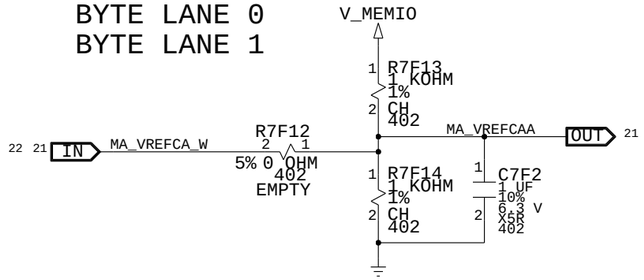
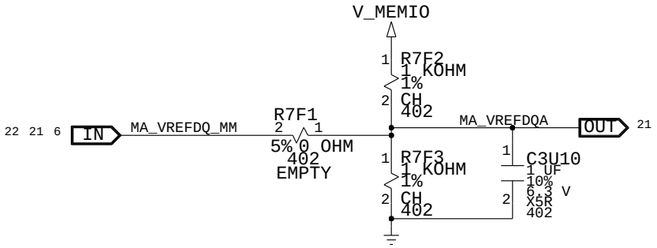
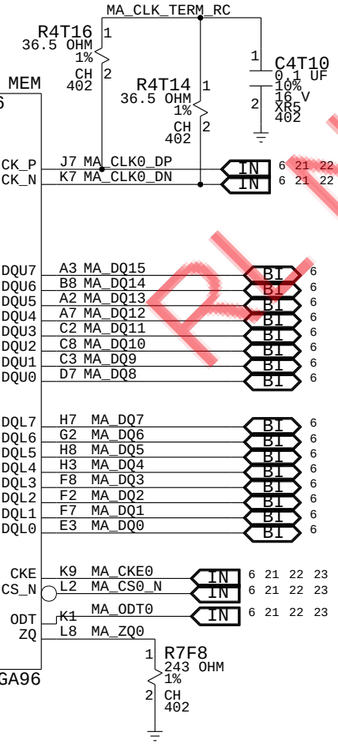
BYTE LANE 1

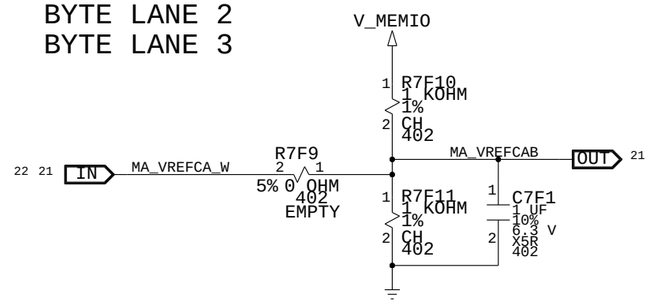


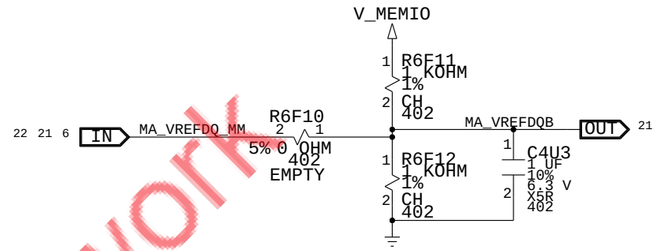


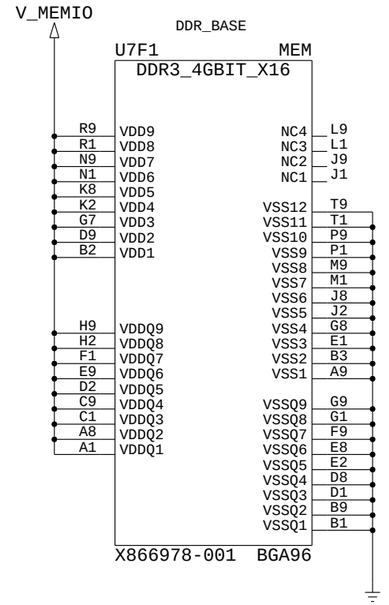


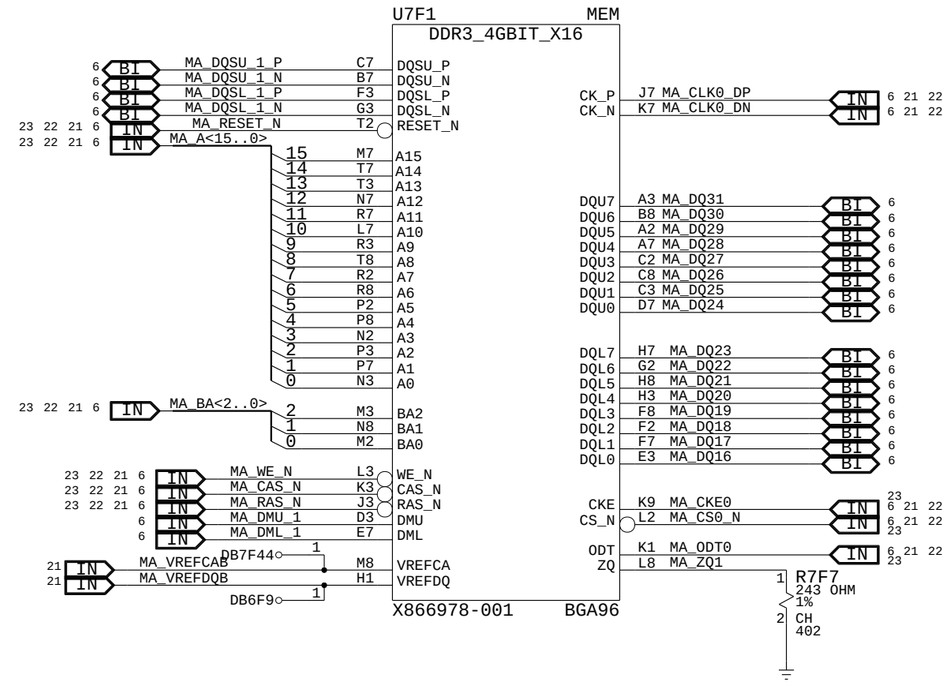


BYTE LANE 2
BYTE LANE 3







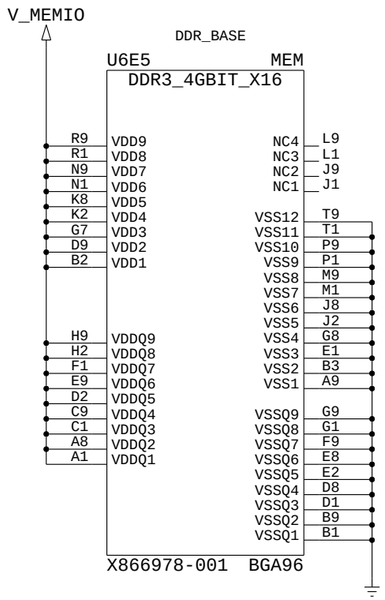


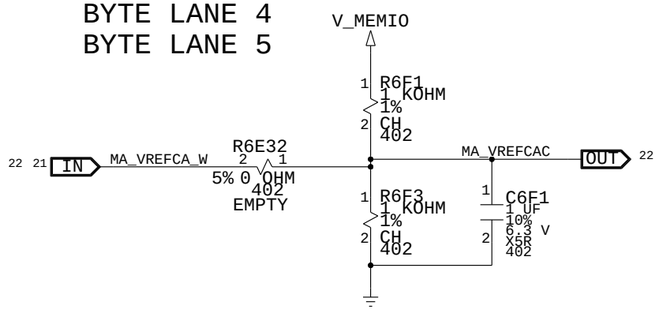
RL Network

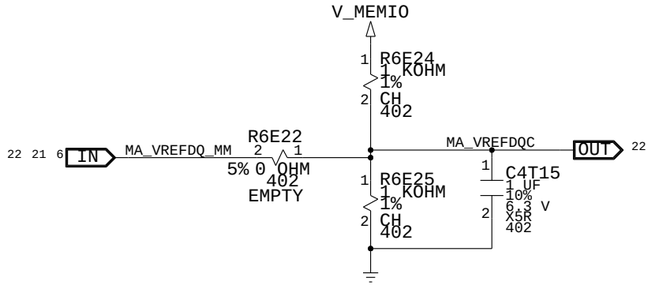
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	21/72	21/72	G	1.01

MEMORY: CHANNEL A

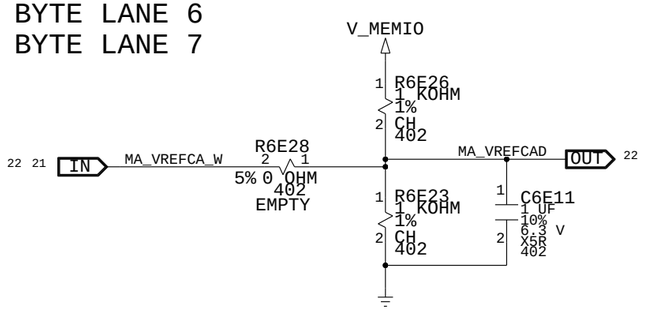
BYTE LANE 4
BYTE LANE 5

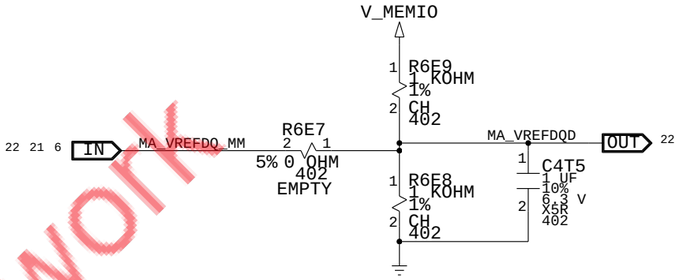


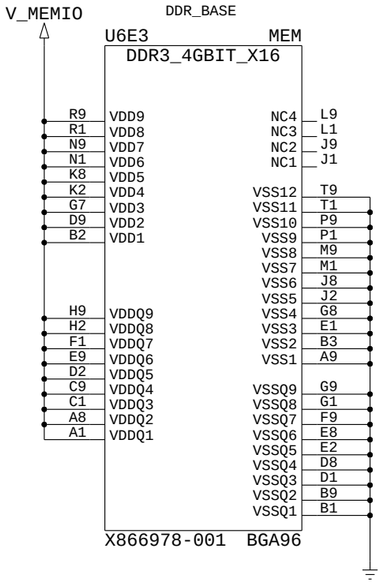


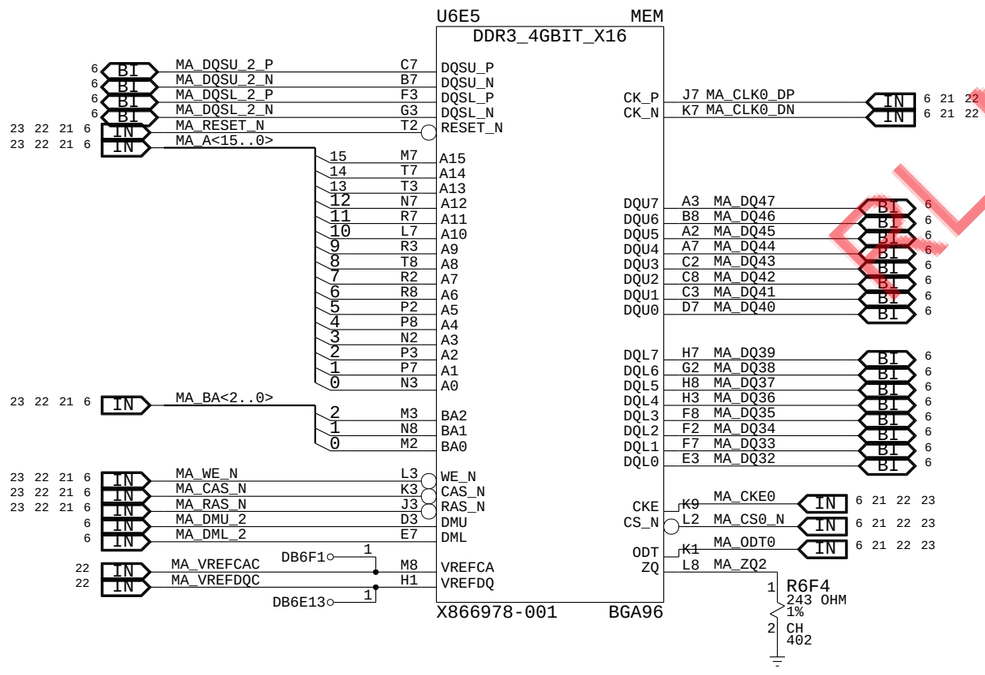


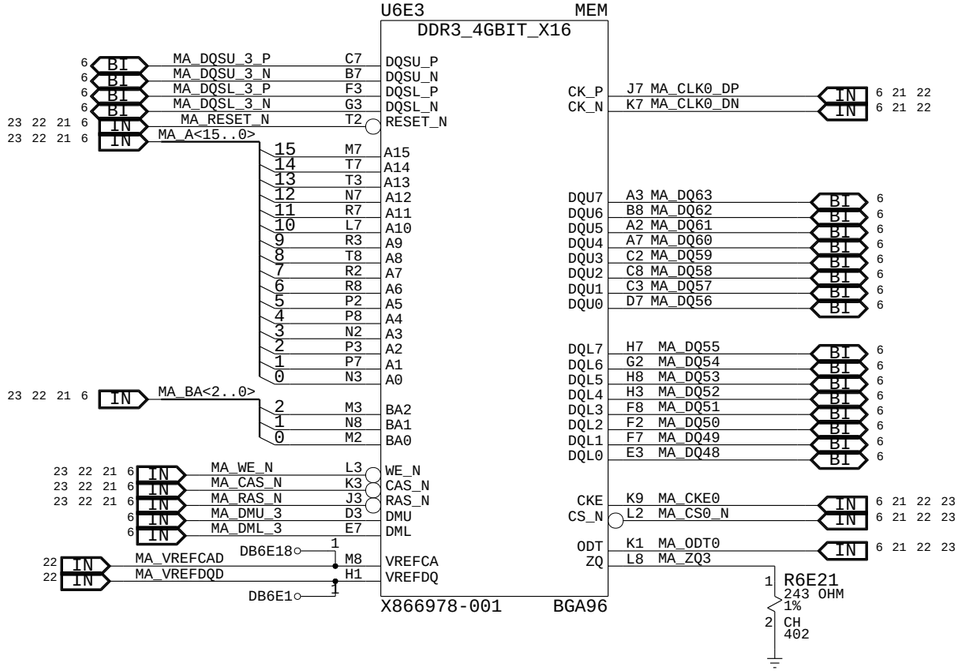
BYTE LANE 6
BYTE LANE 7







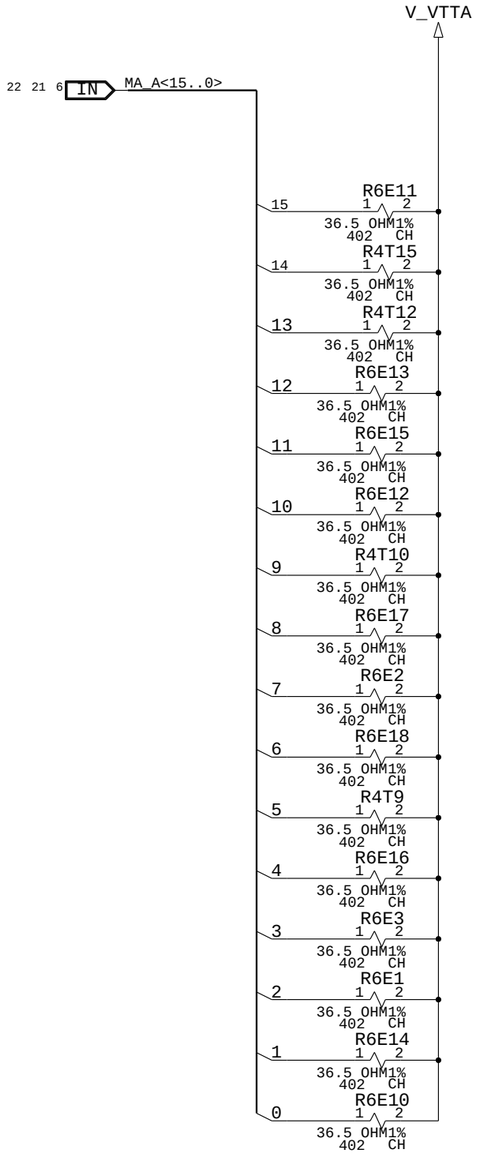


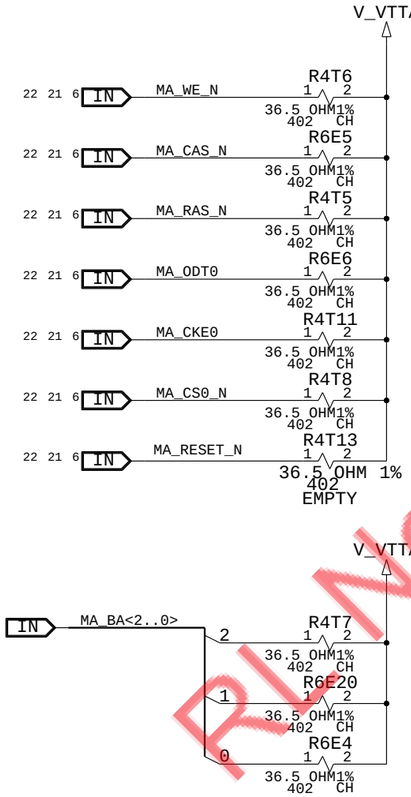


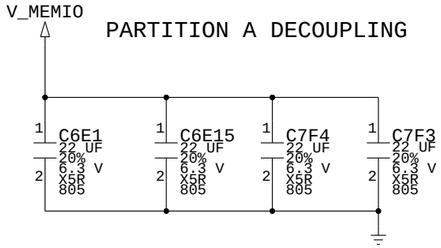
AMD Network

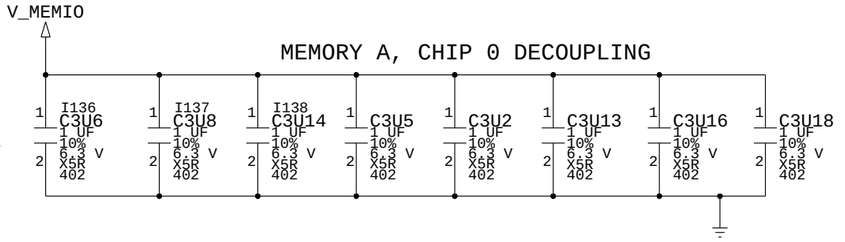
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	22/72	22/72	G	1.01

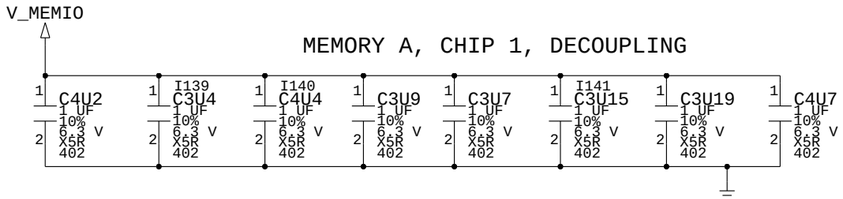
MEMORY: CHANNEL A,DECOUPLING & TERMINATION

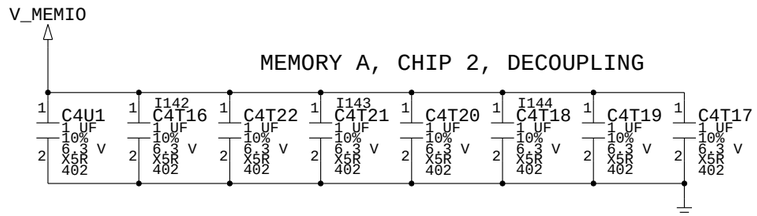


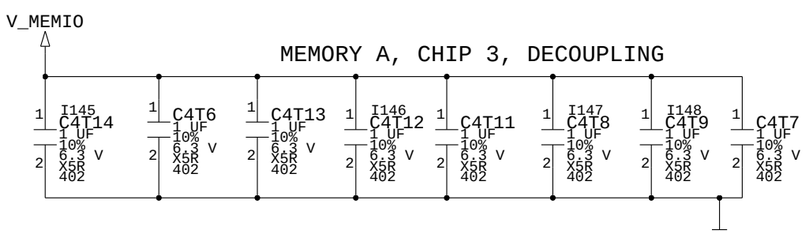












RU Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	23/72	23/72	G	1.01

KIC: USB

U4D2 KIC IC
6 of 11

				USBD_D0_DP	AF8	USB2_WIFI_DP	BI	36	WIFI
				USBD_D0_DN	AE8	USB2_WIFI_DN	BI	36	
				USBC_D0_DP	AC4	USB2_AUX_DP	BI	35	REAR 0
				USBC_D0_DN	AC3	USB2_AUX_DN	BI	35	
REAR 0	35 IN	USB3_AUX_RP	Y1 USBC_D1_RXP	USBC_D1_TXP	W3 USB3_AUX_TP_C	C6B12 0.1 UF 10% 16 V XR5 402	USB3_AUX_TP	OUT 35	
	35 IN	USB3_AUX_RN	Y2 USBC_D1_RXN	USBC_D1_TXN	W4 USB3_AUX_TN_C	C6B11 0.1 UF 10% 16 V XR5 402	USB3_AUX_TN	OUT 35	
REAR 1	35 IN	USB3_BP_P1_RP	V1 USBB_D2_RXP	USBB_D2_TXP	U3 USB3_BP_P1_TP_C	C6B8 0.1 UF 10% 16 V XR5 402	USB3_BP_P1_TP	OUT 35	REAR 1
	35 IN	USB3_BP_P1_RN	V2 USBB_D2_RXN	USBB_D2_TXN	U4 USB3_BP_P1_TN_C	C6B7 0.1 UF 10% 16 V XR5 402	USB3_BP_P1_TN	OUT 35	
				USBB_D0_DP	AE4	USB2_BP_P1_DP	BI	35	
				USBB_D0_DN	AE3	USB2_BP_P1_DN	BI	35	
				USBB_D1_DP	AD2	USB2_BP_P0_DP	1 DB4D19		NOT USED
				USBB_D1_DN	AD1	USB2_BP_P0_DN	1 DB4D20		
NOT USED	DB4D17 1	USB3_BP_P0_RP	T1 USBB_D3_RXP	USBB_D3_TXP	R3	USB3_BP_P0_TP	1 DB4D21		
	DB4D18 1	USB3_BP_P0_RN	T2 USBB_D3_RXN	USBB_D3_TXN	R4	USB3_BP_P0_TN	1 DB4D22		
				USBA_D2_TXP	AB10 USB3_FP_P0_TP_C	C4F14 0.1 UF 10% 16 V XR5 402	USB3_FP_P0_TP	OUT 35	FRONT
FRONT	35 IN	USB3_FP_P0_RP	AA8 USBA_D2_RXP	USBA_D2_TXN	AB9 USB3_FP_P0_TN_C	C4F15 0.1 UF 10% 16 V XR5 402	USB3_FP_P0_TN	OUT 35	
	35 IN	USB3_FP_P0_RN	AA7 USBA_D2_RXN	USBA_D0_DP	AC7		USB2_FP_P0_DP	BI 35	
				USBA_D0_DN	AC8		USB2_FP_P0_DN	BI 35	
				USBA_D1_DP	AF6		USB2_ACC_DP	BI 41	FRONT PANEL ACC
				USBA_D1_DN	AF5		USB2_ACC_DN	BI 41	
NOT USED	DB4C10 1	USB3_ACC_RP	AB1 USBA_D3_RXP	USBA_D3_TXP	AA3		USB3_ACC_TP	1 DB4C12	NOT USED
	DB4C11 1	USB3_ACC_RN	AB2 USBA_D3_RXN	USBA_D3_TXN	AA4		USB3_ACC_TN	1 DB4C13	
				USBA_D2_AMOUT	AA5 USBA_D2_AMOUNT 1			DB6R2	
				USBA_D1_AMOUT	AE6 USBA_D1_AMOUNT 1			DB4D7	
				USBA_D0_AMOUT	AC11 USBA_D0_AMOUNT 1			DB4E3	
				USBB_D2_AMOUT	R5 USBB_D2_AMOUNT 1			DB5R2	
				USBB_D1_AMOUT	AD5 USBB_D1_AMOUNT 1			DB4D12	
				USBB_D0_AMOUT	AF4 USBB_D0_AMOUNT 1			DB4D13	
				USBC_D1_AMOUT	W5 USBC_D1_AMOUNT 1			DB6R1	
				USBC_D0_AMOUT	AC5 USBC_D0_AMOUNT 1			DB6R3	
				USBD_D0_AMOUT	AE9 USBD_D0_AMOUNT 1			DB4E2	
		USBA_D1_TXRTUNE	AB11 USBA_D1_TXRTUNE						

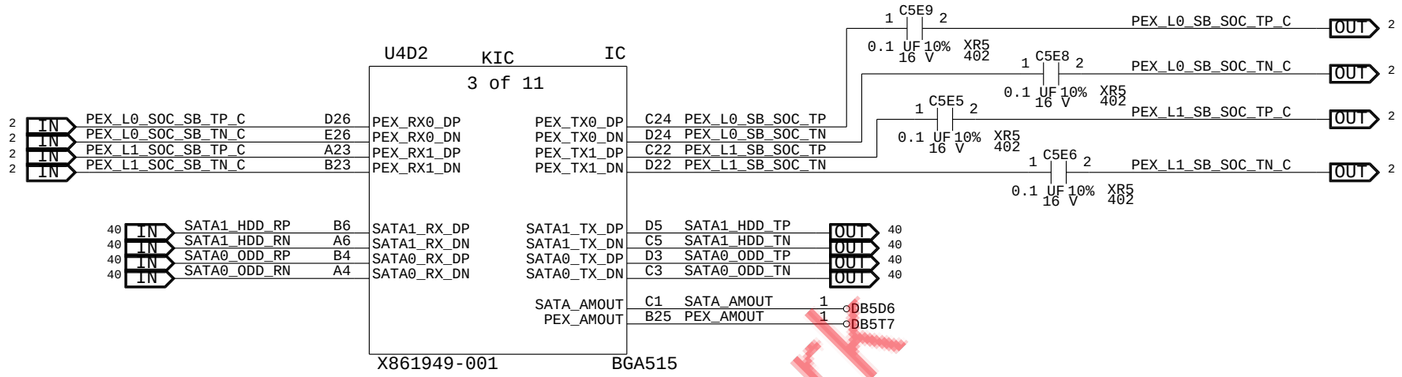
1 R6T1 174 OHM 1% 2 CH 402

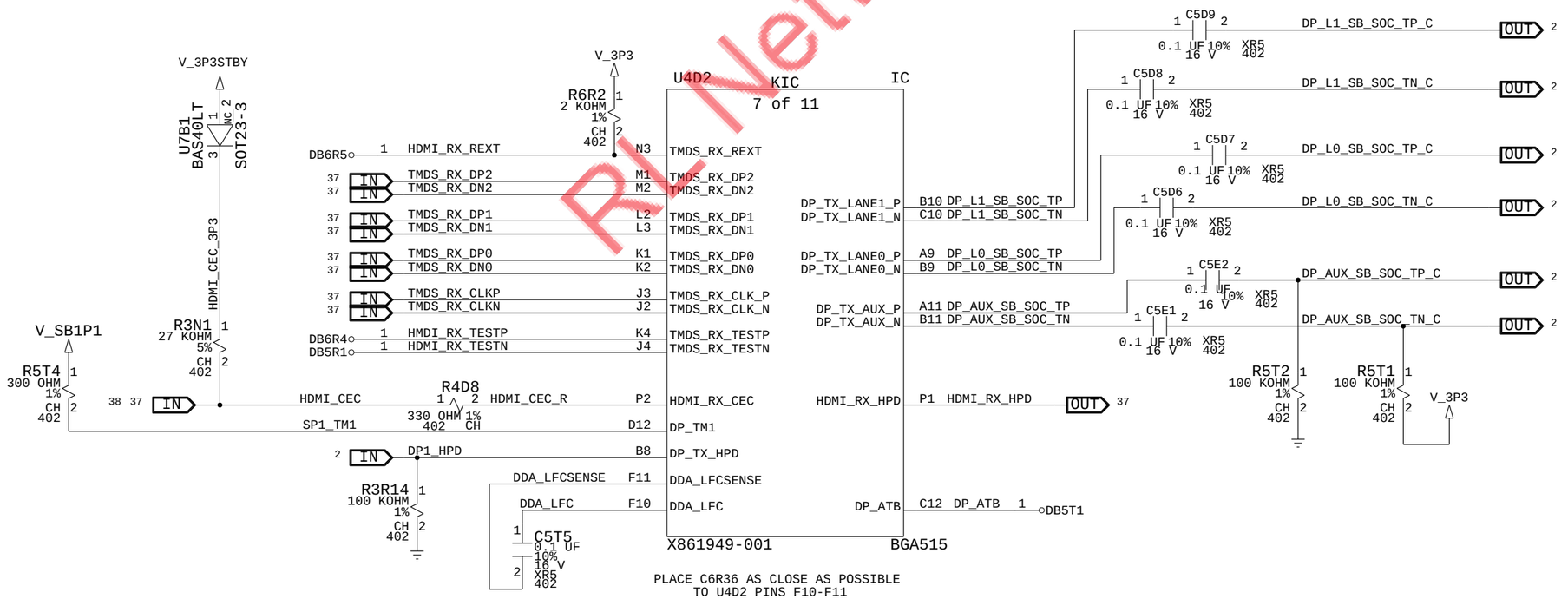
X861949-001 BGA515

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	24/72	24/72	G	1.01

KIC: PCIEX,SATA,VIDEO

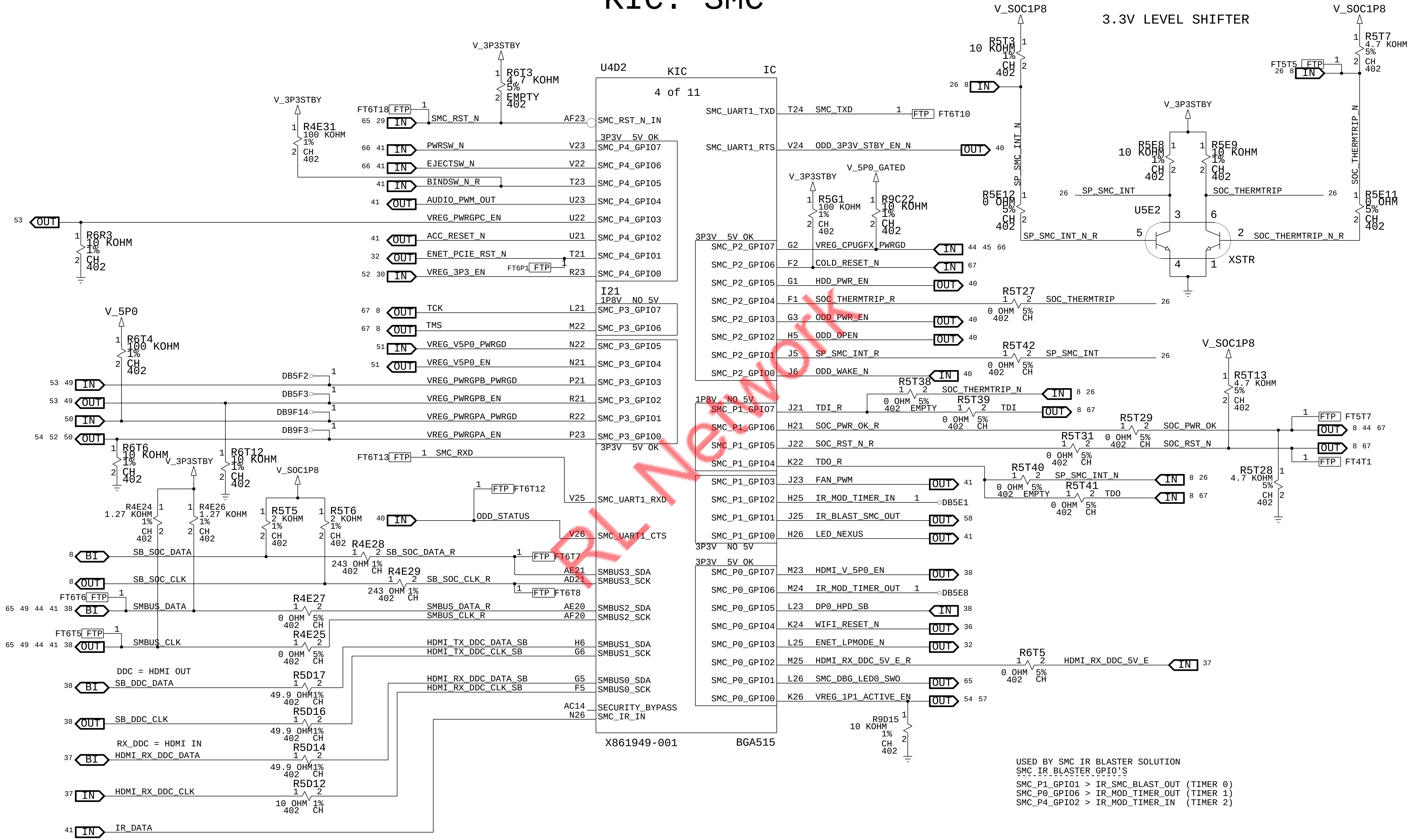




RI Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	25/72	25/72	G	1.01

KIC: SMC



USED BY SMC IR BLASTER SOLUTION

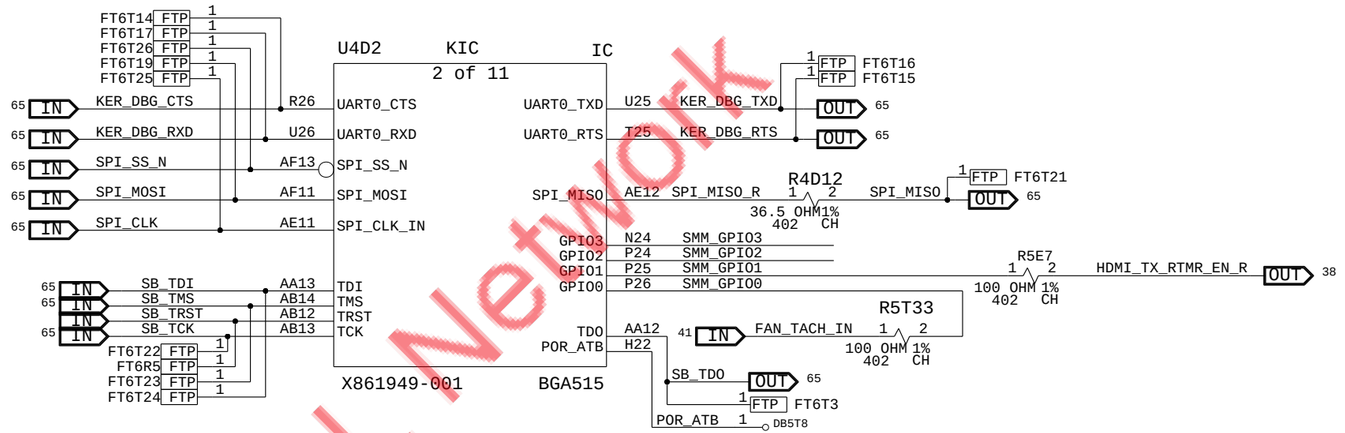
SMC_IR_BLASTER_GPIO'S

SMC_P1_GPIO1 > IR_SMC_BLAST_OUT (TIMER 0)
SMC_P0_GPIO6 > IR_MOD_TIMER_OUT (TIMER 1)
SMC_P4_GPIO2 > IR_MOD_TIMER_IN (TIMER 2)

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	26/72	26/72	G	1.01

RL Network

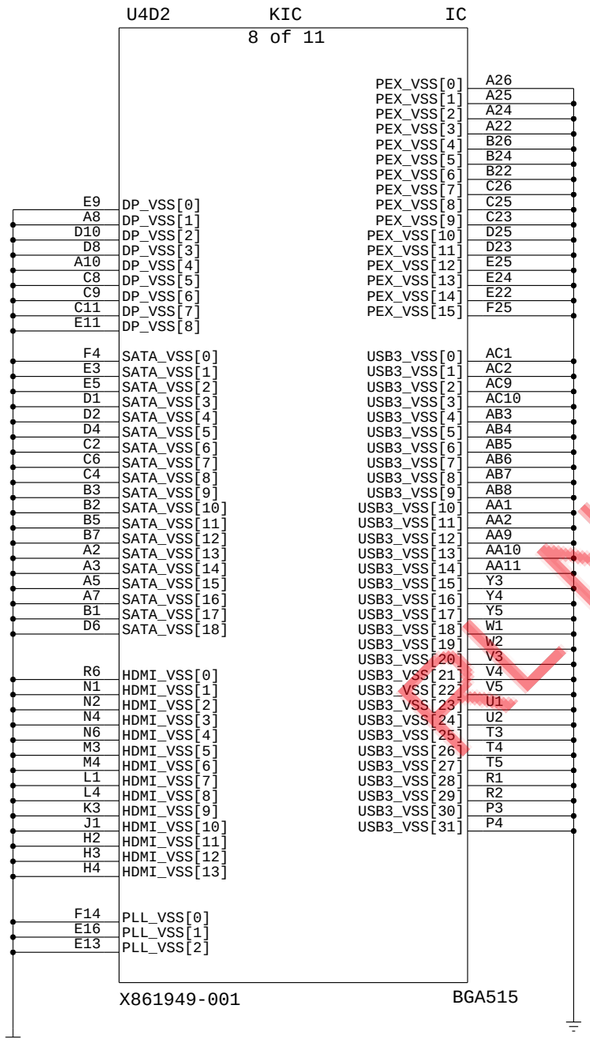
KIC: FACET

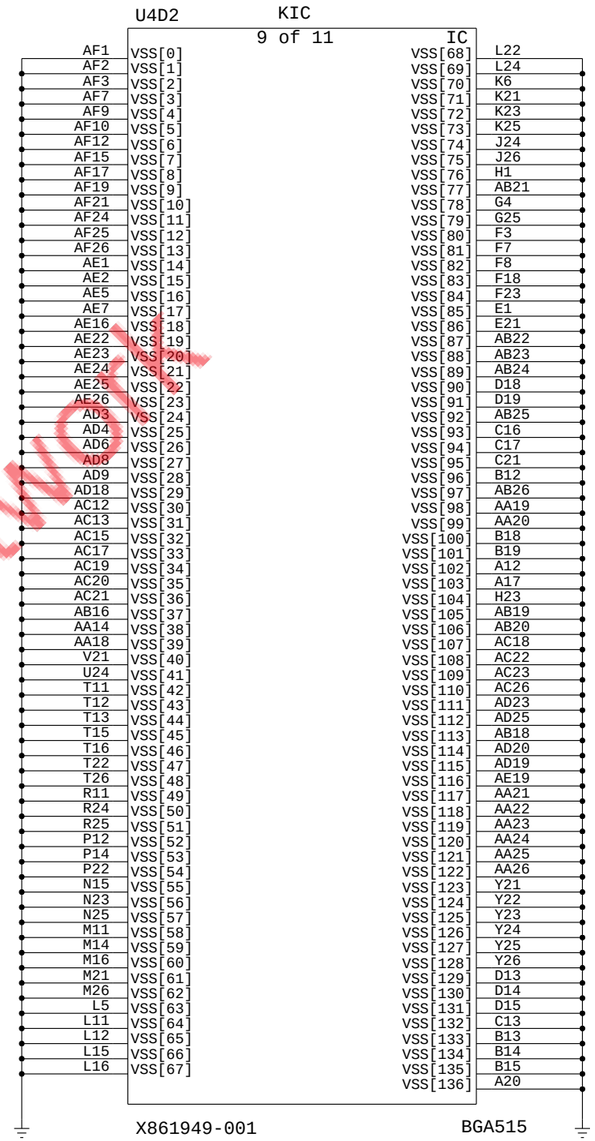


RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	27/72	27/72	G	1.01

KIC: POWER





Intel Confidential

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	28/72	28/72	G	1.01

KIC: CLOCKS,STRAPPING,POR

SEE PAGE 32 FOR ADDITIONAL INFORMATION
100 MHZ CLOCK ENABLE AND ROUTING

32 IN PEX_REF_CLK1_REQN_R

R4B3 0 OHM 5% 402 CH

V_3P3

R4C26 100 KOHM 5% 2 EMPTY 402

R4B10 100 KOHM 5% 2 EMPTY 402

R5T14 100 KOHM 1% 2 CH 402

R5T15 100 KOHM 5% 2 EMPTY 402

V_1P8STBY

KIC_BASE

U4D2 KIC 1 of 11 IC

		G22	V_VDD18_DET	
PEX_REF_CLK1_REQN	C18	PEX_REF_CLK1_REQN	V_EXT_DET	G21 V_EXT_DET
PEX_REF_CLK2_REQN	C19	PEX_REF_CLK2_REQN	V_EXT_OK	F22 V12P0_PWRGD
		AD22	VPGM	
DB5T2 BKUP_SB_SYNC_CLKP	E18	100M_SYNC_CLK_BYPASS_DP	SMC_RST_N_OUT	AF22 SMC_RST_N_OUT_R
DB5T3 BKUP_SB_SYNC_CLKN	E19	100M_SYNC_CLK_BYPASS_DN	I27	
			CLK_MONITOR	E17 SB_CLK_MONITOR
SMC_XTAL_OUT	A18	XTAL_CLK_OUT	RTC_CLK_OUT	A21 RTC_CLK_OUT
SMC_XTAL_IN	A19	XTAL_CLK_IN	EMMC_CLK	AC16 MMC_CLK
		AD24	ENET_REF_CLK	C20 ENET_REF_CLK
SMC_BYPASS_CLK_IN	D21	SMC_BYPASS_CLK_IN	SOC_NS_SYNC_CLK_DP	B16 SOC_SYNC_NS_100M_CLKP
			SOC_NS_SYNC_CLK_DN	B17 SOC_SYNC_NS_100M_CLKN
			SOC_NS_AV_CLK_DP	A13 SOC_AV_NS_100M_CLKP
			SOC_NS_AV_CLK_DN	A14 SOC_AV_NS_100M_CLKN
BKUP_SB_PEX_REF_CLKP	E20	PCIE_BYPASS_CLK_DP	PEX_REF_CLK2_DP	B20 SOC_NB_PEX_SS_100M_CLKP
BKUP_SB_PEX_REF_CLKN	D20	PCIE_BYPASS_CLK_DN	PEX_REF_CLK2_DN	B21 SOC_NB_PEX_SS_100M_CLKN
DB5T4 250M_CLK_BYPASS_DP	F20	250M_CLK_BYPASS_DP	PEX_REF_CLK1_DP	C14 ENET_PEX_SS_100M_CLKP
DB5T6 250M_CLK_BYPASS_DN	F21	250M_CLK_BYPASS_DN	PEX_REF_CLK1_DN	C15 ENET_PEX_SS_100M_CLKN
DB5T10 BKUP_SB_AV_CLKP	D16	AV_CLK_BYPASS_DP	PEX_REF_CLK0_DP	A15 SOC_PEX_SS_100M_CLKP
DB5T9 BKUP_SB_AV_CLKN	D17	AV_CLK_BYPASS_DN	PEX_REF_CLK0_DN	A16 SOC_PEX_SS_100M_CLKN

X861949-001 BGA515

SMC_XTAL_OUT R5E2 249 KOHM 1% 402 CH

R5E1 1 KOHM 1% 402 CH SMC_XTAL_OUT_R

SMC_XTAL_IN

Y5D1 25 MHZ SM XTAL

C5E3 30 PF 5% 50 V NPO 402

C5E4 30 PF 5% 50 V NPO 402

R5E5 49.9 OHM 1% EMPTY 402

R5T17 10 KOHM 1% 402 CH SMC_BYPASS_CLK_IN

V_12P0_GATED

C5T27 1 UF 10% 16 V X5R 603

R5T26 11.3 KOHM 1% 2 CH 402 R5T26/V_EXT_DET IS NOW CONNECTED TO V_12P0_GATED

R5T18 1.13 KOHM 1% 2 CH 402

OUT 53 DB5T5

DB5E5

DB5E6 KEEP DB55E5 AND DB5E6 CLOSE TO EACH OTHER IN LAYOUT

R4E30 1 KOHM 1% 402 CH SMC_RST_N OUT 26 65

C4E3 270 PF 10% 50 V X7R 402

RTC_RETAIL R5E4 0 OHM 5% 402 CH X32K_X2_R OUT 8

R5E6 69.8 KOHM 1% 2 EMPTY 402

R5T16 100 OHM 1% 402 CH PEX_XTAL2 OUT 32

OUT 33

OUT 2 (SOC_SYNC_NS_100M_CLKP)

OUT 2 (SOC_SYNC_NS_100M_CLKN)

OUT 2 (SOC_AV_NS_100M_CLKP)

OUT 2 (SOC_AV_NS_100M_CLKN)

OUT 2 (SOC_NB_PEX_SS_100M_CLKP)

OUT 2 (SOC_NB_PEX_SS_100M_CLKN)

OUT 32 (ENET_PEX_SS_100M_CLKP)

OUT 32 (ENET_PEX_SS_100M_CLKN)

OUT 2 (SOC_PEX_SS_100M_CLKP)

OUT 2 (SOC_PEX_SS_100M_CLKN)

DEBUG
CONN J5F3
MINI RF
GND1 GND2 IO1
X864758-001 SM

DEBUG
CONN J5E2
MINI RF
GND1 GND2 IO1
X864758-001 SM

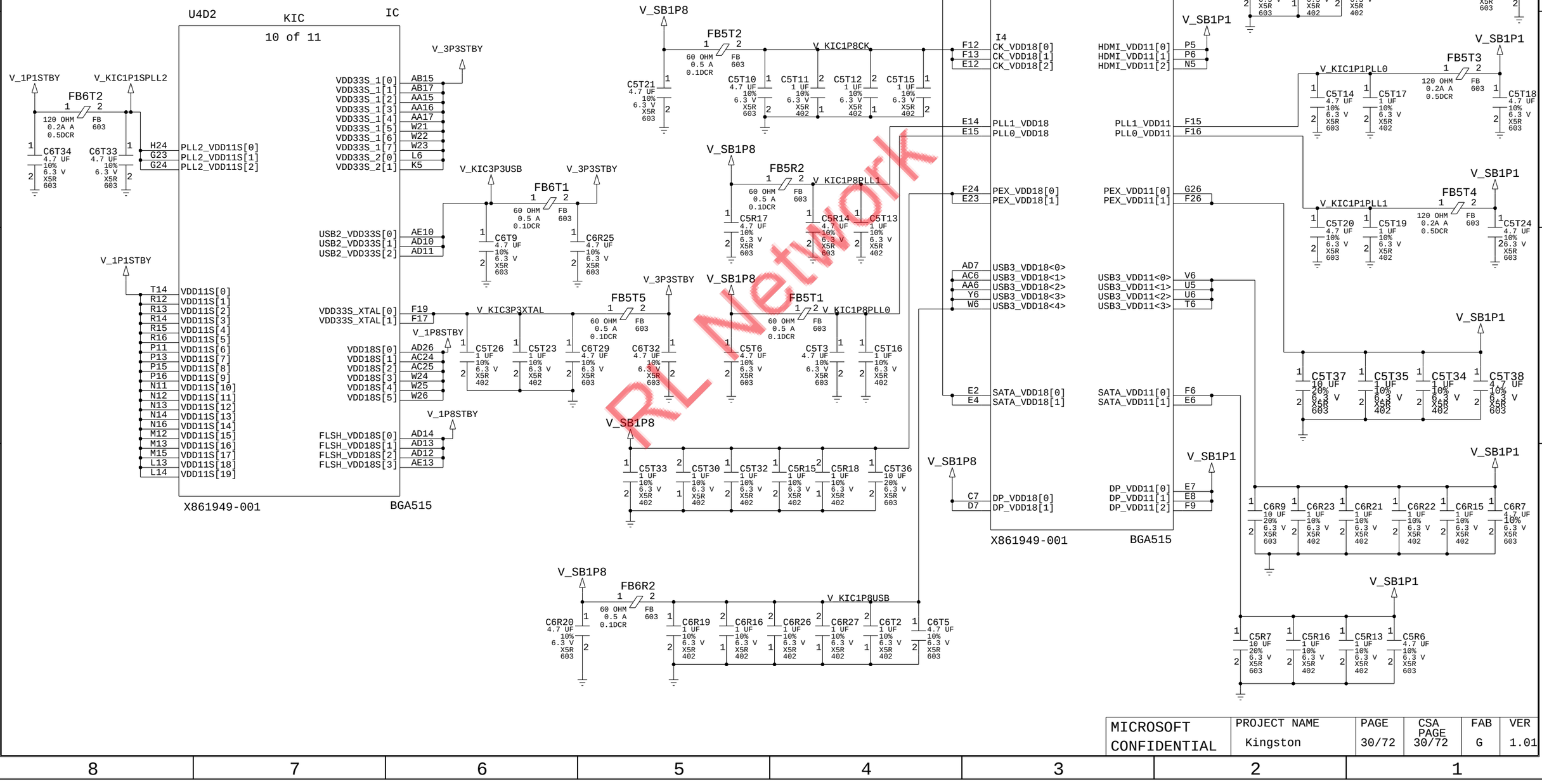
ULTRA MINIATURE COAX
TO SMA CABLE ASSEMBLY
DIGIKEY PN: 931-1098-ND

RU Network

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X861949-005	IC	U4D2	IC,KRAKEN SB,BGA515	KIC_RETAIL
X861949-003	IC	U4D2	IC,KRAKEN SB,BGA515	KIC_DEV

KIC: POWER

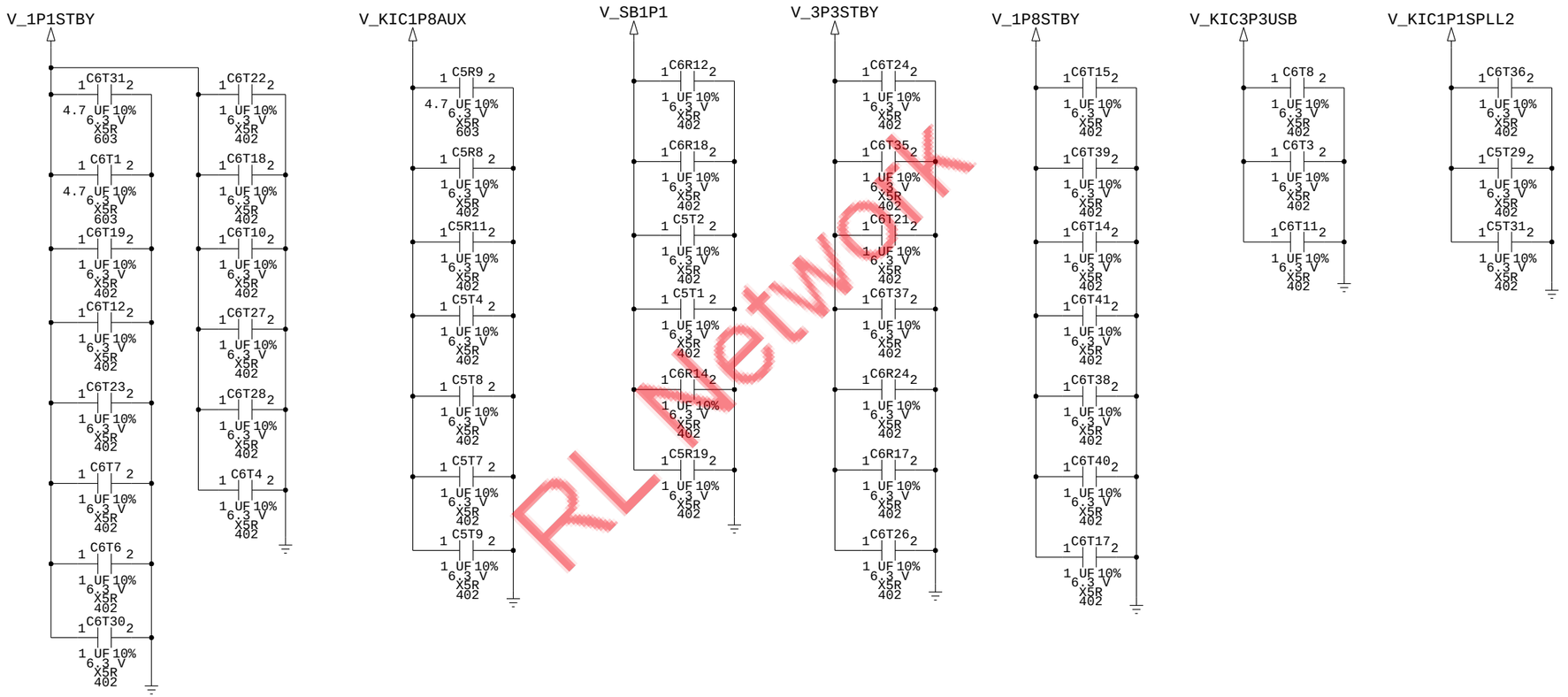
FET PREVENTS LEAKAGE THROUGH KRAKEN
FROM STANDBY RAILS TO 3P3 RAIL



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	30/72	30/72	G	1.01

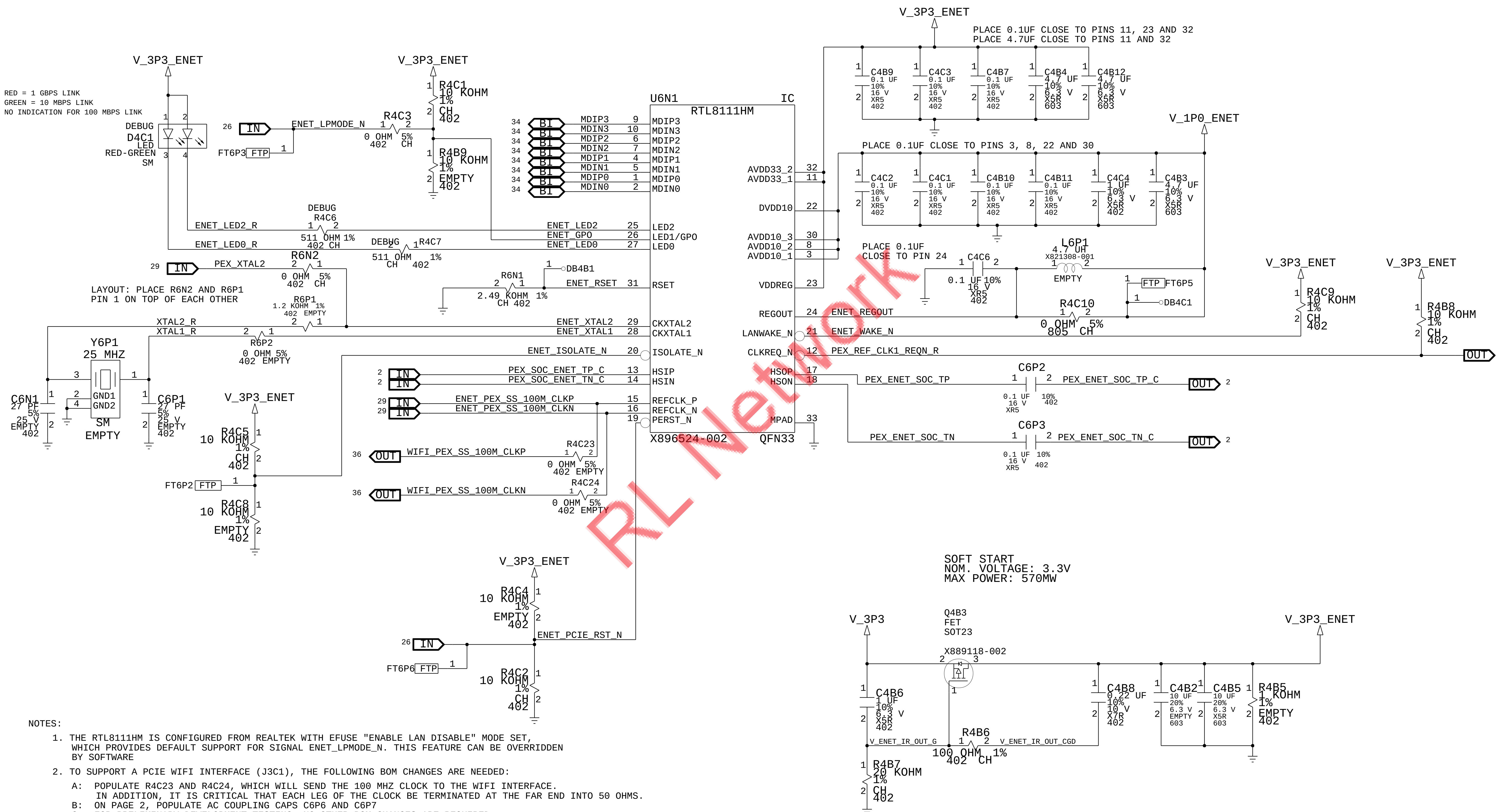
KIC: DECOUPLING



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	31/72	31/72	G	1.01

ETHERNET CONTROLLER



8 7 6 5 4 3 2 1
D C B A
V_3P3_ENET
RED = 1 GBPS LINK
GREEN = 10 MBPS LINK
NO INDICATION FOR 100 MBPS LINK
DEBUG
D4C1
LED
RED-GREEN
SM
ENET_LPMODE_N
R4C3
0 OHM 5%
402 CH
FT6P3 FTP
R4C1
10 KOHM
1%
CH
402
R4B9
10 KOHM
1%
EMPTY
402
U6N1
IC
RTL8111HM
BI
MDIP3 MDIN3 MDIP2 MDIN2 MDIP1 MDIN1 MDIP0 MDIN0
ENET_LED2_R
ENET_LED0_R
DEBUG
R4C6
511 OHM 1%
402 CH
R4C7
511 OHM 1%
CH 402
ENET_LED2
ENET_GPO
ENET_LED0
LED2
LED1/GPO
LED0
PEX_XTAL2
R6N2
0 OHM 5%
402 CH
LAYOUT: PLACE R6N2 AND R6P1
PIN 1 ON TOP OF EACH OTHER
R6P1
1.2 KOHM 1%
402 EMPTY
DB4B1
R6N1
2.49 KOHM 1%
CH 402
ENET_RSET
RSET
XTAL2_R
XTAL1_R
R6P2
0 OHM 5%
402 EMPTY
ENET_XTAL2
ENET_XTAL1
CKXTAL2
CKXTAL1
Y6P1
25 MHZ
GND1
GND2
SM
EMPTY
C6N1
27 PF
5%
25 V
EMPTY
402
C6P1
27 PF
5%
25 V
EMPTY
402
ENET_ISOLATE_N
ISOLATE_N
PEX_SOC_ENET_TP_C
PEX_SOC_ENET_TN_C
HSIP
HSIN
ENET_PEX_SS_100M_CLKP
ENET_PEX_SS_100M_CLKN
REFCLK_P
REFCLK_N
PERST_N
X896524-002
QFN33
R4C5
10 KOHM
1%
CH
402
FT6P2 FTP
R4C8
10 KOHM
1%
EMPTY
402
OUT
WIFI_PEX_SS_100M_CLKP
WIFI_PEX_SS_100M_CLKN
R4C23
0 OHM 5%
402 EMPTY
R4C24
0 OHM 5%
402 EMPTY
R4C4
10 KOHM
1%
EMPTY
402
ENET_PCIE_RST_N
FT6P6 FTP
R4C2
10 KOHM
1%
CH
402
AVDD33_2
AVDD33_1
DVDD10
AVDD10_3
AVDD10_2
AVDD10_1
VDDREG
REGOUT
LANWAKE_N
CLKREQ_N
HSOP
HSON
MPAD
PLACE 0.1UF CLOSE TO PINS 11, 23 AND 32
PLACE 4.7UF CLOSE TO PINS 11 AND 32
C4B9 C4C3 C4B7
0.1 UF
10%
16 V
XR5
402
C4B4
4.7 UF
10%
6.3 V
X5R
603
C4B12
4.7 UF
10%
6.3 V
X5R
603
V_1P0_ENET
PLACE 0.1UF CLOSE TO PINS 3, 8, 22 AND 30
C4C2 C4C1 C4B10 C4B11
C4C4
1 UF
10%
6.3 V
X5R
402
C4B3
4.7 UF
10%
6.3 V
X5R
603
PLACE 0.1UF
CLOSE TO PIN 24
C4C6
0.1 UF 10%
16 V
XR5
402
L6P1
4.7 UH
X821308-001
EMPTY
FTP FT6P5
DB4C1
R4C10
0 OHM 5%
805 CH
ENET_REGOUT
ENET_WAKE_N
PEX_REF_CLK1_REQN_R
R4C9
10 KOHM
1%
CH
402
R4B8
10 KOHM
1%
CH
402
C6P2
PEX_ENET_SOC_TP
PEX_ENET_SOC_TP_C
C6P3
PEX_ENET_SOC_TN
PEX_ENET_SOC_TN_C
0.1 UF 10%
16 V 402
XR5
SOFT START
NOM. VOLTAGE: 3.3V
MAX POWER: 570MW
V_3P3
Q4B3
FET
SOT23
X889118-002
C4B6
1 UF
10%
6.3 V
X5R
402
V_ENET_IR_OUT_G
R4B6
100 OHM 1%
402 CH
V_ENET_IR_OUT_CGD
R4B7
20 KOHM
1%
CH
402
C4B8
0.22 UF
10%
10 V
X7R
402
C4B2
10 UF
20%
6.3 V
EMPTY
603
C4B5
10 UF
20%
6.3 V
X5R
603
R4B5
1 KOHM
1%
EMPTY
402

NOTES:

1. THE RTL8111HM IS CONFIGURED FROM REALTEK WITH EFUSE "ENABLE LAN DISABLE" MODE SET, WHICH PROVIDES DEFAULT SUPPORT FOR SIGNAL ENET_LPMODE_N. THIS FEATURE CAN BE OVERRIDDEN BY SOFTWARE
2. TO SUPPORT A PCIE WIFI INTERFACE (J3C1), THE FOLLOWING BOM CHANGES ARE NEEDED:
   - A: POPULATE R4C23 AND R4C24, WHICH WILL SEND THE 100 MHZ CLOCK TO THE WIFI INTERFACE. IN ADDITION, IT IS CRITICAL THAT EACH LEG OF THE CLOCK BE TERMINATED AT THE FAR END INTO 50 OHMS.
   - B: ON PAGE 2, POPULATE AC COUPLING CAPS C6P6 AND C6P7
   - C: FOR PRELIMINARY DEVELOPMENT TESTING, NO OTHER BOM CHANGES ARE REQUIRED. THE ETHERNET CONTROLLER WILL MANAGE THE ENABLING OF THE 100 MHZ CLOCK.
   - D: FOR PRODUCTION RETAIL, ON PAGE 29 REMOVE R4B3 AND POPULATE R4C26. THIS CHANGE WILL REQUIRE MODIFIED SMC FIRMWARE TO EXPLICITLY ENABLE THE 100 MHZ CLOCK.

RL Network

EMMC

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X934261-001	IC	U3D1	MEM,SM,8GB,EMMC,15NM,THGBMFG6C1LBAILL	EMMC_TOSHIBA
X904693-001	IC	U3D1	MEM,SM,8GB,EMMC,FLASH,16NM,BGA153,KLM8G1GEND-B031,SAMSUNG	EMMC_SAMSUNG
X939723-001	IC	U3D1	MEM,SM,8GB,64GBX1,H26M41204HPR	EMMC_HYNIX_5P0
X800617-001	CH	R4E9,R4E13,R4E11,R4E17,R4E15,R4E21,R4E19,R4E23	RES-FXD,SM,49.9 OHM 1%,1/16W,0402	EMMC_TOSHIBA,EMMC_SAMSUNG
X809936-001	CH	R4E9,R4E13,R4E11,R4E17,R4E15,R4E21,R4E19,R4E23	RES-FXD,SM,100 OHM 1%,1/16W,0402	EMMC_HYNIX_5P0

RL Network

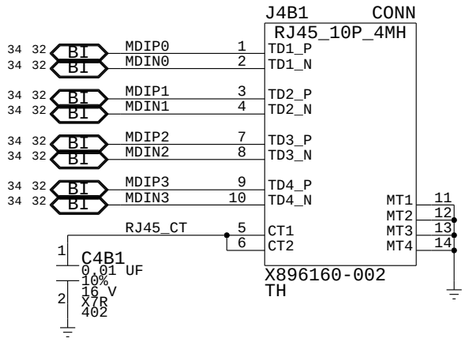
SIGNALS ROUTED TO NC PINS FOR ESCAPE

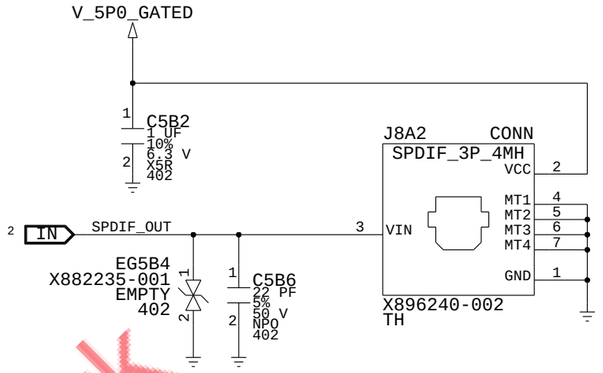
D7	PIN B6 ROUTED TO PIN C7, C8
D6	PIN B5 ROUTED TO PIN C5
D5	PIN B4 ROUTED TO PIN C3, D3
D4	PIN B3 ROUTED TO PIN A2
D3	PIN B2 ROUTED TO PIN C1
VDDI	PIN C2 ROUTED TO PIN D1
GND	PIN N2 ROUTED TO PIN M1

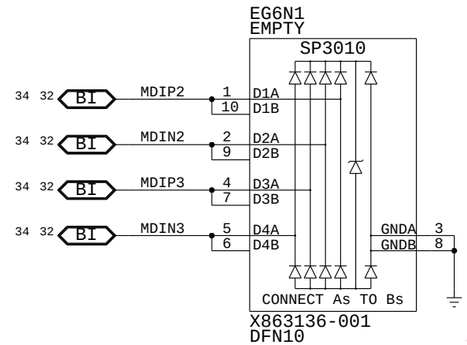
MMC_X NETS ARE DUMMY NETS TO IMPROVE PAD ADHESION

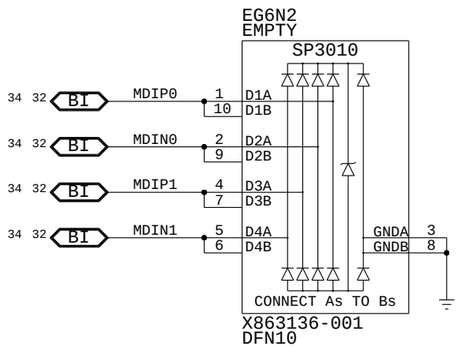
MICROSOFT CONFIDENTIAL	PROJECT NAME: Kingston	PAGE: 33/72	CSA PAGE: 33/72	FAB: G	VER: 1.01

CONN: RJ45,TOSLINK





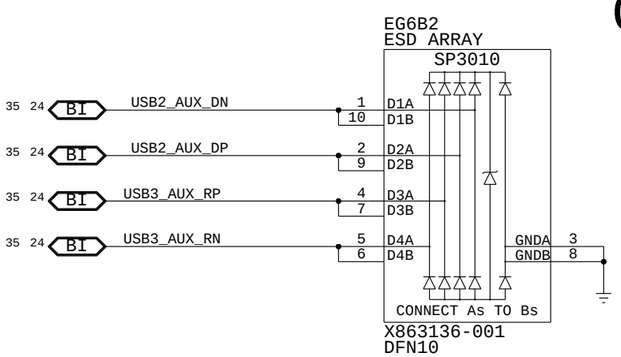


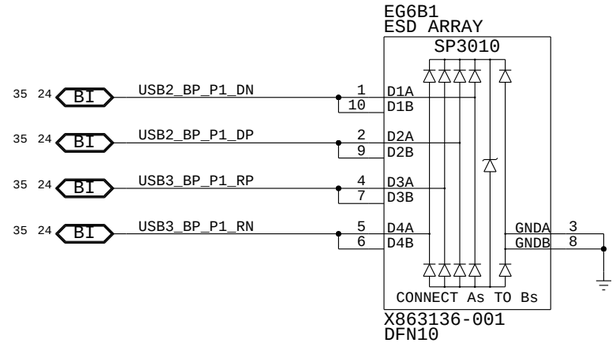


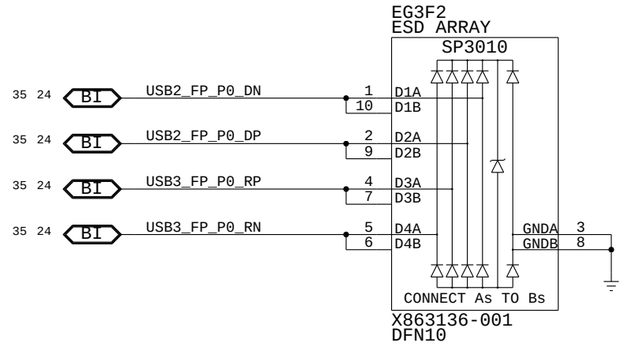
RL Network

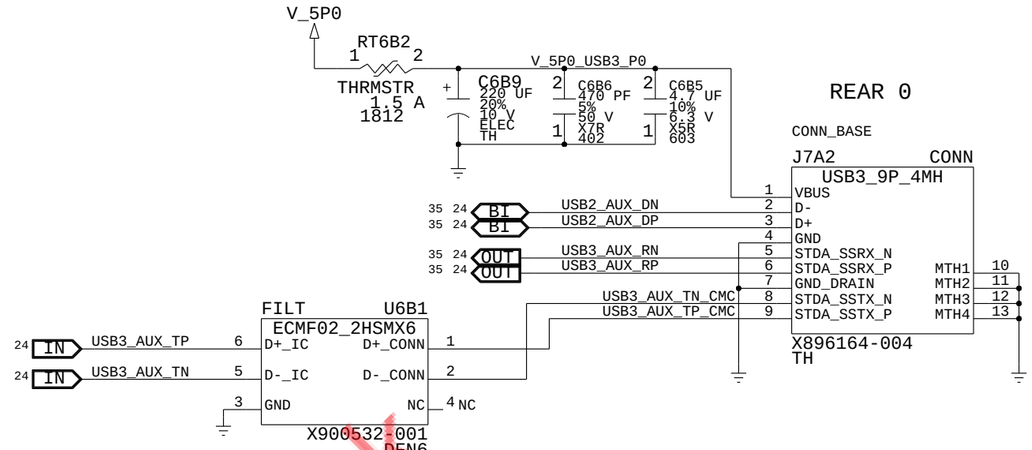
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	34/72	34/72	G	1.01

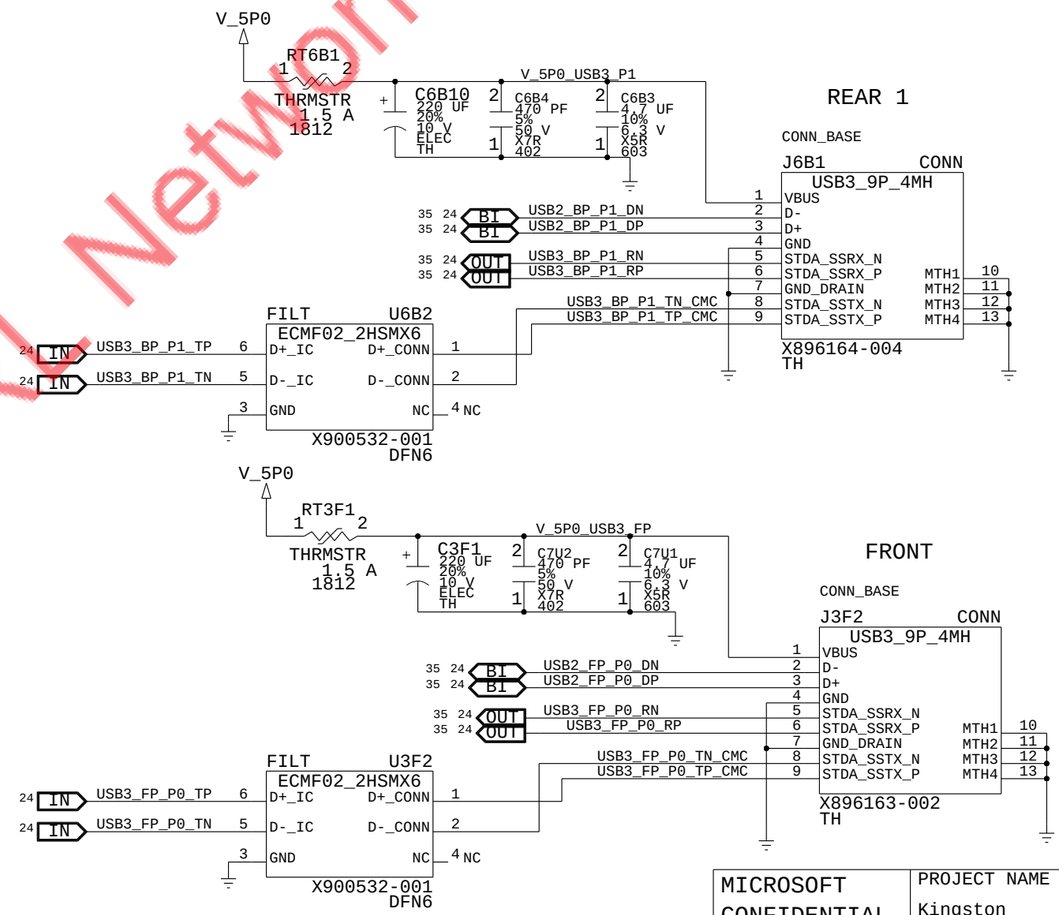
CONN: USB (FRONT & REAR)











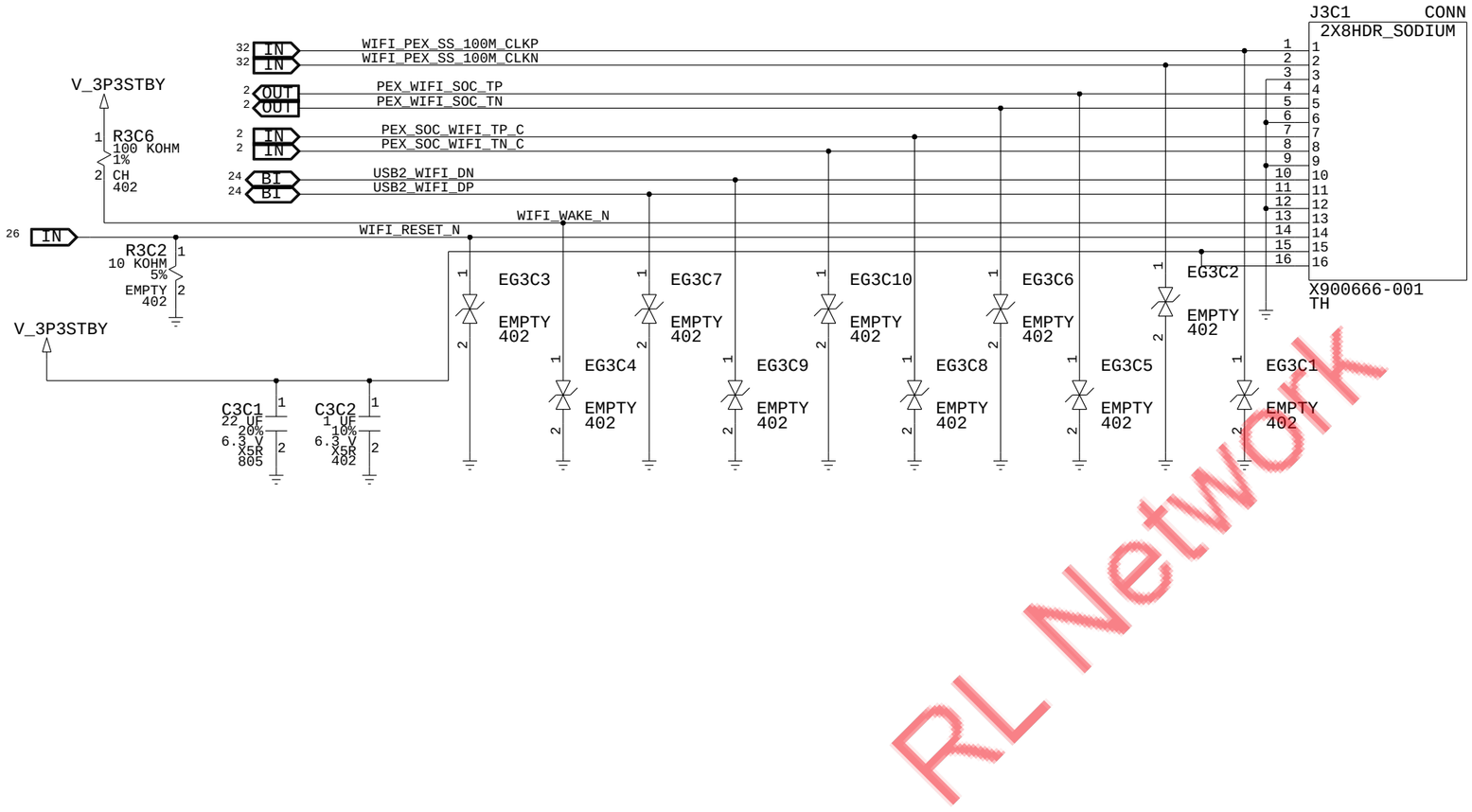
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896164-004	CONN	J7A2,J6B1	CONN-USB,TH,009,FEMALE,USB3-A,BLACK NI, KGS	USB_REAR_FOXC_BLACK
X896164-003	CONN	J7A2,J6B1	CONN-USB,SM,009,FEMALE,USB3-A,PLAIN NI, KGS	USB_REAR_FOXC_PLAIN

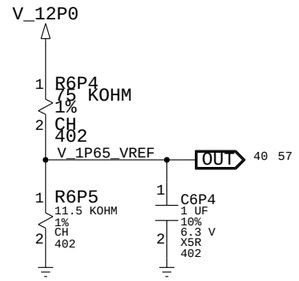
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896163-004	CONN	J3F2	CONN-USB,TH,009,FEMALE,FRONT,USB3-A,BLACK NICKEL,KGS	USB_FRONT_FOXC
X907318-002	CONN	J3F2	CONN-USB,TH,009,FEMALE,FRONT,USB3-A,KGS,(QUAL-AMPHENOL)	USB_FRONT_AMPH

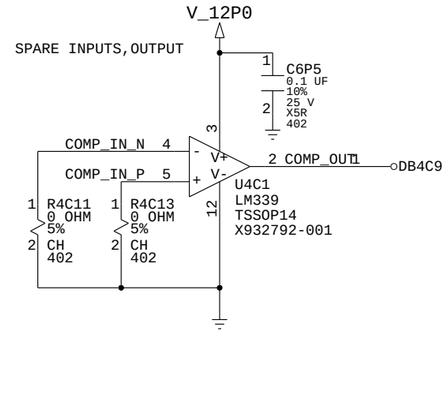
RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	35/72	35/72	G	1.01

CONN: WIFI



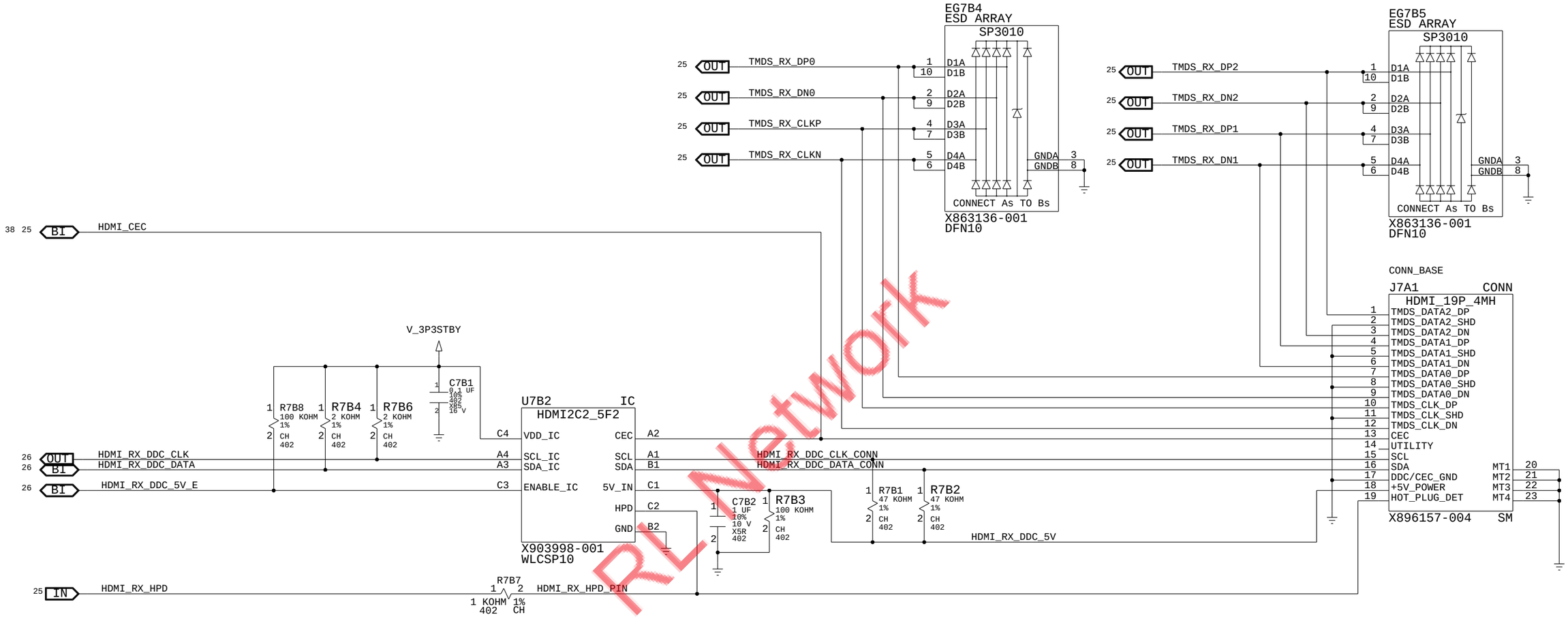




RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	36/72	36/72	G	1.01

CONN: HDMI IN



RL Network

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X896157-006	CONN	J7A1,J8A1	CONN-HDMI,SM.019,FEMALE,W/EMI FLANGES,BLACK NI,KGS	HDMI_FOXC_BLACK
X896157-005	CONN	J7A1,J8A1	CONN-HDMI,SM,019,FEMALE,W/ EMI FLANGES,PLAIN NI, KGS	HDMI_FOXC_PLAIN

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	37/72	37/72	G	1.01

CONN: HDMI OUT

DP159 CONTROL SLAVE ADDRESS			
SELECTED	A1/A0	7-BIT ADDRESS	8-BIT ADDRESS
-->	00	0X5E	BC/BD
	01	0X5D	BA/BB
	10	0X5C	B8/B9
	11	0X5B	B6/B7

U8B2 IC — SN75DP159 1 OF 3 CONTROL — X944186-001 QFN41

U8B2 IC — SN75DP159 2 OF 3 HDMI — X944186-001 QFN41

U8B2 IC — SN75DP159 3 OF 3 POWER — X944186-001 QFN41

EG8B6 ESD ARRAY SP3010 — X863136-001 DFN10

EG8B7 ESD ARRAY SP3010 — X863136-001 DFN10

U8B1 IC — HDMI2C4_5F2 — X934148-001 WLCSP12

HDMI LOAD SWITCH
NOM.VOLTAGE: 5V
PEAK CURRENT: 0.2A

CONN_BASE
J8A1 CONN — HDMI_19P_4MH — X896157-004 SM

DATA P LINE DELAY ADDED TO BOARD TO COMPENSATE FOR DP159 INTRAPAIR SKEW

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	38/72	38/72	G	1.01

CONN: HDMI SUPPORT

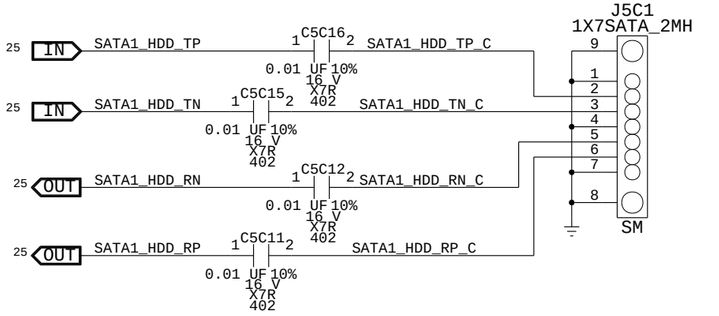
BLANK

RL Network

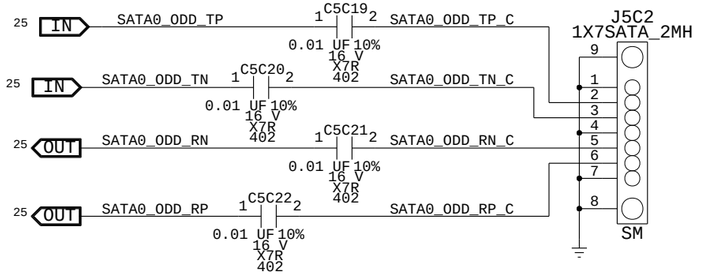
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	39/72	39/72	G	1.01

CONN: ODD & HDD

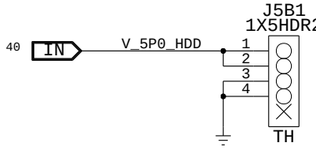
HDD SATA

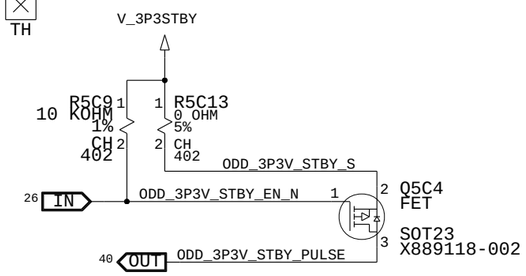


ODD SATA

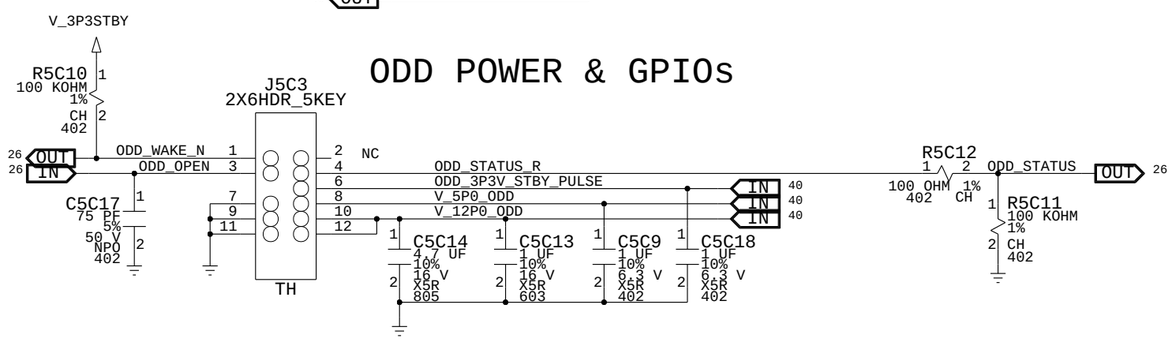


HDD POWER



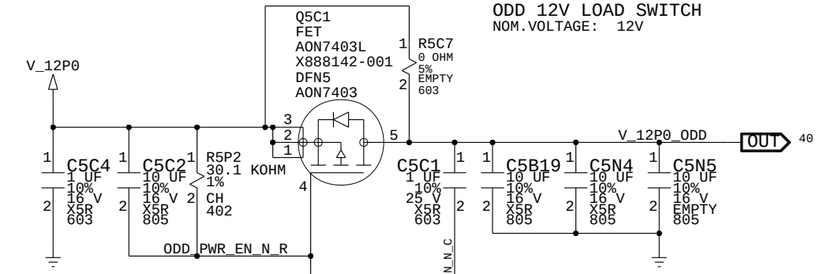


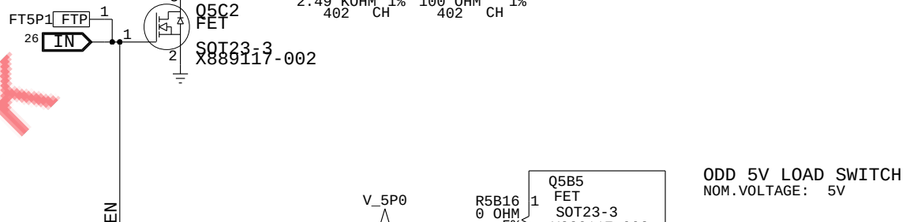
ODD POWER & GPIOs



ODD 12V LOAD SWITCH

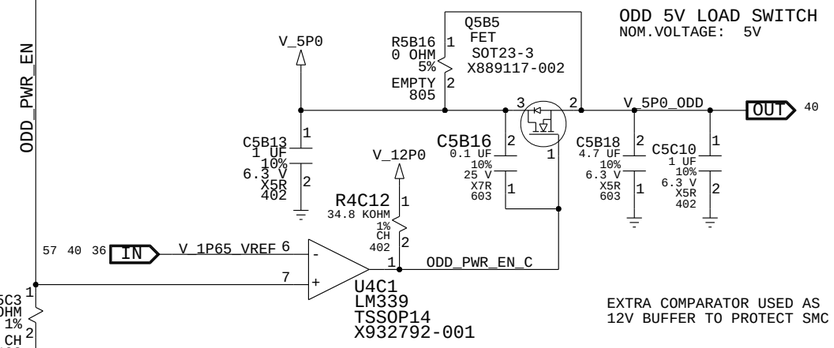
NOM.VOLTAGE: 12V





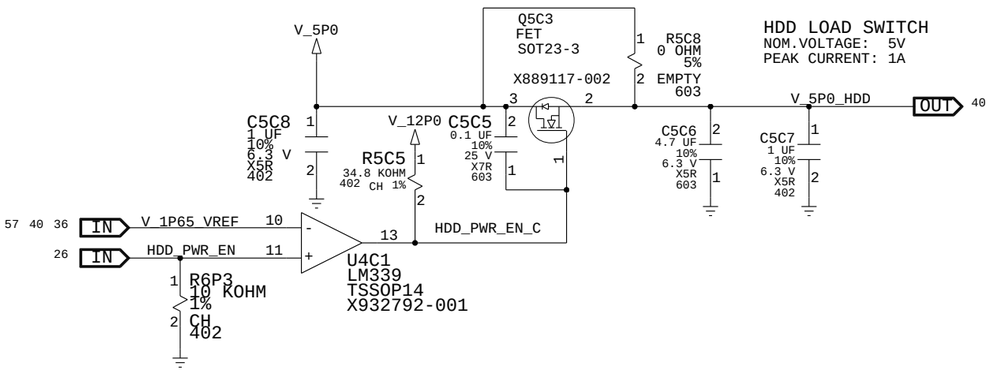
ODD 5V LOAD SWITCH

NOM.VOLTAGE: 5V



HDD LOAD SWITCH

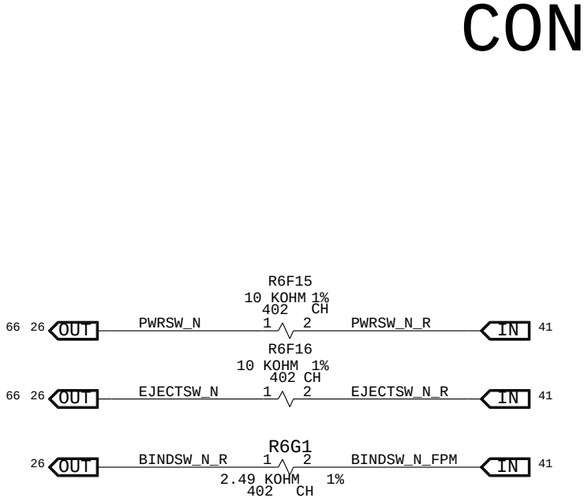
NOM.VOLTAGE: 5V
PEAK CURRENT: 1A

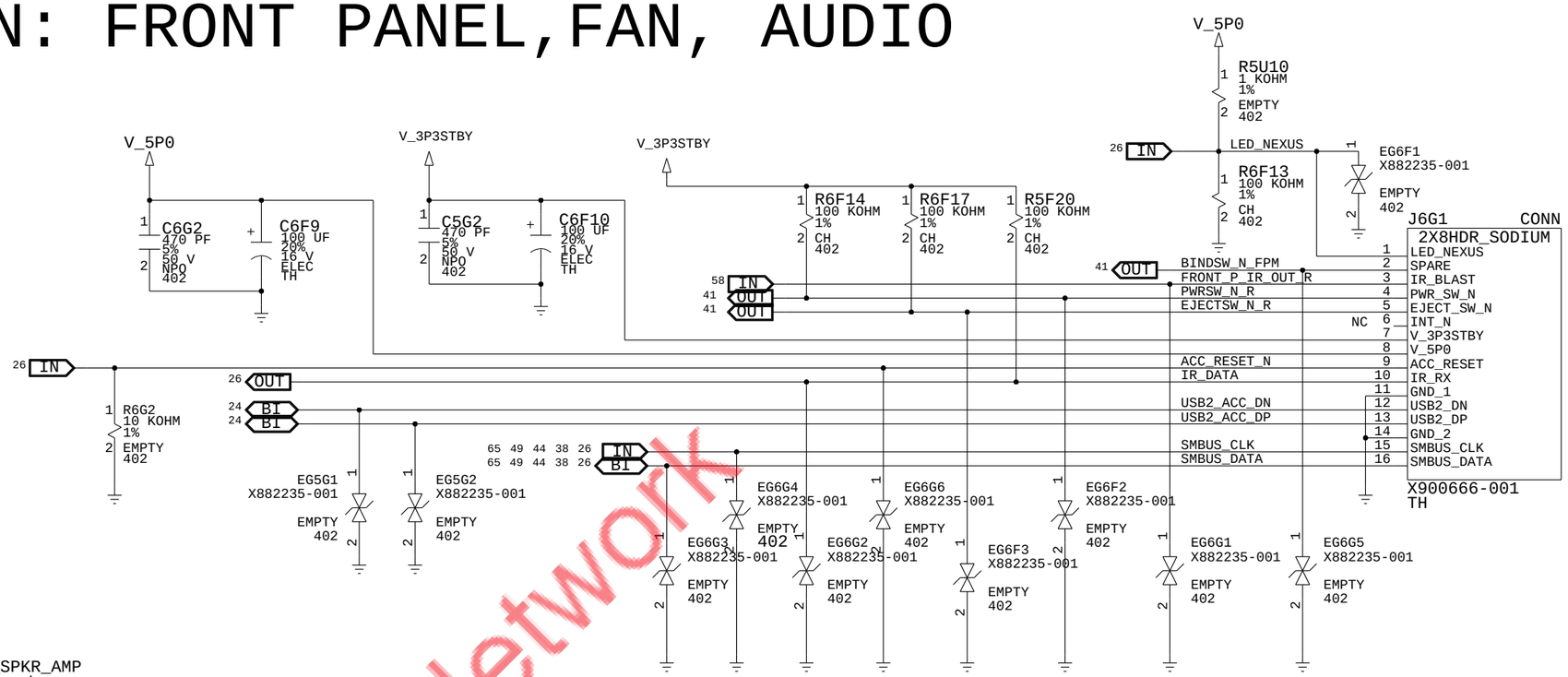


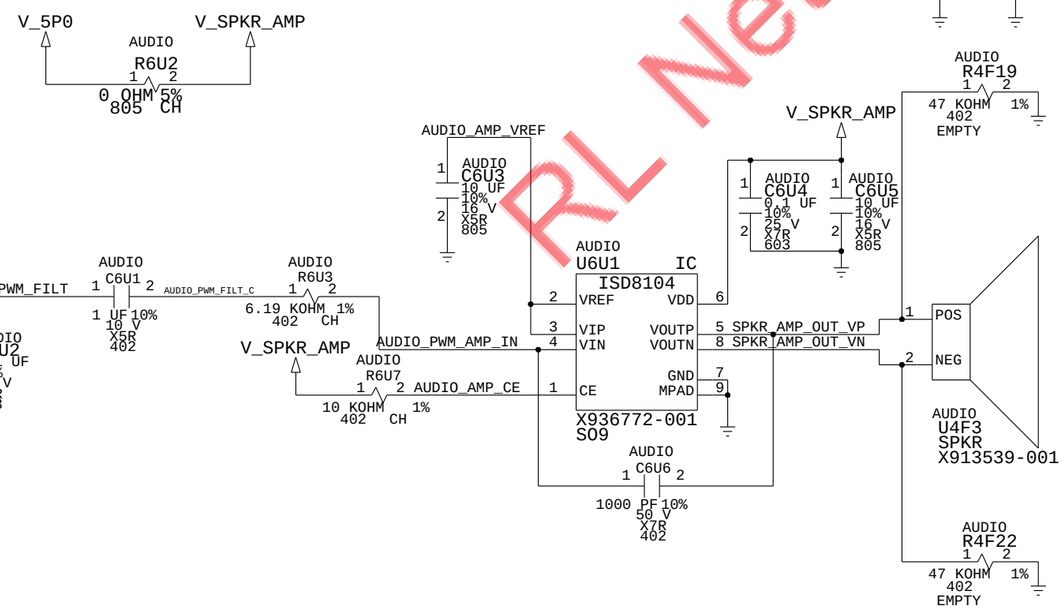
RL Network

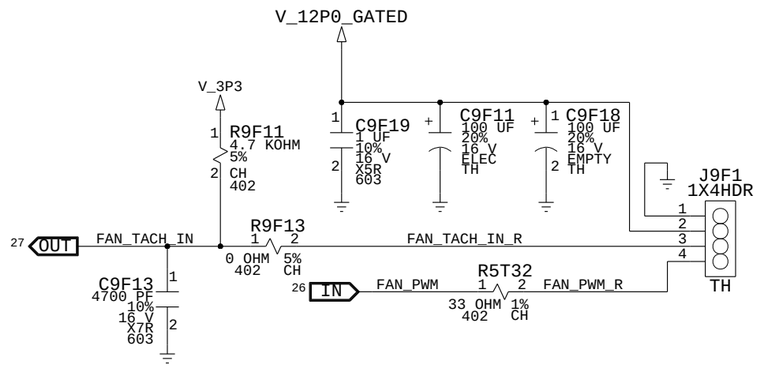
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	40/72	40/72	G	1.01

CONN: FRONT PANEL,FAN, AUDIO





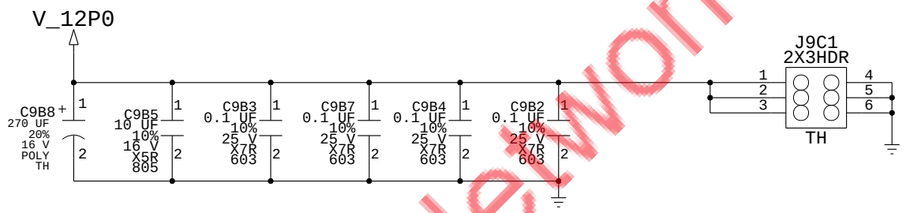


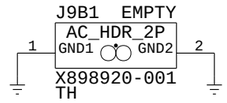


RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	41/72	41/72	G	1.01

CONN: POWER



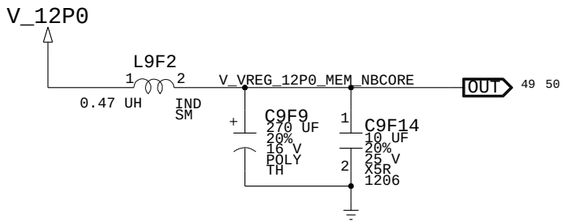


RL Network

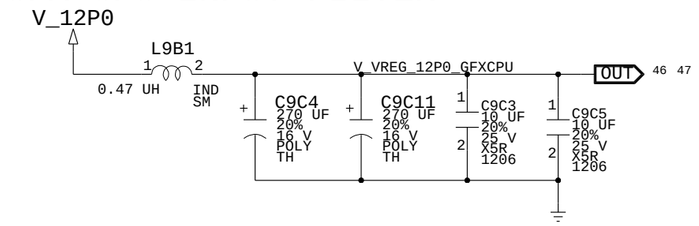
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	42/72	42/72	G	1.01

VREGS: INPUT & OUTPUT FILTERS

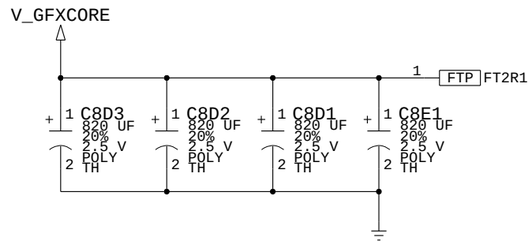
IO/NBCORE INPUT FILTER



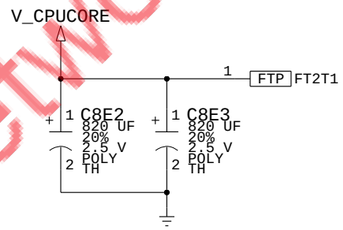
GFX/CPU INPUT FILTER



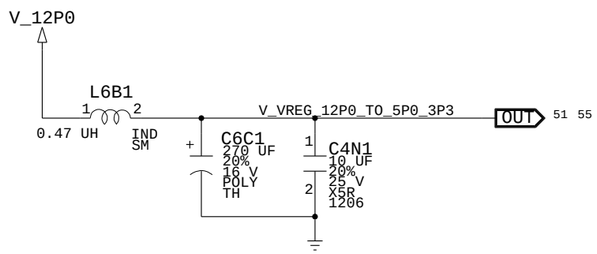
V_GFXCORE OUTPUT FILTER



V_CPUCORE OUTPUT FILTER



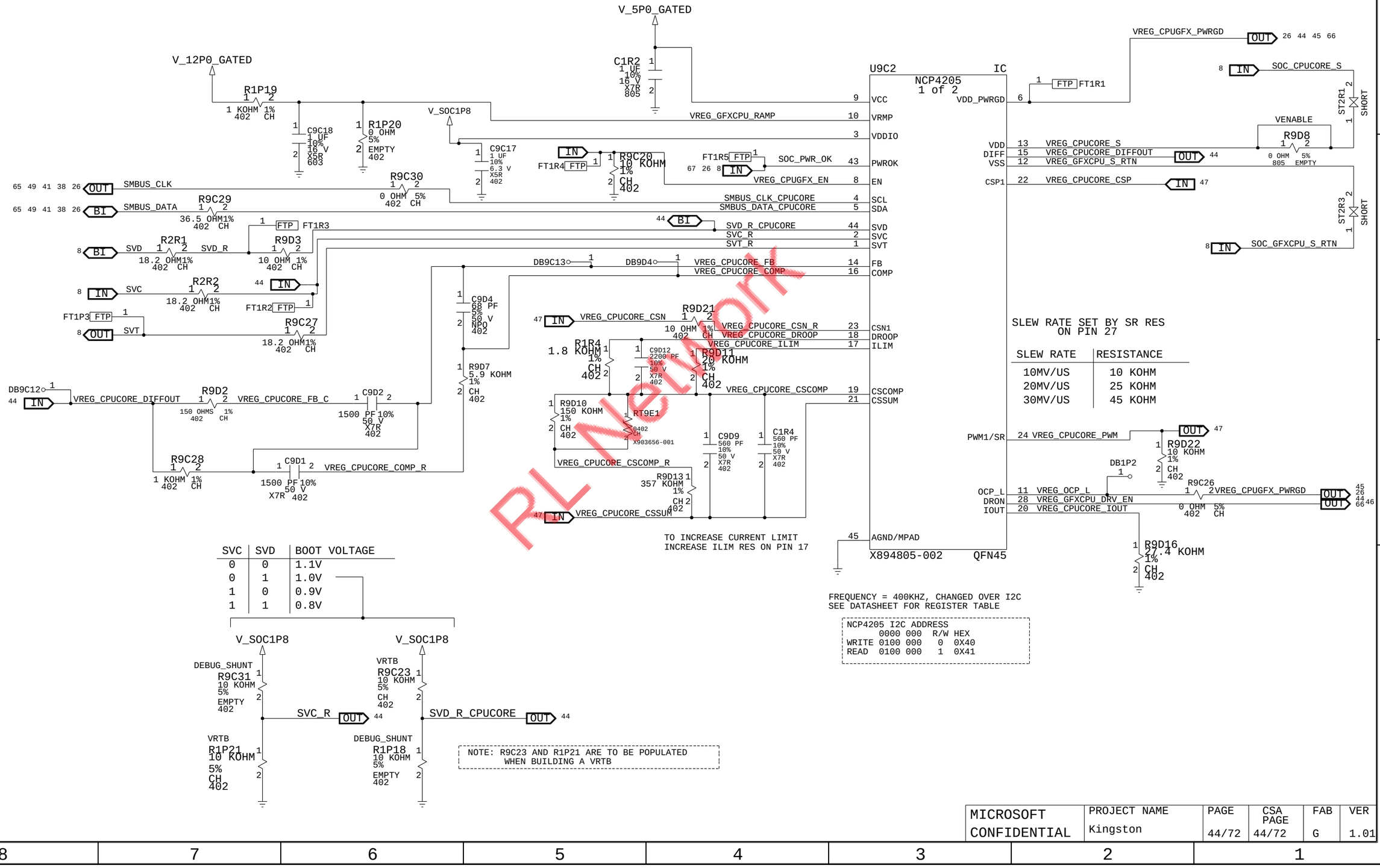
V_5P0 AND V_3P3 INPUT FILTER



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	43/72	43/72	G	1.01

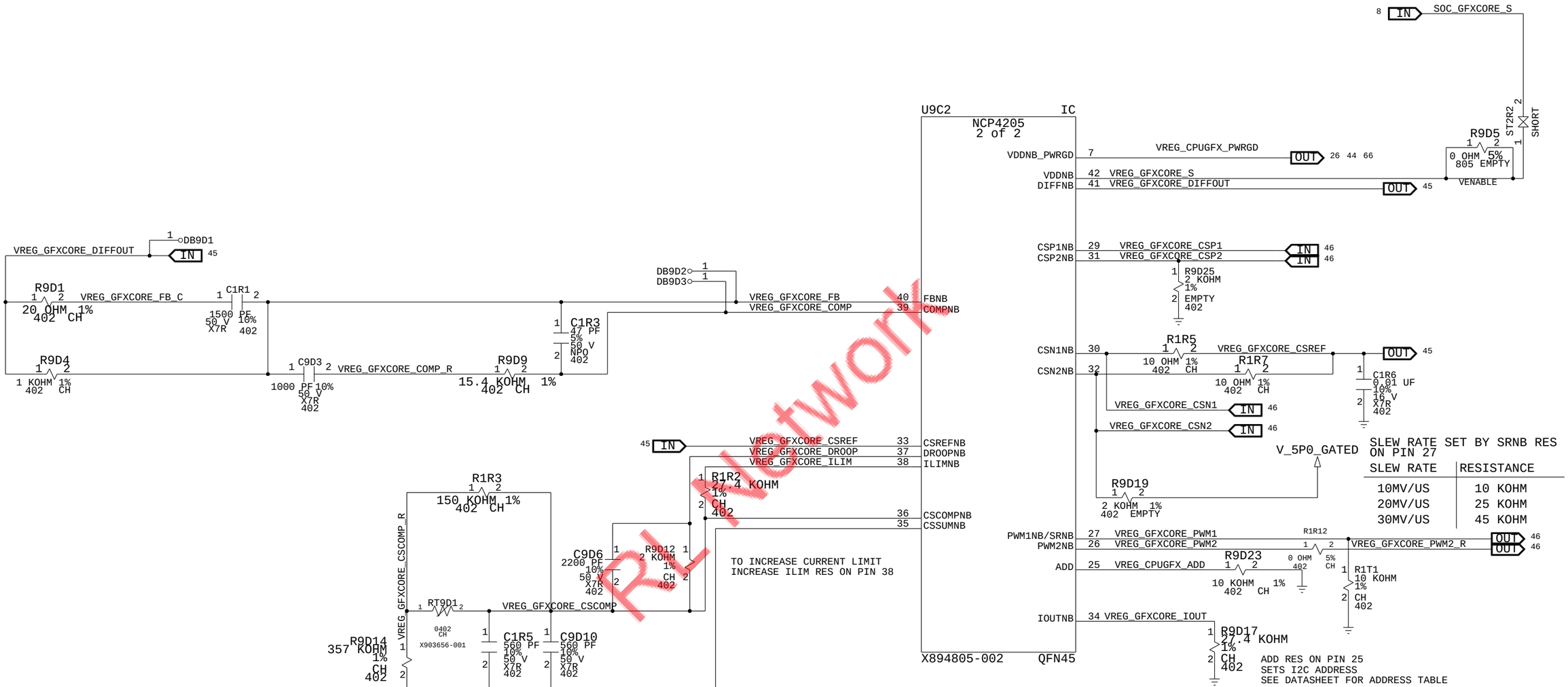
VREGS: CPUCORE



RLNetwork

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	44/72	44/72	G	1.01

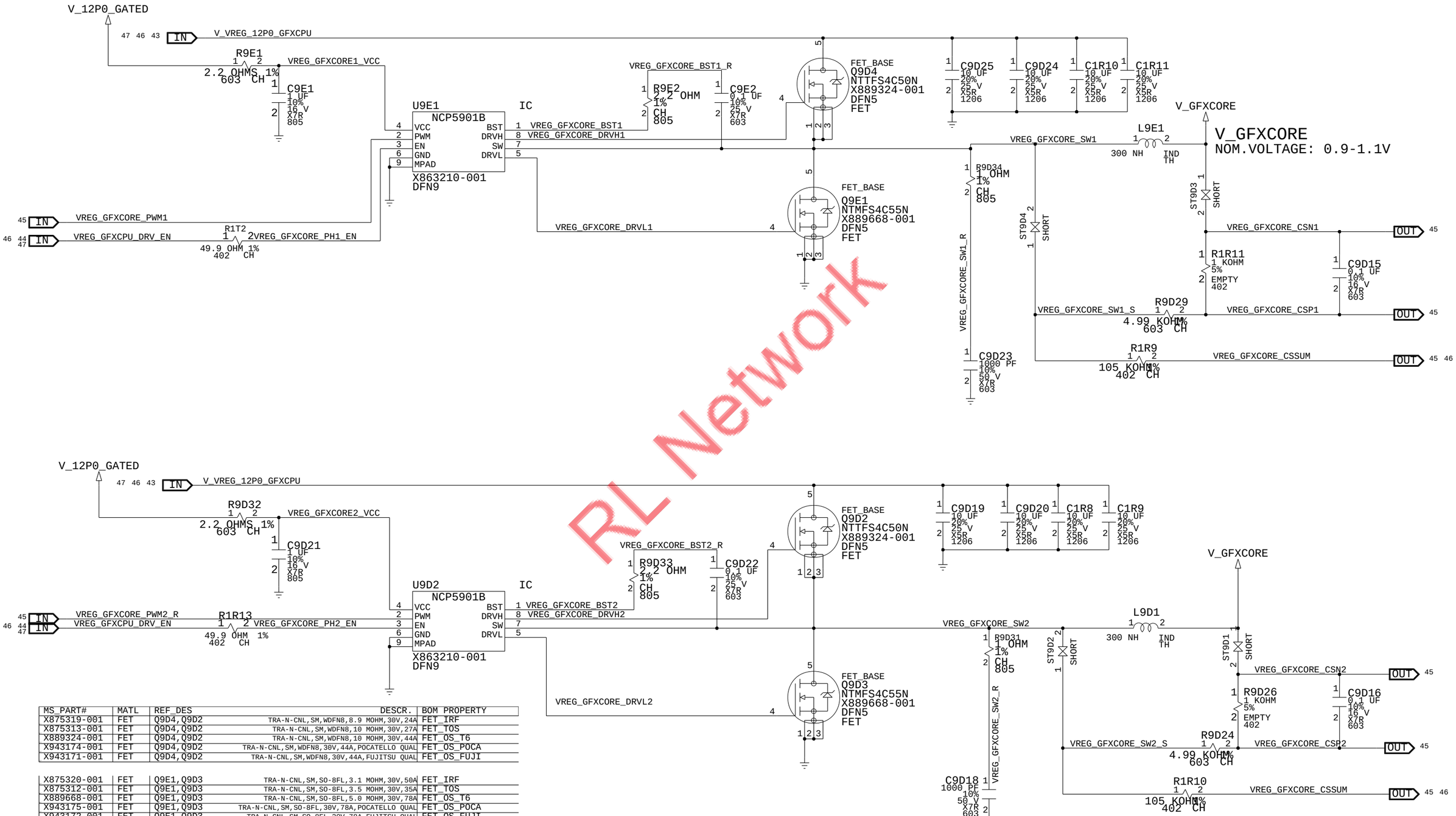
VREGS: GFXCORE



Rev Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	45/72	45/72	G	1.01

VREGS: GFXCORE OUTPUT PHASE 1 & 2



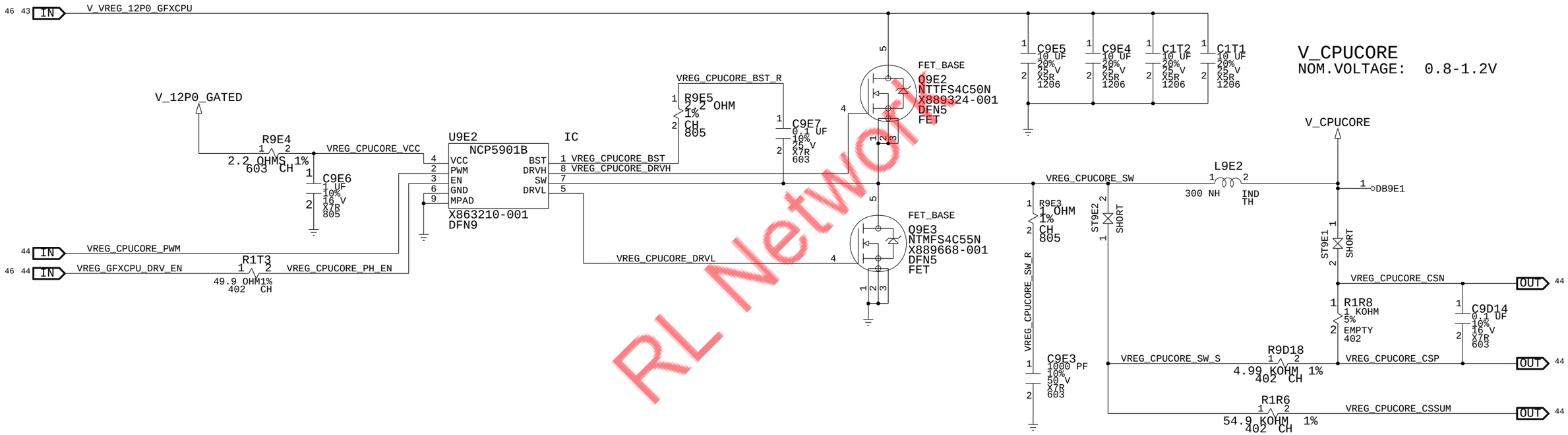
RL Network

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X875319-001	FET	Q9D4,Q9D2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30V,24A	FET_IRF
X875313-001	FET	Q9D4,Q9D2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,27A	FET_TOS
X889324-001	FET	Q9D4,Q9D2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,44A	FET_OS_T6
X943174-001	FET	Q9D4,Q9D2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9D4,Q9D2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

X875320-001	FET	Q9E1,Q9D3	TRA-N-CNL,SM,SO-8FL,3.1 MOHM,30V,50A	FET_IRF
X875312-001	FET	Q9E1,Q9D3	TRA-N-CNL,SM,SO-8FL,3.5 MOHM,30V,35A	FET_TOS
X889668-001	FET	Q9E1,Q9D3	TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A	FET_OS_T6
X943175-001	FET	Q9E1,Q9D3	TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO QUAL	FET_OS_POCA
X943172-001	FET	Q9E1,Q9D3	TRA-N-CNL,SM,SO-8FL,30V,78A,FUJITSU QUAL	FET_OS_FUJI

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	46/72	46/72	G	1.01

VREGS: CPUCORE OUTPUT PHASE



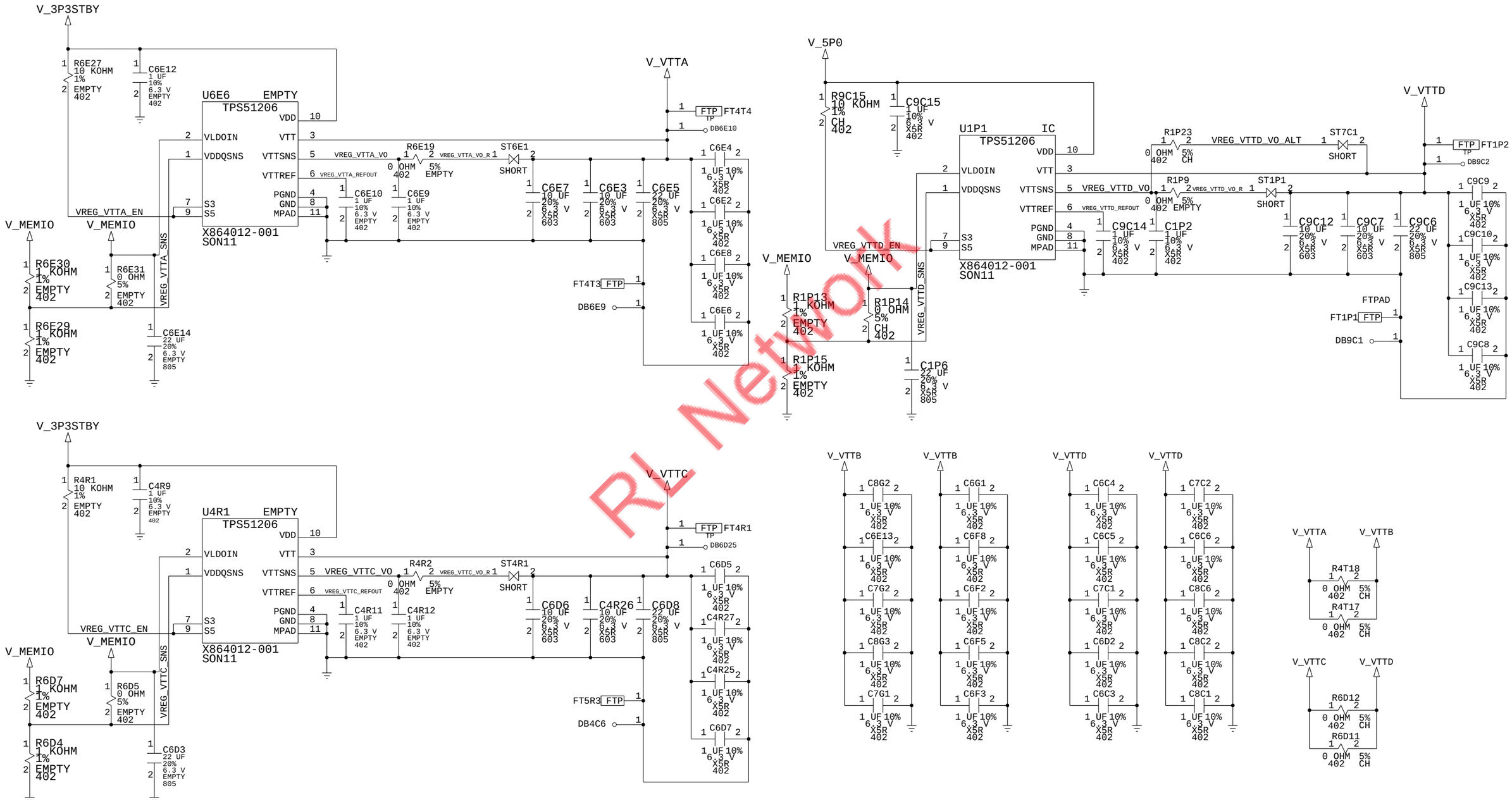
RL Network

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X875319-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30V,24A	FET_IRF
X875313-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,27A	FET_TOS
X889324-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,44A	FET_OS_T6
X943174-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9E2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

X875320-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,3.1 MOHM,30V,50A	FET_IRF
X875312-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,3.5 MOHM,30V,35A	FET_TOS
X889668-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A	FET_OS_T6
X943175-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO QUAL	FET_OS_POCA
X943172-001	FET	Q9E3	TRA-N-CNL,SM,SO-8FL,30V,78A,FUJITSU QUAL	FET_OS_FUJI

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	47/72	47/72	G	1.01

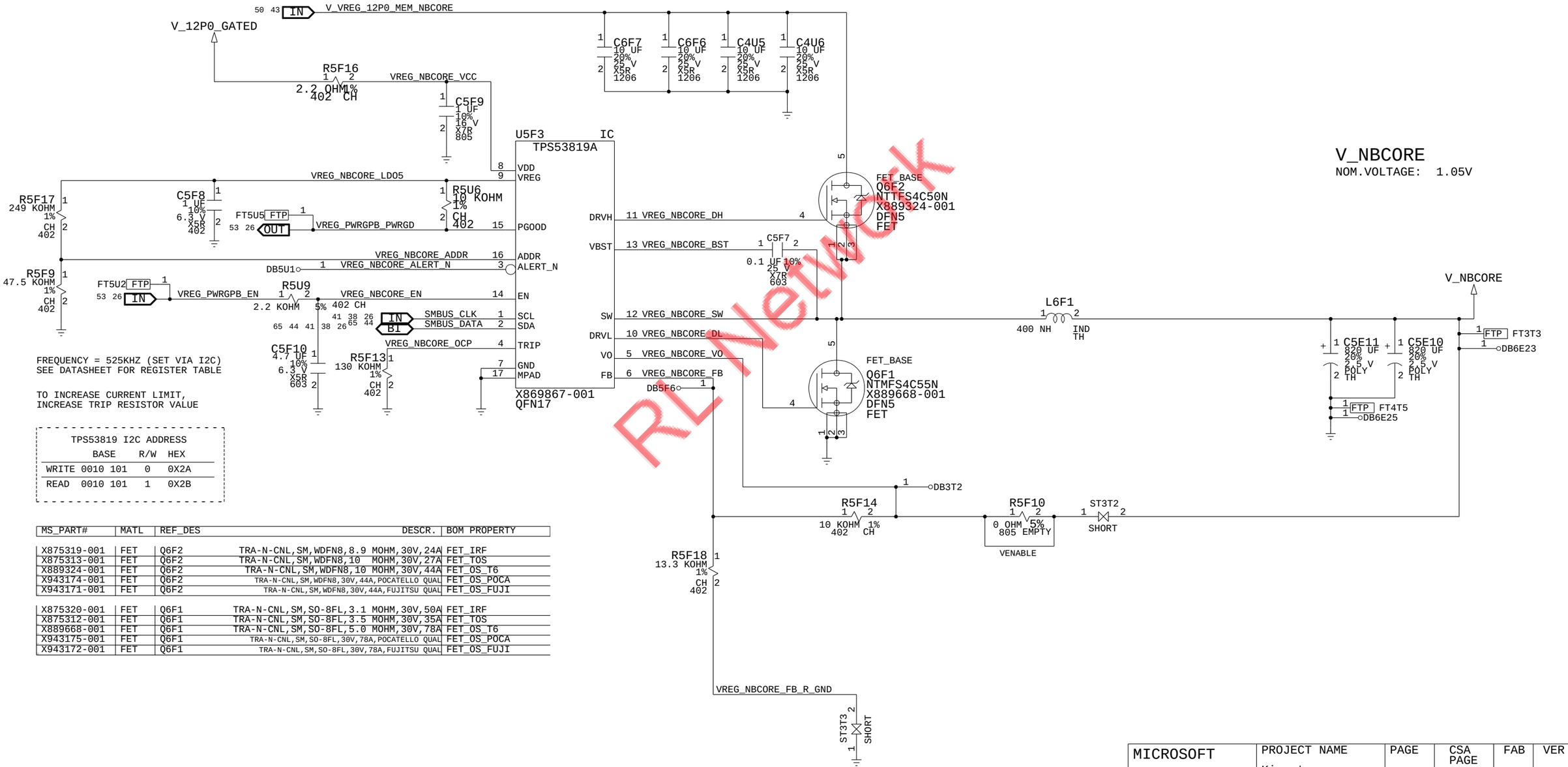
VREGS: VTT TERMINATION



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	48/72	48/72	G	1.01

VREGS: NBCORE



FREQUENCY = 525KHZ (SET VIA I2C)
SEE DATASHEET FOR REGISTER TABLE

TO INCREASE CURRENT LIMIT,
INCREASE TRIP RESISTOR VALUE

TPS53819 I2C ADDRESS

BASE	R/W	HEX
WRITE 0010 101	0	0X2A
READ 0010 101	1	0X2B

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X875319-001	FET	Q6F2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30V,24A	FET_IRF
X875313-001	FET	Q6F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,27A	FET_TOS
X889324-001	FET	Q6F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30V,44A	FET_OS_T6
X943174-001	FET	Q6F2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q6F2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI
X875320-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,3.1 MOHM,30V,50A	FET_IRF
X875312-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,3.5 MOHM,30V,35A	FET_TOS
X889668-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,5.0 MOHM,30V,78A	FET_OS_T6
X943175-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,30V,78A,POCATELLO QUAL	FET_OS_POCA
X943172-001	FET	Q6F1	TRA-N-CNL,SM,SO-8FL,30V,78A,FUJITSU QUAL	FET_OS_FUJI

V_NBCORE
NOM.VOLTAGE: 1.05V

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	49/72	49/72	G	1.01

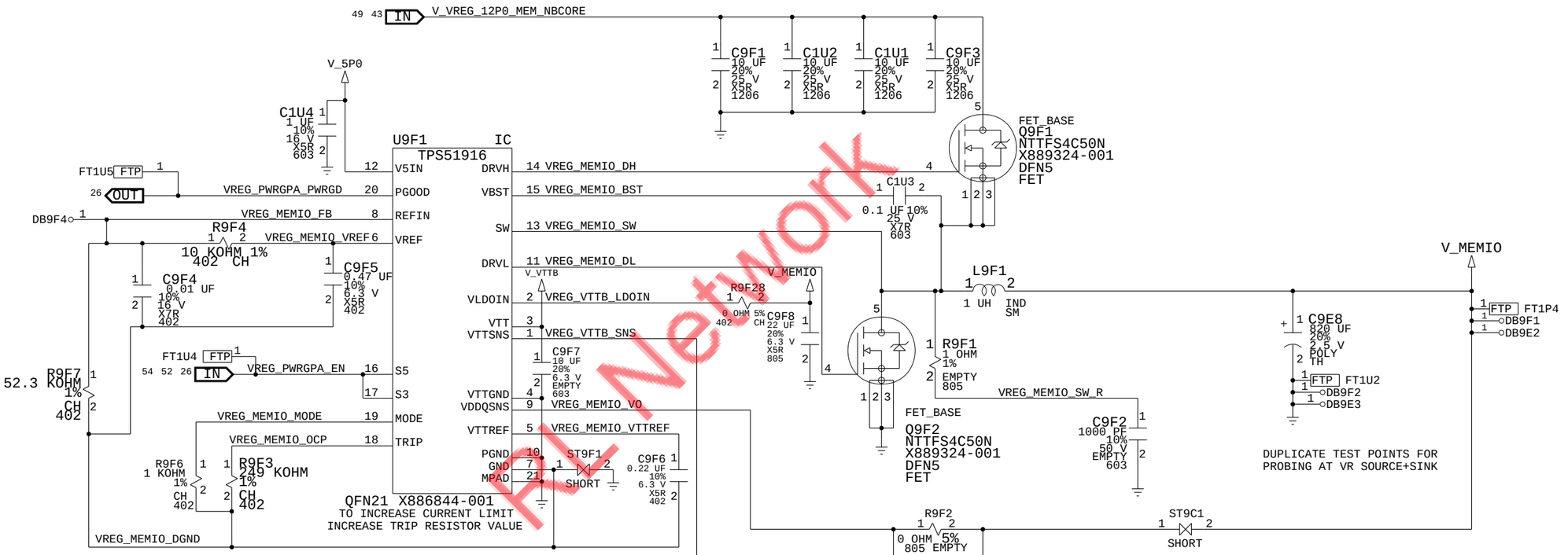
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X875319-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A	FET_IRF
X875313-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A	FET_TOS
X889324-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A	FET_OS_T6
X943174-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9F1	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

X875319-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,8.9 MOHM,30 V,24 A	FET_IRF
X875313-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,27 A	FET_TOS
X889324-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,10 MOHM,30 V,44 A	FET_OS_T6
X943174-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,30V,44A,POCATELLO QUAL	FET_OS_POCA
X943171-001	FET	Q9F2	TRA-N-CNL,SM,WDFN8,30V,44A,FUJITSU QUAL	FET_OS_FUJI

Q9F2 MATCHES Q9F1

VREG: MEMIO

V_MEMIO
NOM. VOLTAGE: 1.50



Rail Network

Rmode	Cntrl- Freq - Discharge
200K	Dcap - 400KHz Tracking
100K	Dcap - 300KHz Tracking
68K	Dcap - 300KHz Nontracking
47K	Dcap - 400KHz Nontracking
33K	Dcap2- 500KHz Nontracking
22K	Dcap2- 670KHz Nontracking
12K	Dcap2- 670KHz Tracking
1K	Dcap2- 500KHz Tracking

$$Itrip = \frac{Rtrip \times 10uA}{8 \times Rdson\_lowfet} + \frac{(Vin - Vout) \times Vout}{2 \times Lx \times fsw \times Vin}$$

$$Itrip = (Rtrip/4800) + 1.64$$

$$Iripple = \frac{(Vin - Vout) \times Vout}{Lx \times fsw \times Vin}$$

$$Iripple = 3.281A$$

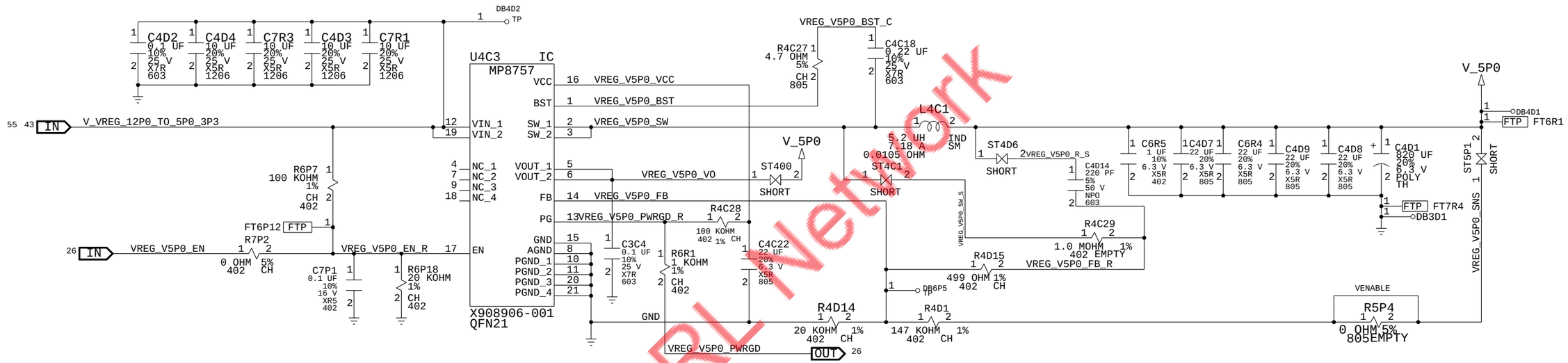
$$Vout = \frac{1.8 \times R2}{R1 + R2} + \frac{Iripple \times ESR}{2}$$

$$Vout = 1.8\ R2/(R1+R2) + 0.010$$

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	50/72	50/72	G	1.01

VREGS: V5P0

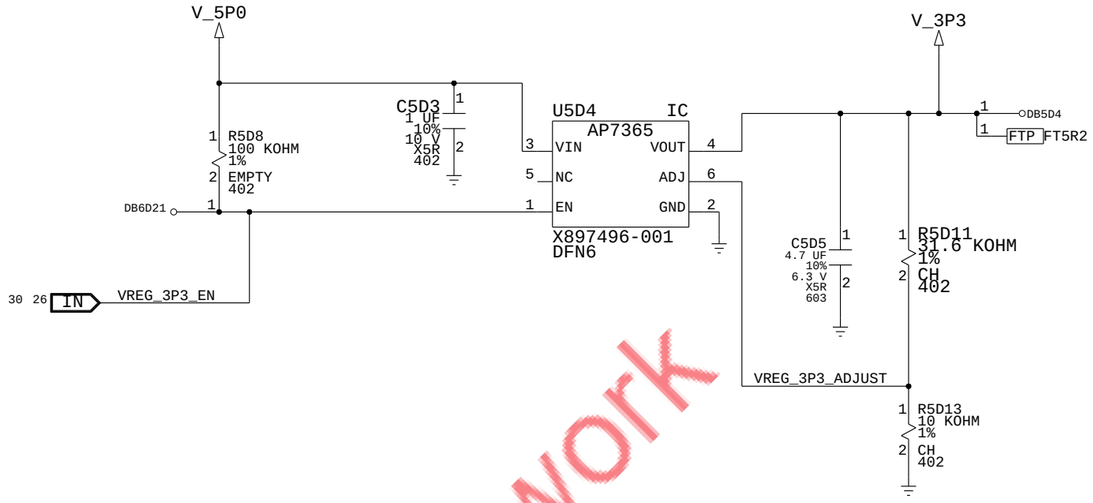
V_5P0
NOM. VOLTAGE: 5.09

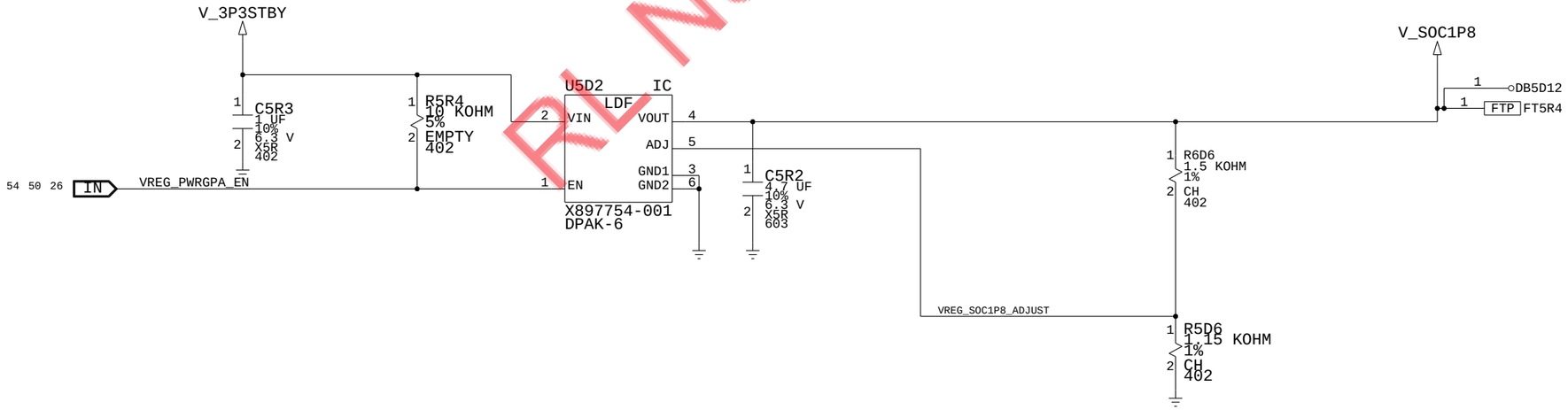


RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	51/72	51/72	G	1.01

VREGS: V3P3, VS0C1P8

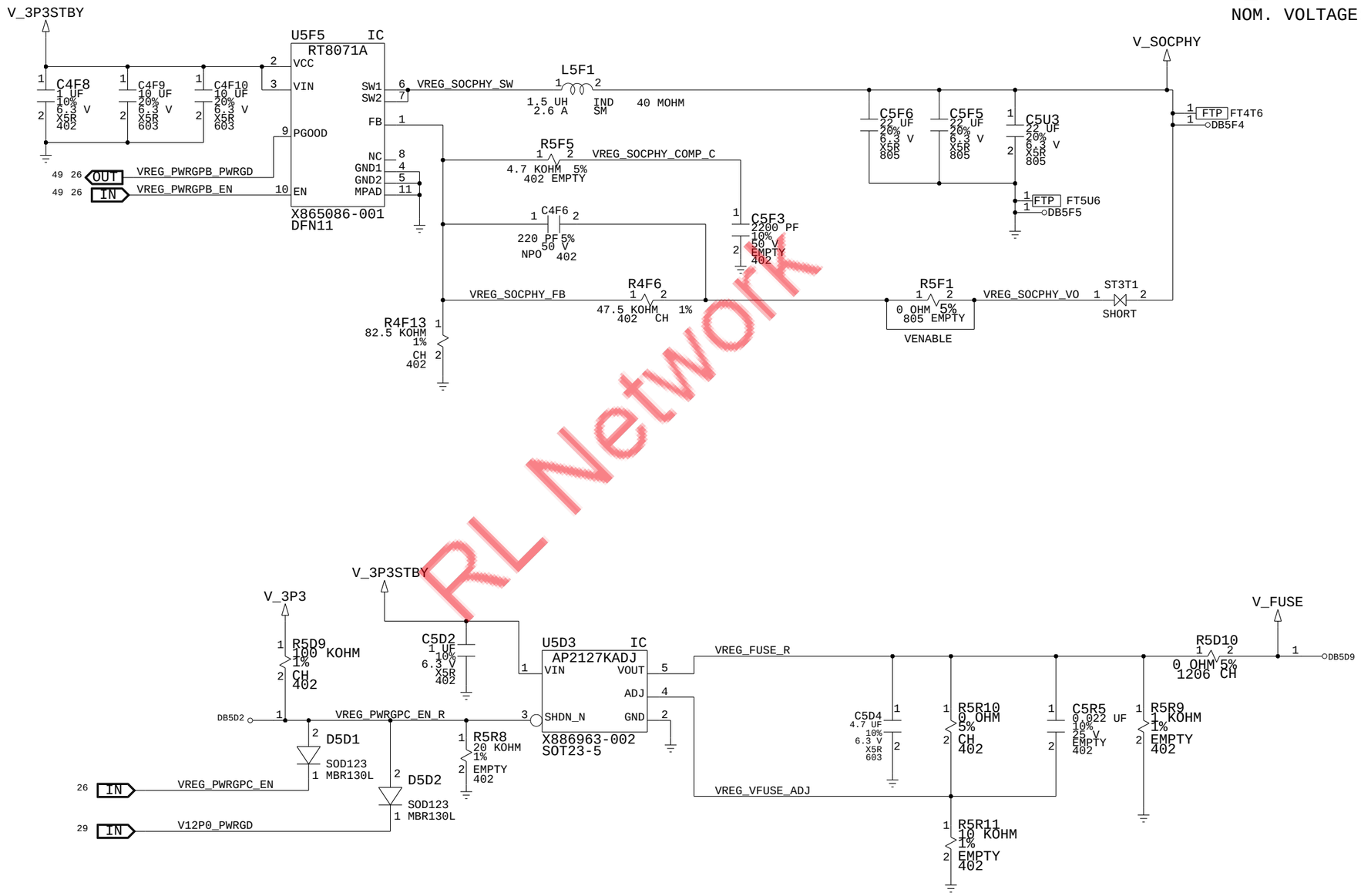




RE Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	52/72	52/72	G	1.01

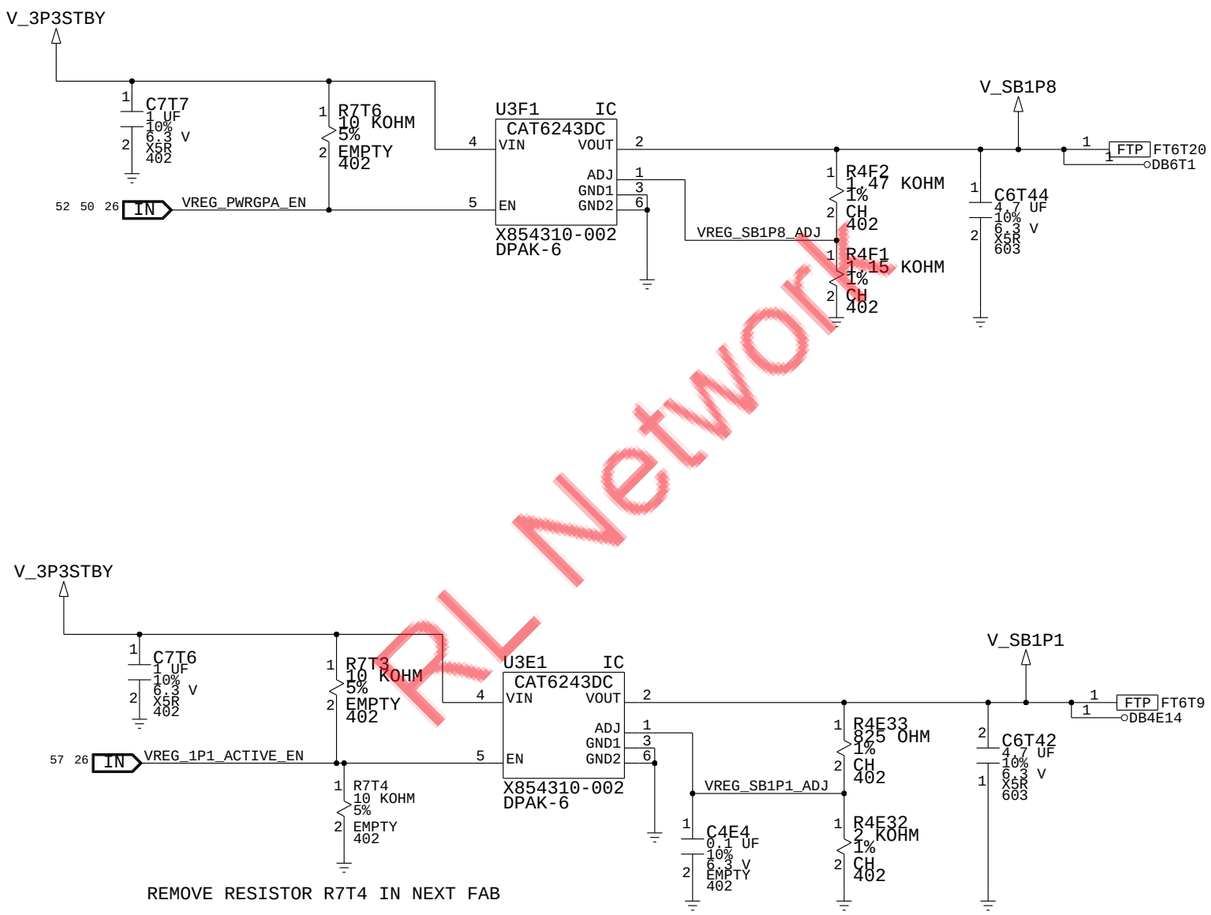
VREGS: VSOCPHY/VFUSE



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	53/72	53/72	G	1.01

VREGS: V_SB1P8, V_SB1P1



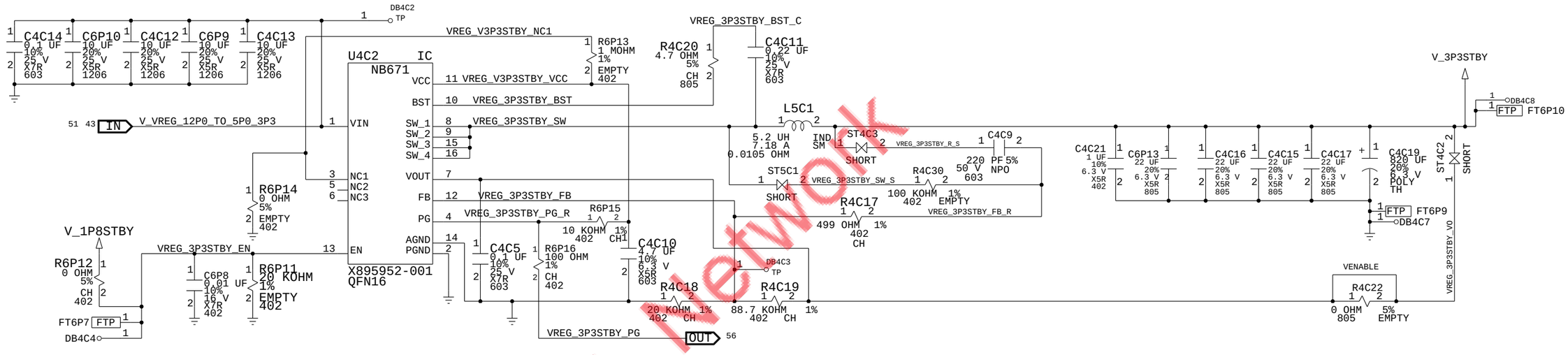
REMOVE RESISTOR R7T4 IN NEXT FAB

RL Networks

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	54/72	54/72	G	1.01

VREGS: V3P3 STANDBY

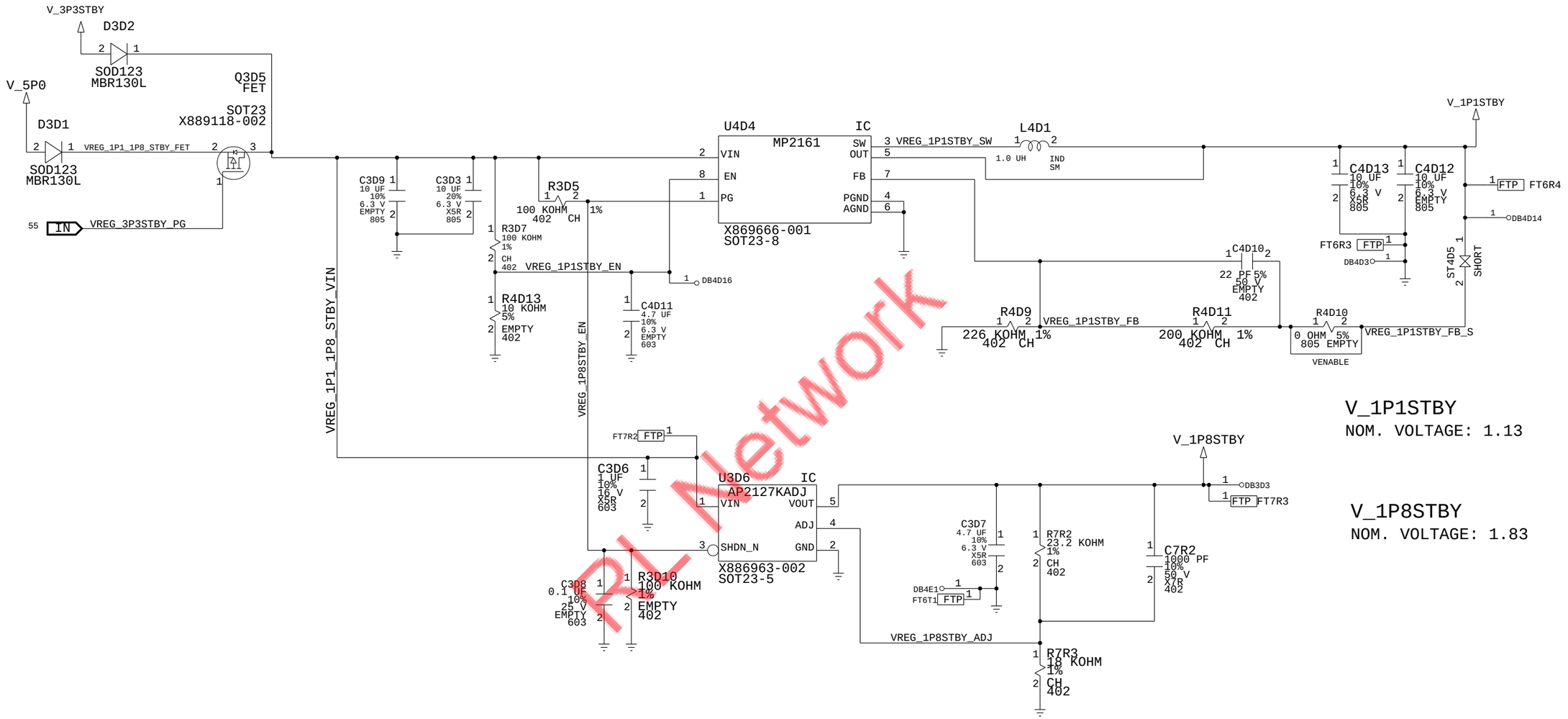
V_3P3STBY
NOM. VOLTAGE: 3.31



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	55/72	55/72	G	1.01

VREGS: V1P1 STANDBY, V1P8 STANDBY



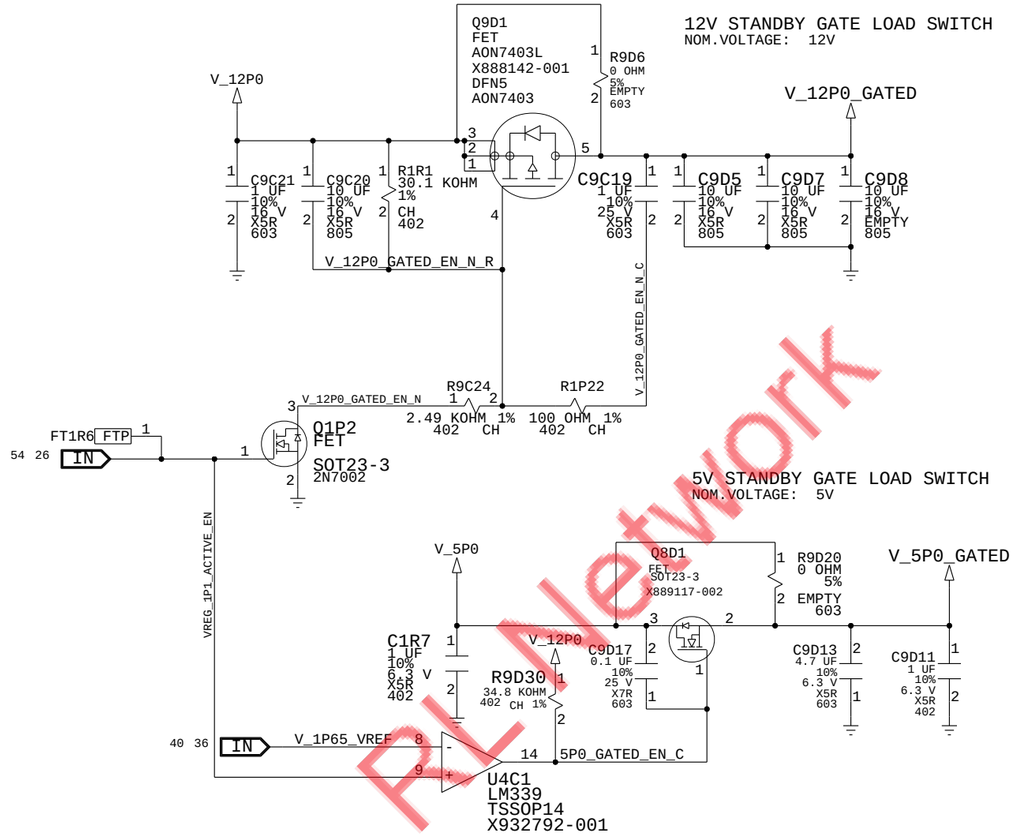
V_1P1STBY
NOM. VOLTAGE: 1.13

V_1P8STBY
NOM. VOLTAGE: 1.83

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	56/72	56/72	G	1.01

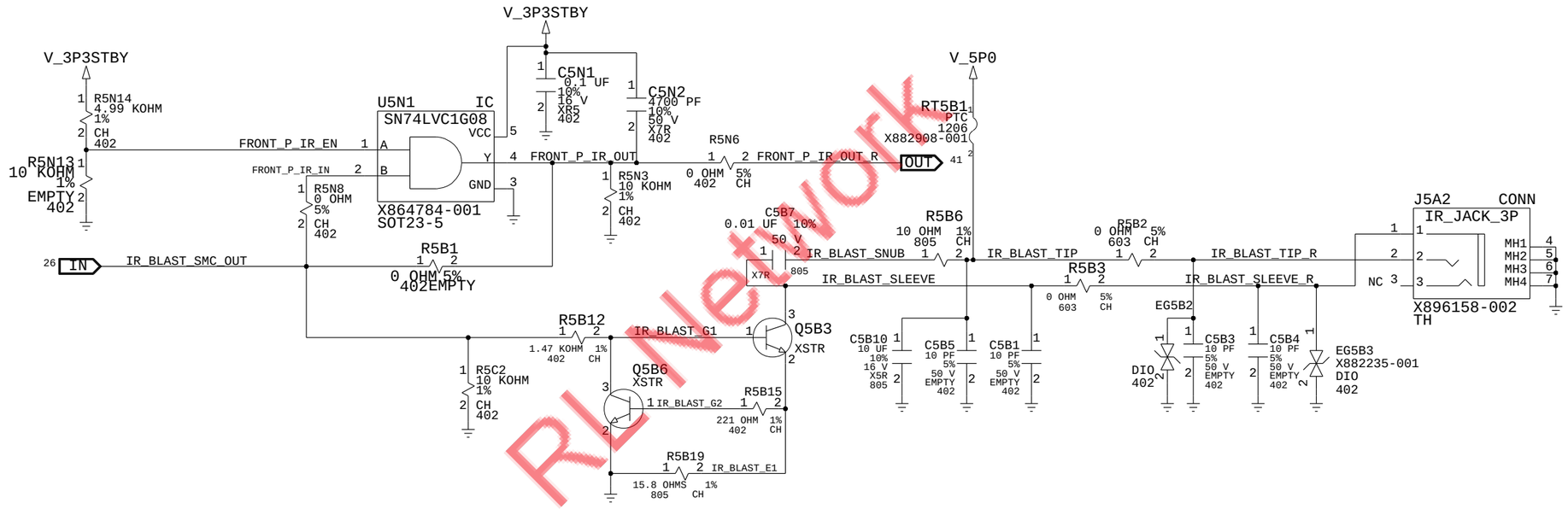
STANDBY GATES



PL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	57/72	57/72	G	1.01

IR BLASTER



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	58/72	58/72	G	1.01

I2C

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RL Network

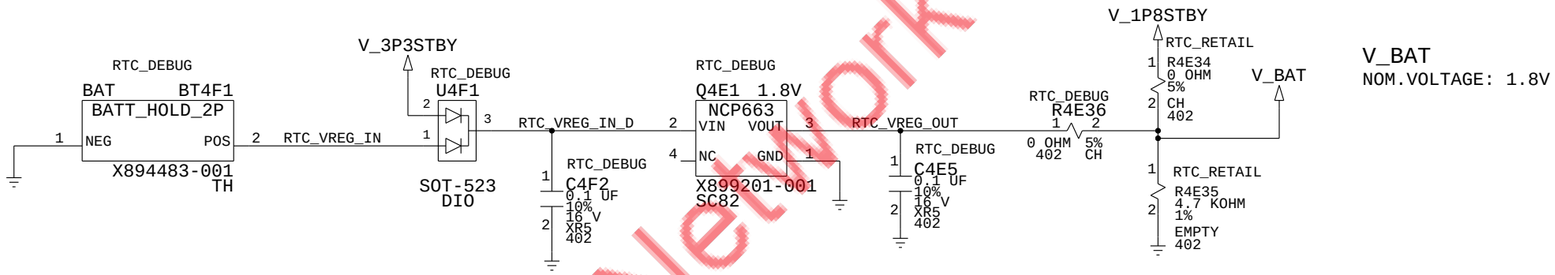
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	59/72	59/72	G	1.01

MARGIN: SOCPHY,SOC1P8,MEMIO,NBCORE

BLANK

RL Network

V_BAT



V_BAT
NOM.VOLTAGE: 1.8V

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X895557-001	BAT	COIN_CELL1	BAT-COIN,OTH,3 V,OTHER,OTH,2032(VARTA QUAL)	BAT_VARTA

VARTA MAXIMUM OPERATING TEMP 70C

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	61/72	61/72	G	1.01

MONITOR: NBCORE,MEMIO

BLANK

RL Network

MONITOR: VSOC1P8,VSOCPHY

BLANK

RL Network

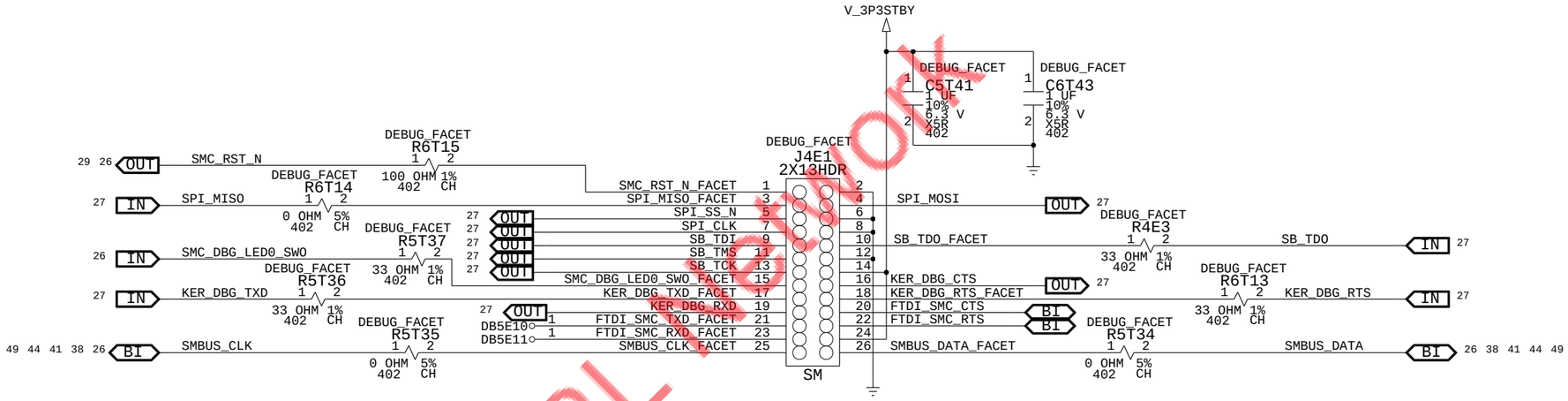
MONITOR: V12P0

BLANK

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	64/72	64/72	G	1.01

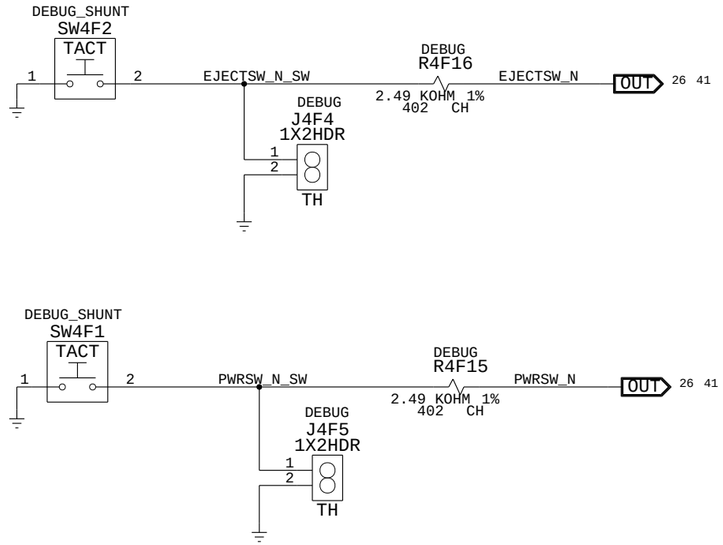
CONN: FACET BOARD

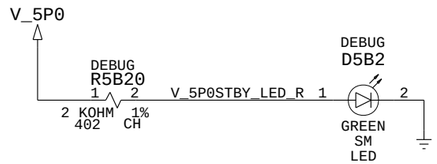


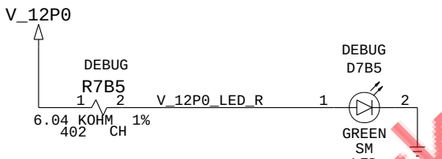
RL Working

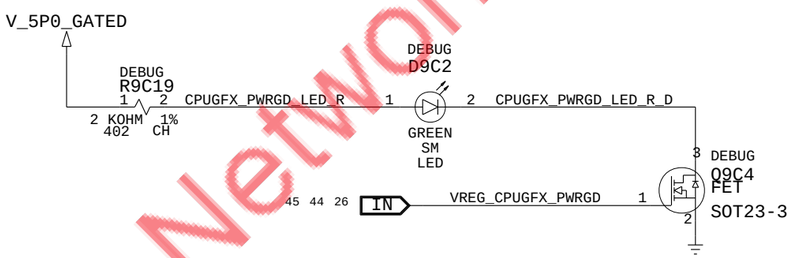
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	65/72	65/72	G	1.01

CONN: SWITCHES





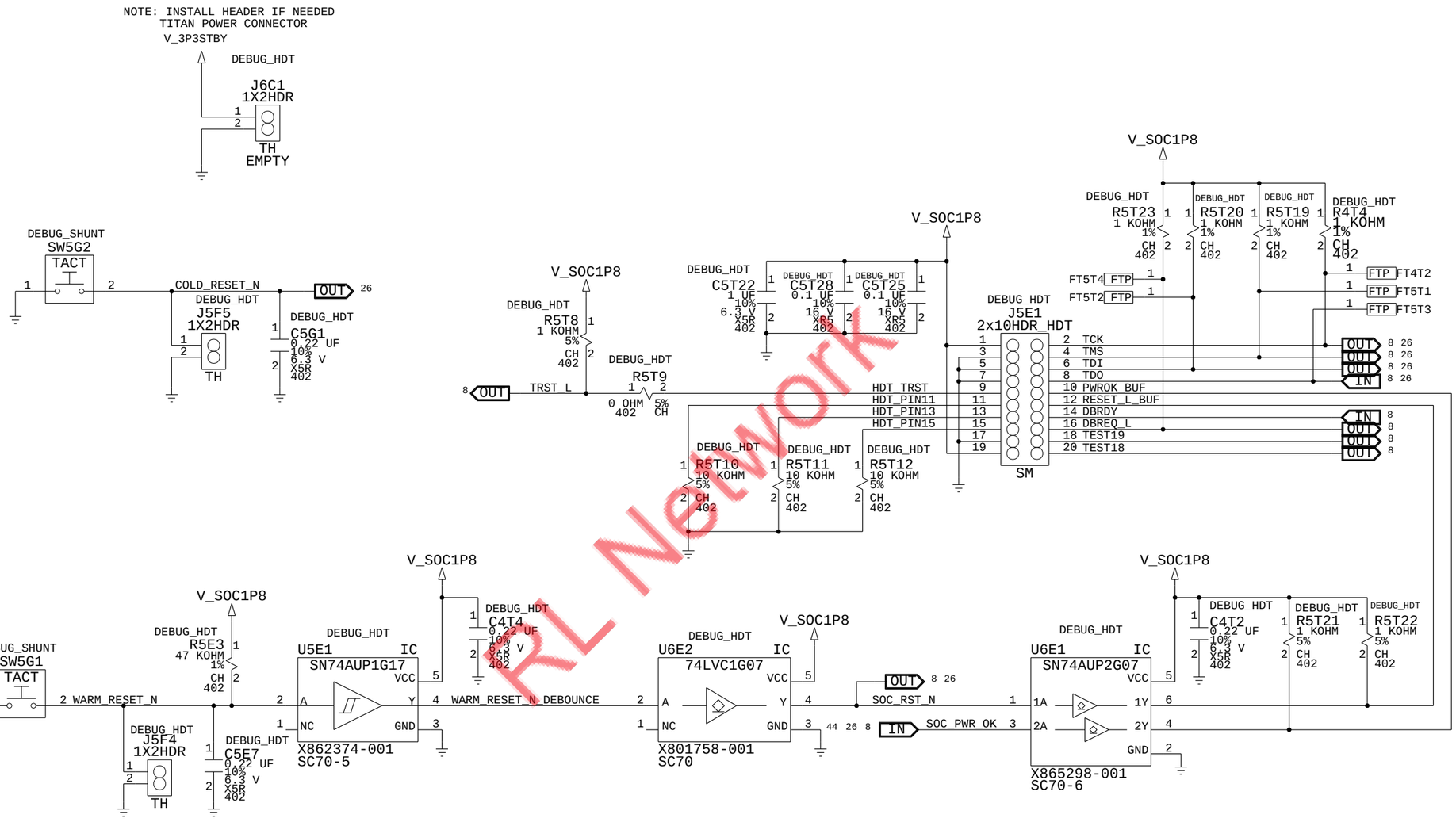




RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	66/72	66/72	G	1.01

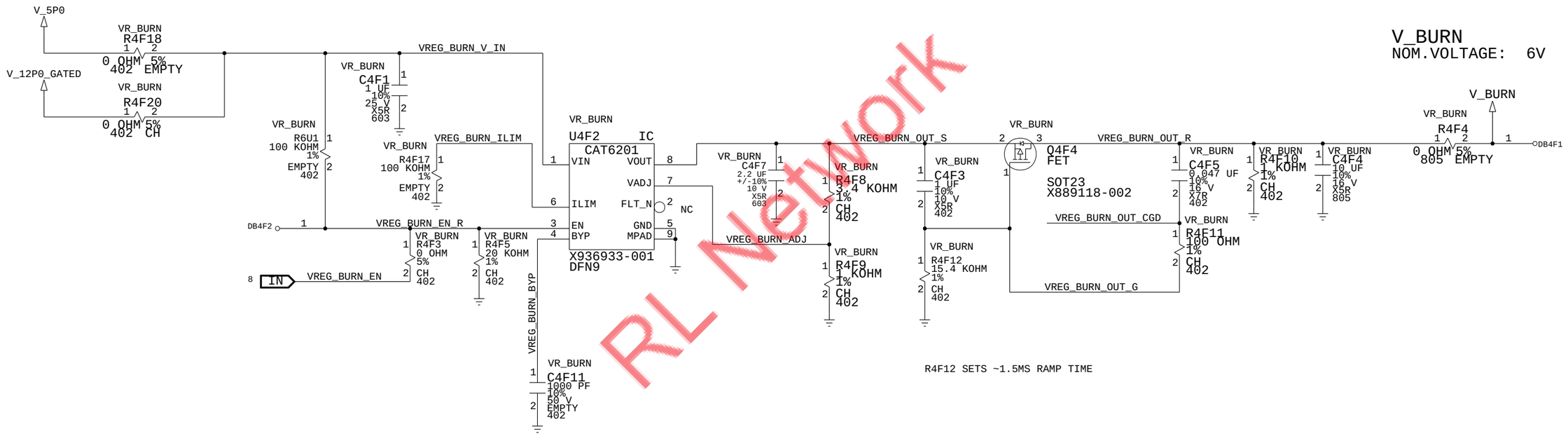
CONN: HDT



Network
RL

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	67/72	67/72	G	1.01

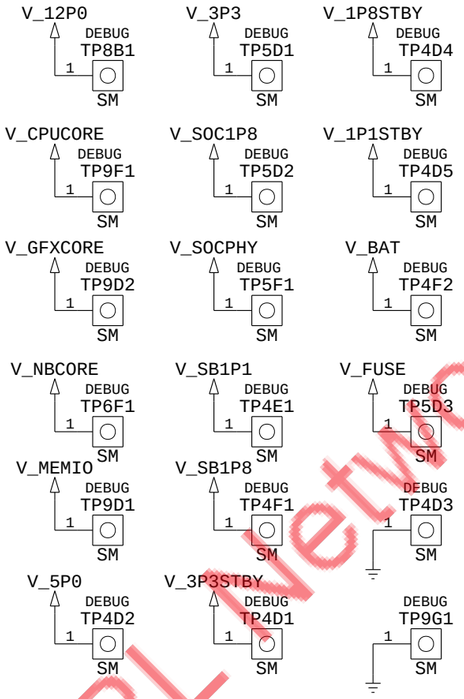
DEBUG: V_BURN



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	68/72	68/72	G	1.01

DEBUG: VR HEADERS & TEST POINTS



RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	69/72	69/72	G	1.01

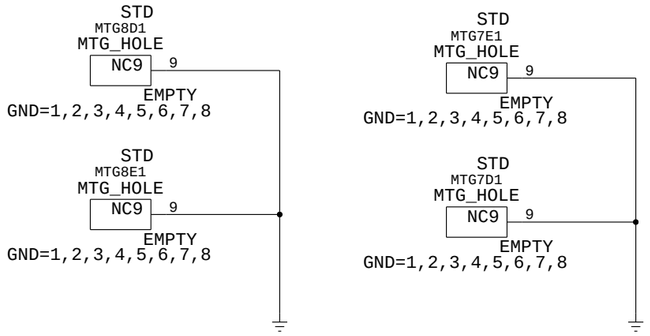
DEBUG: CONNECTORS

BLANK

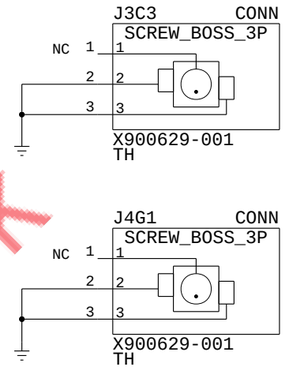
RL Network

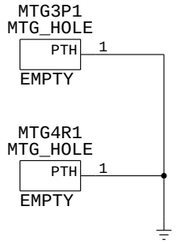
LABELS AND MOUNTING

HEAT SINK MOUNTING HOLES



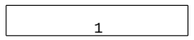
SCREW BOSS





INTELLIGENT SERIAL NUMBER TARGET

LB5G1
X801181-001
LABEL



1375X250_TARGET

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X947889-001	FR4	PCB1	PCB-RIGID,RETAIL,FAB G,6L,FR4,OSP	PCB_OSP

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	71/72	71/72	G	1.01

BOM DEFINITIONS

BOM	DEFINTION
AUX	HDMI STUFFING OPTION. NEVER USED IN PRODUCTION. REWORK PURPOSES ONLY
COMMON	ALL COMPONENTS WITH NO BOM PROPERTY
DDC	HDMI STUFFING OPTION. ALWAYS USED IN PRODUCTION
DDR_BASE	DUMMY PLACE HOLDER FOR DDR3 DEVICES. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE 3 INSTEAD: DDR_HYNIX, DDR_MICRON, DDR_SAMSUNG
DDR_HYNIX	HYNIX DDR3
DDR_MICRON	MICRON DDR3
DDR_SAMSUNG	SAMSUNG DDR3
DEBUG	COMPONENTS REQUIRED FOR BRING UP & DEBUG
DEBUG_HDT	HDT-RELATED DEBUG COMPONENTS
DEBUG_HDMI	DEBUG HDMI CONNECTOR USED 8L DEBUG BOARDS
DEBUG_SHUNT	COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL
EMMC_BASE	DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_20NM, EMMC_HYNIX_5P0, EMMC_HYNIX_1XNM, EMMC_SAMSUNG AND EMMC_TOSHIBA
EMMC_HYNIX_5P0	HYNIX EMMC V5.0 EMMC DEVICE
FET_BASE	DUMMY PLACE HOLDER FOR HIGH AND LOW FETS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: FET_AOS, FET_OS_T6, FET_STM, OR FET_TOS
FET_IRF	INTERNATIONAL RECTIFIER FETS USED FOR VOLTAGE REGUALTORS
FET_OS_T6	ON-SEMI T6 FETS USED FOR VOLTAGE REGULATORS
FET_STM	STMICROELECTRONICS FETS USED FOR VOLTAGE REGULATORS
FET_TOS	TOSHIBA FETS USED FOR VOLTAGE REGULATORS
GARFIELD	CONTAINS GARFIELD (SOC) RELATED PASSIVE/ACTIVE COMPONENTS
KIC_BASE	DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL
KIC_DEV	DEBUG VERSION OF KRAKEN
KIC_RETAIL	RETAIL VERSION OF KRAKEN
MEM_FIXED	SETS V_MEMIO TO A FIXED VOLTAGE (NON-MARGINED). MUST BE USED IN CONJUNCTION WITH NOT MEM_MM
MEM_MM	ALLOWS V_MEMIO TO BE MARGINED FOR M&M BOARDS. MUST BE USED IN CONJUNCTION WITH NOT MEM_FIXED
PANTHER	CONTAINS PANTHER (SOC) RELATED PASSIVE/ACTIVE COMPONENTS
PANTHER_SOC	PANTHER SYSTEM-ON-CHIP (SOC)
PANTHER_SOC_LP	PANTHER SYSTEM-ON-CHIP (SOC) LOW POWER VERSION
PCB_GI	FAB TYPE: GOLD
PCB_OSP	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE
RTC_RETAIL	RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS
RTC_DEBUG	RTC CIRCUIT IMPLEMENTATION FOR DEBUG BOARDS
SOC_BASE	DUMMY PLACE HOLDER FOR SOC
VR_FIXED	SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM
VR_MM	ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED
VRTB	BOOT STRAPPING RESISTOR ONLY TO BE POPULATED WHEN BUILDING VOLTAGE REGULATOR TEST BOARD WHICH CONTAINS NO SOC
WW	CAPACITORS WHICH NEED TO BE NO-STUFFED WHEN AI CPU/GPU SOCKET IS INSTALLED

RL Network

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Kingston	72/72	72/72	G	1.01