TRINITY
REV 1.01
FAB G RETAIL

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[3]	GCPU, DEBUG BUS
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[7]	GCPU, PWR
[8]	GCPU, PWR
[9]	GCPU, DECOUPLING
[10]	GCPU, DECOUPLING
[11]	GCPU, DECOUPLING
[12]	GCPU, MEMORY CONTROLLER A + B
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[17]	MEMORY PARTITION B, BOTTOM
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[47]	VREGS, V5P0
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[51]	VREGS, VCS
[52]	VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE
[53]	VREGS, STANDBY SWITCHERS
[54]	BOARD, DECOUPLING
[55]	MARGIN, VMEM + VEDRAM
[56]	MARGIN, V3P3 + V5P0
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[60]	XDK, DEBUG TITAN
[61]	DEBUG BOARD, SPYDER CONN
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RULES: (APPLIED WHEN POSSIBLE)
1.) MSB TO LSB IS TOP TO BOTTOM
2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7.) SUFFIX _V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12.) SUFFIX _P FOR P JUNCTION
13.) SUFFIX _EN FOR ENABLE
14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15.) PWRGD FOR POWER GOOD
16.) REV AND FAB ARE SET USING CUSTOM VARIABLES. TOOLS>OPTIONS>VARIABLES

[PAGE_TITLE=COVER PAGE]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	1/81	G	1.01

GCPU SETUP

27 IN CPU_RST_N
FT4R2 FTP 1
R4D4 2 1 1.27 KOHM 1% 402 CH
C5R11 1 2 360 PF 5% 50 V EMPTY 603
R4D5 1 2 2 KOHM 1% CH 402
CPU_RST_V1P1_N OUT 60

27 IN CPU_PWRGD
FT5R18 FTP 1
C4T1 1 2 360 PF 5% 50 V EMPTY 603

22 IN CPU_CLK_DP
R4D1 2 1 0 OHM 5% 402 CH
IN CPU_CLK_DP_R2

22 IN CPU_CLK_DN
R4D2 2 1 0 OHM 5% 402 CH
IN CPU_CLK_DN_R2

U5E1 14 OF 17 IC
GCPU VERSION 1

D5 HARD_RESET_B
T5 POWER_GOOD
P2 CPU_CLK_DP
P1 CPU_CLK_DN

E5 CHECKSTOP_B → CPU_CHECKSTOP_N OUT 60

VID6 C24 → CPU_VREG_APS6 OUT 43
VID5 B24 → CPU_VREG_APS5 OUT 43
VID4 A24 → CPU_VREG_APS4 OUT 43
VID3 C23 → CPU_VREG_APS3 OUT 43
VID2 B23 → CPU_VREG_APS2 OUT 43
VID1 A23 → CPU_VREG_APS1 OUT 43

1 1 FTP FT7P8
1 1 FTP FT7P7
1 1 FTP FT7P6
1 1 FTP FT7P5
1 1 FTP FT7P4
1 1 FTP FT7P3

CPU_DBG_RST_EN	INTERNAL PULLDN
GPU_DBG_RST_EN	INTERNAL PULLDN

OUT CPU_DBG_RST_EN → P5 CPU_DBG_RST_EN<DN>
OUT GPU_DBG_RST_EN → R5 GPU_DBG_RST_EN<DN>

OUT EDRAM_PSRO_DOUT → N6 PSRO_DOUT
OUT CPU_PSRO0_OUT → G7 PSRO0_OUT

V_CPUPLL
WHEN V_CPUPLL=1.83V
SET VGATE=1.20V
ACTUAL=1.202V
R4T5 1 2 562 OHM 1% CH 402
N: IF V_CPUPLL CHANGES
VGATE RESISTORS SHOULD BE ADJUSTED
CPU_VGATE
FT4T2 FTP 1
R4T6 1 2 1.07 KOHM 1% CH 402

<DN>PULSE_LIMIT_BYPASS
J6 → CPU_LIMIT_BYPASS OUT
V6 V_GATE <DN>PLL_BYPASS
F8 → CPU_PLL_BYPASS OUT

OUT RESISTOR0_DP → L7 RESISTOR0_DP
OUT RESISTOR0_DN → M7 RESISTOR0_DN
SRVID A3 → CPU_SRVID OUT 51
EFU_POWERON C1 → VREG_EFUSE_EN OUT 52

OUT CPU_EXT_CLK_EN → F7 EXT_CLK_EN<DN>
CPU_TINIT
J7 TI_39_TINIT
E7 TE CORE_HF_BGR_PLL → M6 CORE_HF_BGR_PLL OUT

1 R5R1 2 200 OHM 5% CH 402

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6 LAYER ONLY SIGNALS

CORE_HF_BGR_PLL	6 LAYER ONLY; TP ONLY
CPU_LIMIT_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_PLL_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_CORE_HF_CLKOUT_DN	6 LAYER ONLY; TP ONLY
CPU_CORE_HF_CLKOUT_DP	6 LAYER ONLY; TP ONLY
CPU_EXT_CLK_EN	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_DLL_SNIF_OUT	6 LAYER ONLY; TP ONLY
CPU_VDDS0_DP	6 LAYER ONLY
CPU_VDDS0_DN	6 LAYER ONLY
CPU_VDDS1_DP	6 LAYER ONLY
CPU_VDDS1_DN	6 LAYER ONLY
RESISTOR0_DP	6 LAYER ONLY
RESISTOR0_DN	6 LAYER ONLY
EDRAM_PSRO_DOUT	6 LAYER ONLY

[PAGE_TITLE=GCPU SETUP]

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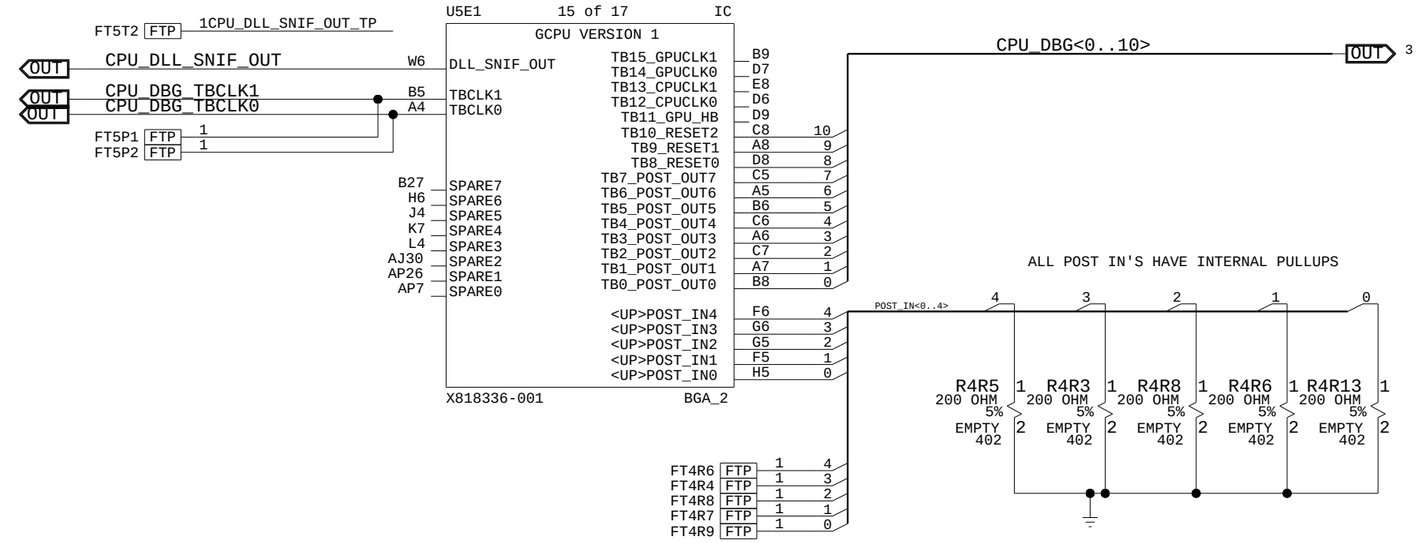
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	2/81	G	1.01

GCPU, DEBUG BUS



[PAGE_TITLE=GCPU, DEBUG BUS]

DRAWING
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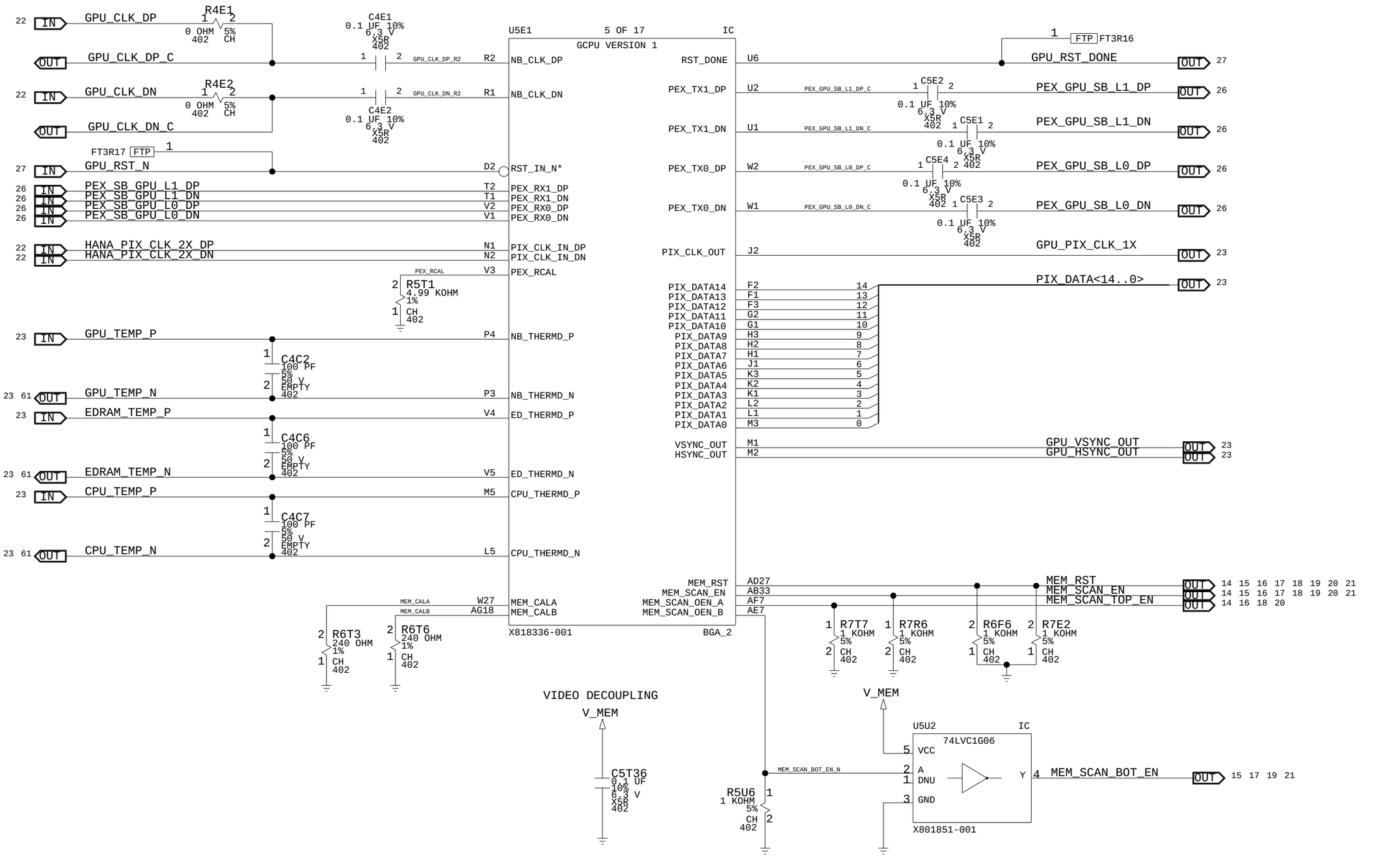
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	3/81	G	1.01

GCPU, VIDEO + PCIEX



[PAGE_TITLE=GCPU, VIDEO + PCIEX]

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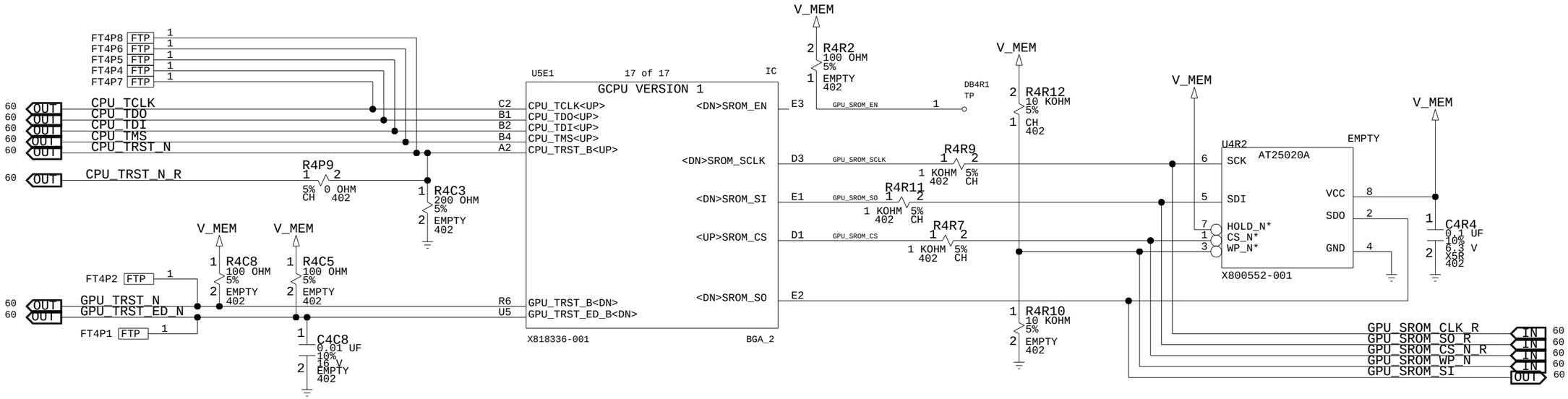
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	4/81	G	1.01

GCPU, EEPROM + JTAG



[PAGE_TITLE=GCPU, EEPROM + JTAG]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	5/81	G	1.01

GCPU, PLL POWER + FSB POWER

V_GPUPCIE V_CPUEDRAM V_CPUPLL V_EFUSE

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GCPU VERSION 1

CPU_VDDS1_DP
CPU_VDDS1_DN
CPU_VDDS0_DP
CPU_VDDS0_DN

E4 VDDE
H25 VDDS1_DP
J26 VDDS1_DN
P7 VDDS0_DP
N7 VDDS0_DN

CORE_HF_CLKOUT_DP L6 → CPU_CORE_HF_CLKOUT_DP
CORE_HF_CLKOUT_DN K6 → CPU_CORE_HF_CLKOUT_DN

FB5R1	V_CPU_PVDDA_MEM	D4	PVDDA_MEM	C5R14 10 UF 20% 6.3 V X5R 805
	V_CPU_PVSSA_MEM	C4	PVSSA_MEM	ST5R1 SHORT
FB5T2	V_CPU_PVDDA_PEX	U3	PVDDA_PEX	C5T9 10 UF 20% 6.3 V X5R 805
	V_CPU_PVSSA_PEX	U4	PVSSA_PEX	ST5T1 SHORT
FB5R2	V_CPU_PVDDA_HS	C3	PVDDA_HS	C5R17 10 UF 20% 6.3 V X5R 805
	V_CPU_PVSSA_HS	B3	PVSSA_HS	ST5R2 SHORT
FB5T3	V_CPU_PVDDA_ED	W5	PVDDA_ED	C5T13 4.7 UF 10% 6.3 V X5R 805
	V_CPU_PVSSA_ED	W4	PVSSA_ED	ST5T2 SHORT
FB5R5	V_CPU_VDDA_RNG	N4	VDDA_RNG	C5R54 10 UF 20% 6.3 V X5R 805
	V_CPU_GNDA_RNG	N3	GNDA_RNG	ST5R5 SHORT
FB5R4	V_CPU_CORE_HF_VDDA_PLL	J5	CORE_HF_VDDA_PLL	C5R42 10 UF 20% 6.3 V X5R 805
	V_CPU_CORE_HF_GNDA_PLL	K5	CORE_HF_GNDA_PLL	ST5R4 SHORT
FB5R3	V_GPU_VDDA_PLL	G4	GPU_VDDA_PLL	C5R31 10 UF 20% 6.3 V X5R 805
	V_GPU_GNDA_PLL	H4	GPU_GNDA_PLL	ST5R3 SHORT
		R3	VDD_VTT	
FB5T1	V_CPU_VDD_VTTA	R4	VDD_VTTA	C5T4 4.7 UF 10% 6.3 V X5R 805; C5T6 0.1 UF 10% 6.3 V X5R 402

All FB: 603, 0.2A, 0.5 DCR

DB5R5

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[PAGE_TITLE=GCPU, PLL POWER + FSB POWER]

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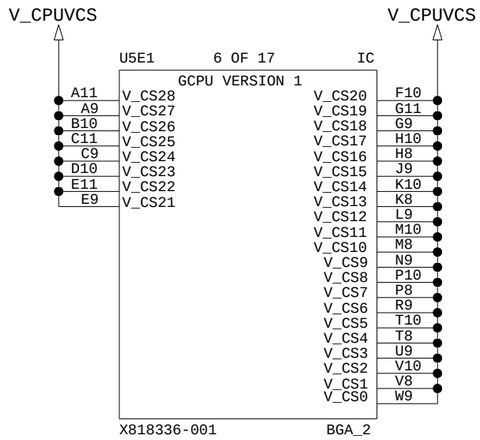
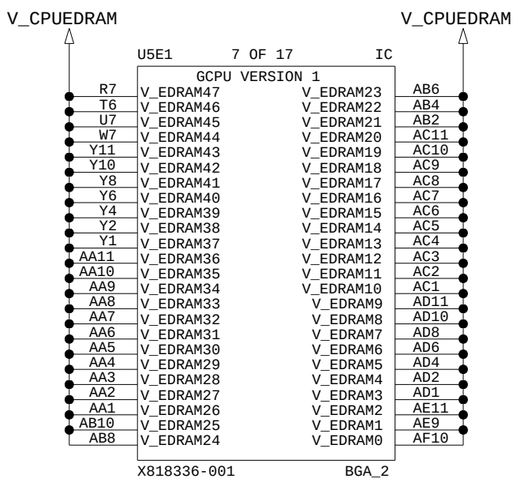
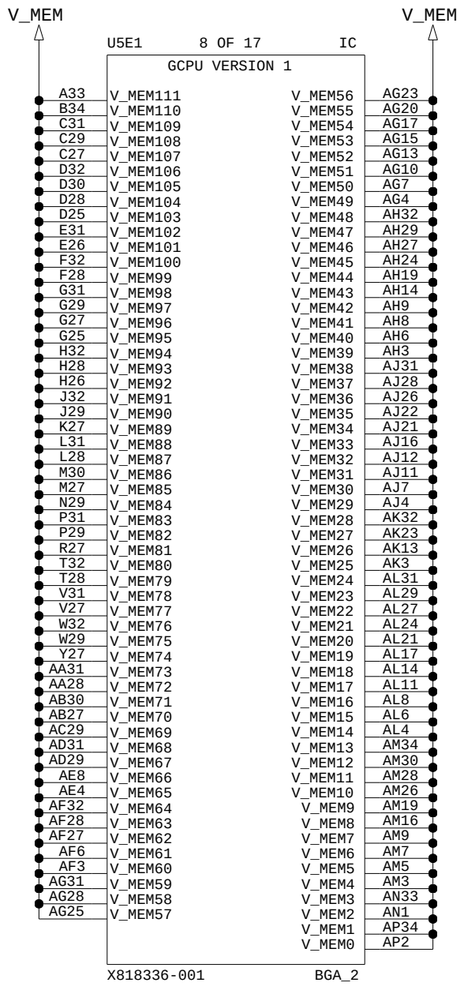
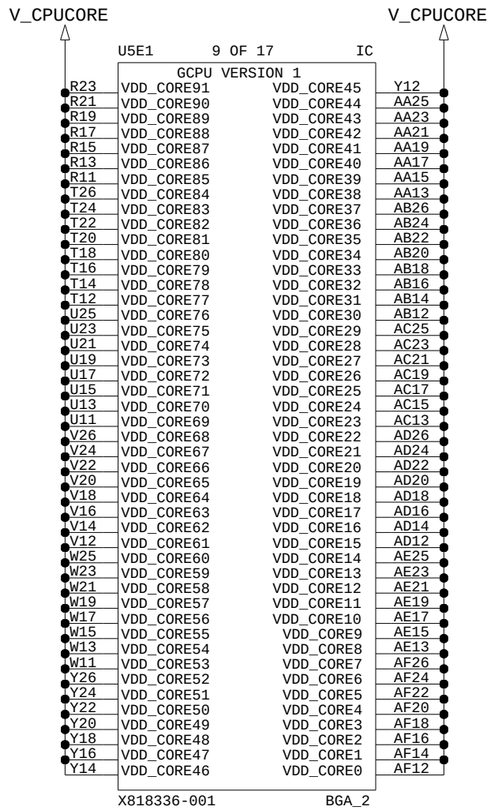
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	6/81	G	1.01

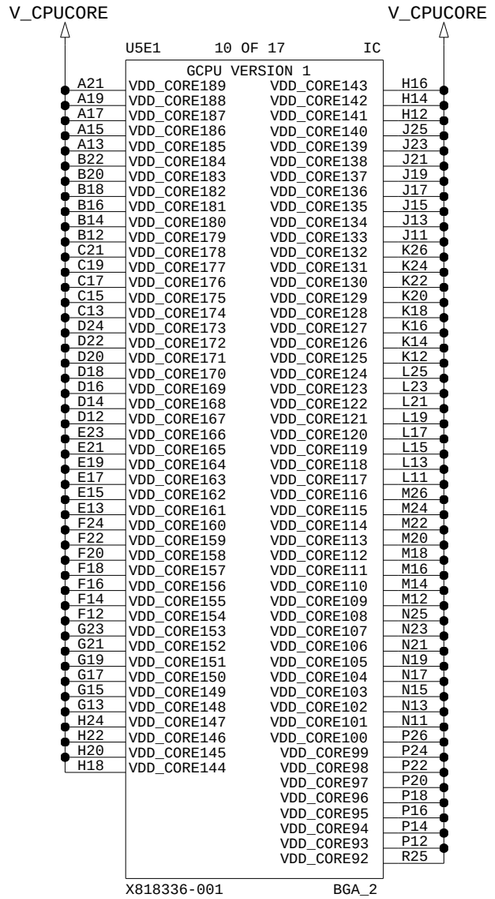
GCPU, POWER











[PAGE_TITLE=GCPU, POWER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	7/81	G	1.01

GCPU, POWER

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GCPU VERSION 1

Y3	VSS130	VSS65	AF15
AA32	VSS129	VSS64	AF13
AA27	VSS128	VSS63	AF11
AA26	VSS127	VSS62	AF9
AA24	VSS126	VSS61	AF8
AA22	VSS125	VSS60	AF4
AA20	VSS124	VSS59	AG32
AA18	VSS123	VSS58	AG29
AA16	VSS122	VSS57	AG27
AA14	VSS121	VSS56	AG26
AA12	VSS120	VSS55	AG24
AB25	VSS119	VSS54	AG22
AB23	VSS118	VSS53	AG21
AB21	VSS117	VSS52	AG19
AB19	VSS116	VSS51	AG16
AB17	VSS115	VSS50	AG14
AB15	VSS114	VSS49	AG12
AB13	VSS113	VSS48	AG11
AB11	VSS112	VSS47	AG9
AB9	VSS111	VSS46	AG8
AB7	VSS110	VSS45	AG6
AB5	VSS109	VSS44	AG3
AB3	VSS108	VSS43	AH31
AB1	VSS107	VSS42	AH28
AC31	VSS106	VSS41	AH7
AC27	VSS105	VSS40	AH4
AC26	VSS104	VSS39	AJ32
AC24	VSS103	VSS38	AJ29
AC22	VSS102	VSS37	AJ27
AC20	VSS101	VSS36	AJ25
AC18	VSS100	VSS35	AJ20
AC16	VSS99	VSS34	AJ17
AC14	VSS98	VSS33	AJ15
AC12	VSS97	VSS32	AJ10
AD32	VSS96	VSS31	AJ8
AD25	VSS95	VSS30	AJ6
AD23	VSS94	VSS29	AJ3
AD21	VSS93	VSS28	AK31
AD19	VSS92	VSS27	AK18
AD17	VSS91	VSS26	AK4
AD15	VSS90	VSS25	AL32
AD13	VSS89	VSS24	AL30
AD9	VSS88	VSS23	AL28
AD7	VSS87	VSS22	AL26
AD5	VSS86	VSS21	AL22
AD3	VSS85	VSS20	AL19
AE29	VSS84	VSS19	AL16
AE27	VSS83	VSS18	AL12
AE26	VSS82	VSS17	AL9
AE24	VSS81	VSS16	AL7
AE22	VSS80	VSS15	AL5
AE20	VSS79	VSS14	AL3
AE18	VSS78	VSS13	AM33
AE16	VSS77	VSS12	AM31
AE14	VSS76	VSS11	AM29
AE12	VSS75	VSS10	AM27
AE10	VSS74	VSS9	AM24
AE6	VSS73	VSS8	AM21
AE3	VSS72	VSS7	AM14
AF31	VSS71	VSS6	AM11
AF25	VSS70	VSS5	AM8
AF23	VSS69	VSS4	AM6
AF21	VSS68	VSS3	AM4
AF19	VSS67	VSS2	AN34
AF17	VSS66	VSS1	AP33
		VSS0	AP1

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GCPU VERSION 1

K29	VSS260	VSS195	R16
K25	VSS259	VSS194	R14
K23	VSS258	VSS193	R12
K21	VSS257	VSS192	R10
K19	VSS256	VSS191	R8
K17	VSS255	VSS190	T31
K15	VSS254	VSS189	T27
K13	VSS253	VSS188	T25
K11	VSS252	VSS187	T23
K9	VSS251	VSS186	T21
K4	VSS250	VSS185	T19
L32	VSS249	VSS184	T17
L27	VSS248	VSS183	T15
L26	VSS247	VSS182	T13
L24	VSS246	VSS181	T11
L22	VSS245	VSS180	T9
L20	VSS244	VSS179	T7
L18	VSS243	VSS178	T4
L16	VSS242	VSS177	T3
L14	VSS241	VSS176	U30
L12	VSS240	VSS175	U27
L10	VSS239	VSS174	U26
L8	VSS238	VSS173	U24
L3	VSS237	VSS172	U22
M25	VSS236	VSS171	U20
M23	VSS235	VSS170	U18
M21	VSS234	VSS169	U16
M19	VSS233	VSS168	U14
M17	VSS232	VSS167	U12
M15	VSS231	VSS166	U10
M13	VSS230	VSS165	U8
M11	VSS229	VSS164	V29
M9	VSS228	VSS163	V25
M4	VSS227	VSS162	V23
N31	VSS226	VSS161	V21
N27	VSS225	VSS160	V19
N26	VSS224	VSS159	V17
N24	VSS223	VSS158	V15
N22	VSS222	VSS157	V13
N20	VSS221	VSS156	V11
N18	VSS220	VSS155	V9
N16	VSS219	VSS154	V7
N14	VSS218	VSS153	W31
N12	VSS217	VSS152	W26
N10	VSS216	VSS151	W24
N8	VSS215	VSS150	W22
N5	VSS214	VSS149	W20
P32	VSS213	VSS148	W18
P27	VSS212	VSS147	W16
P25	VSS211	VSS146	W14
P23	VSS210	VSS145	W12
P21	VSS209	VSS144	W10
P19	VSS208	VSS143	W8
P17	VSS207	VSS142	W3
P15	VSS206	VSS141	Y29
P13	VSS205	VSS140	Y25
P11	VSS204	VSS139	Y23
P9	VSS203	VSS138	Y21
P6	VSS202	VSS137	Y19
R29	VSS201	VSS136	Y17
R26	VSS200	VSS135	Y15
R24	VSS199	VSS134	Y13
R22	VSS198	VSS133	Y9
R20	VSS197	VSS132	Y7
R18	VSS196	VSS131	Y5

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GCPU VERSION 1

A34	VSS354	VSS318	E24
A22	VSS353	VSS317	E22
A20	VSS352	VSS316	E20
A18	VSS351	VSS315	E18
A16	VSS350	VSS314	E16
A14	VSS349	VSS313	E14
A12	VSS348	VSS312	E12
A10	VSS347	VSS311	E10
B33	VSS346	VSS310	E6
B21	VSS345	VSS309	F31
B19	VSS344	VSS308	F29
B17	VSS343	VSS307	F27
B15	VSS342	VSS306	F23
B13	VSS341	VSS305	F21
B11	VSS340	VSS304	F19
B7	VSS339	VSS303	F17
C28	VSS338	VSS302	F15
C25	VSS337	VSS301	F13
C22	VSS336	VSS300	F11
C20	VSS335	VSS299	F9
C18	VSS334	VSS298	F4
C16	VSS333	VSS297	G32
C14	VSS332	VSS296	G28
C12	VSS331	VSS295	G24
C10	VSS330	VSS294	G22
D31	VSS329	VSS293	G20
D29	VSS328	VSS292	G18
D27	VSS327	VSS291	G16
D23	VSS326	VSS290	G14
D21	VSS325	VSS289	G12
D19	VSS324	VSS288	G10
D17	VSS323	VSS287	G8
D15	VSS322	VSS286	G3
D13	VSS321	VSS285	H31
D11	VSS320	VSS284	H29
E32	VSS319	VSS283	H27
		VSS282	H23
		VSS281	H21
		VSS280	H19
		VSS279	H17
		VSS278	H15
		VSS277	H13
		VSS276	H11
		VSS275	H9
		VSS274	H7
		VSS273	J31
		VSS272	J27
		VSS271	J24
		VSS270	J22
		VSS269	J20
		VSS268	J18
		VSS267	J16
		VSS266	J14
		VSS265	J12
		VSS264	J10
		VSS263	J8
		VSS261	J3

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[PAGE_TITLE=GCPU, POWER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	8/81	G	1.01

GCPU, DECOUPLING

V_CPUCORE

C6R4 1 2 4.7 UF 10% 6.3 V X5R 805
C5D13 1 2 4.7 UF 10% 6.3 V X5R 805
C5R8 1 2 4.7 UF 10% 6.3 V X5R 805
C5R9 1 2 4.7 UF 10% 6.3 V X5R 805
C5R15 1 2 4.7 UF 10% 6.3 V X5R 805
C5D14 1 2 4.7 UF 10% 6.3 V X5R 805
C6D3 1 2 4.7 UF 10% 6.3 V X5R 805
C5D7 1 2 4.7 UF 10% 6.3 V X5R 805
C6R3 1 2 4.7 UF 10% 6.3 V X5R 805
C5D3 1 2 4.7 UF 10% 6.3 V X5R 805
C5R7 1 2 4.7 UF 10% 6.3 V X5R 805
C5D6 1 2 4.7 UF 10% 6.3 V X5R 805
C5R10 1 2 4.7 UF 10% 6.3 V X5R 805
C5D8 1 2 4.7 UF 10% 6.3 V X5R 805
C6R6 1 2 4.7 UF 10% 6.3 V X5R 805
C5D5 1 2 4.7 UF 10% 6.3 V X5R 805
C5D12 1 2 4.7 UF 10% 6.3 V X5R 805
C5R6 1 2 4.7 UF 10% 6.3 V X5R 805
C6D4 1 2 4.7 UF 10% 6.3 V X5R 805
C5D9 1 2 4.7 UF 10% 6.3 V X5R 805
C6R2 1 2 4.7 UF 10% 6.3 V X5R 805
C5R5 1 2 4.7 UF 10% 6.3 V X5R 805
C6R1 1 2 4.7 UF 10% 6.3 V X5R 805
C5R18 1 2 4.7 UF 10% 6.3 V X5R 805
C5R12 1 2 4.7 UF 10% 6.3 V X5R 805
C5D2 1 2 4.7 UF 10% 6.3 V X5R 805
C5R3 1 2 4.7 UF 10% 6.3 V X5R 805
C5D10 1 2 4.7 UF 10% 6.3 V X5R 805
C6D5 1 2 4.7 UF 10% 6.3 V X5R 805
C5R16 1 2 4.7 UF 10% 6.3 V X5R 805
C6R7 1 2 4.7 UF 10% 6.3 V X5R 805
C5D11 1 2 4.7 UF 10% 6.3 V X5R 805
C6D1 1 2 4.7 UF 10% 6.3 V X5R 805
C6D2 1 2 4.7 UF 10% 6.3 V X5R 805
C6D6 1 2 4.7 UF 10% 6.3 V X5R 805
C5T33 1 2 4.7 UF 10% 6.3 V X5R 805
C6R5 1 2 4.7 UF 10% 6.3 V X5R 805
C5R13 1 2 4.7 UF 10% 6.3 V X5R 805
C5R2 1 2 4.7 UF 10% 6.3 V X5R 805
C6T22 1 2 4.7 UF 10% 6.3 V X5R 805
C6T23 1 2 4.7 UF 10% 6.3 V X5R 805

V_CPUEDRAM

C5T26 1 2 0.1 UF 10% 6.3 V X5R 402
C5E6 1 2 4.7 UF 10% 6.3 V X5R 805
C5T32 1 2 0.1 UF 10% 6.3 V X5R 402
C5E5 1 2 4.7 UF 10% 6.3 V X5R 805
C5T24 1 2 0.1 UF 10% 6.3 V X5R 402
C5T35 1 2 4.7 UF 10% 6.3 V X5R 805
C5T31 1 2 0.1 UF 10% 6.3 V X5R 402
C5E7 1 2 4.7 UF 10% 6.3 V X5R 805
C5T27 1 2 0.1 UF 10% 6.3 V X5R 402
C5T34 1 2 4.7 UF 10% 6.3 V X5R 805
C5T22 1 2 0.1 UF 10% 6.3 V X5R 402
C5T43 1 2 4.7 UF 10% 6.3 V X5R 805
C5T23 1 2 0.1 UF 10% 6.3 V X5R 402
C5E8 1 2 4.7 UF 10% 6.3 V X5R 805
C5T20 1 2 0.1 UF 10% 6.3 V X5R 402
C5E9 1 2 4.7 UF 10% 6.3 V X5R 805
C5T25 1 2 0.1 UF 10% 6.3 V X5R 402
C4T3 1 2 4.7 UF 10% 6.3 V X5R 805
C5T21 1 2 0.1 UF 10% 6.3 V X5R 402
C4T4 1 2 4.7 UF 10% 6.3 V X5R 805

V_CPUVCS

C5R35 1 2 0.1 UF 10% 6.3 V X5R 402
C5D1 1 2 4.7 UF 10% 6.3 V X5R 805
C5R58 1 2 0.1 UF 10% 6.3 V X5R 402
C5R4 1 2 4.7 UF 10% 6.3 V X5R 805
C5R43 1 2 0.1 UF 10% 6.3 V X5R 402
C5D4 1 2 4.7 UF 10% 6.3 V X5R 805
C5T7 1 2 0.1 UF 10% 6.3 V X5R 402
C5R1 1 2 4.7 UF 10% 6.3 V X5R 805
C5R50 1 2 0.1 UF 10% 6.3 V X5R 402
C5T1 1 2 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	9/81	G	1.01

GCPU, DECOUPLING

V_CPUCORE

C5T12	C5R26	C5T17	C5T10	C6R36
C5R33	C6R25	C6T11	C5T8	C5R63
C5R39	C5R60	C6R42	C6R45	C5R28
C5R40	C5R61	C5R37	C5R49	C5R59
C6T7	C6T20	C6R37	C6R33	C5R27
C5R38	C5R32	C5R57	C6T8	C5R62
C6T12	C6T6	C5R64	C6R15	C5R55
C6R31	C6R28	C5R46	C6R21	C5R51
C6R38	C5R36	C5R45	C6R20	C6R18
C6R43	C5T11	C6T14	C6R44	C6R17

Each: 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	10/81	G	1.01

GCPU, DECOUPLING

V_CPUCORE

C5R25 1 2 0.1 UF 10% 6.3 V X5R 402
C6R8 1 2 0.1 UF 10% 6.3 V X5R 402
C6R39 1 2 0.1 UF 10% 6.3 V X5R 402
C5R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6T5 1 2 0.1 UF 10% 6.3 V X5R 402
C5T14 1 2 0.1 UF 10% 6.3 V X5R 402

C6T15 1 2 0.1 UF 10% 6.3 V X5R 402
C6R34 1 2 0.1 UF 10% 6.3 V X5R 402
C6T3 1 2 0.1 UF 10% 6.3 V X5R 402
C5R52 1 2 0.1 UF 10% 6.3 V X5R 402
C5R21 1 2 0.1 UF 10% 6.3 V X5R 402
C6T9 1 2 0.1 UF 10% 6.3 V X5R 402

C5T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R35 1 2 0.1 UF 10% 6.3 V X5R 402
C5T15 1 2 0.1 UF 10% 6.3 V X5R 402
C5T16 1 2 0.1 UF 10% 6.3 V X5R 402
C5T3 1 2 0.1 UF 10% 6.3 V X5R 402

C6T18 1 2 0.1 UF 10% 6.3 V X5R 402
C5R53 1 2 0.1 UF 10% 6.3 V X5R 402
C6R22 1 2 0.1 UF 10% 6.3 V X5R 402
C5T28 1 2 0.1 UF 10% 6.3 V X5R 402
C6T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R13 1 2 0.1 UF 10% 6.3 V X5R 402

C6R9 1 2 0.1 UF 10% 6.3 V X5R 402
C5T30 1 2 0.1 UF 10% 6.3 V X5R 402
C5R44 1 2 0.1 UF 10% 6.3 V X5R 402
C5R41 1 2 0.1 UF 10% 6.3 V X5R 402
C6T25 1 2 0.1 UF 10% 6.3 V X5R 402
C5R34 1 2 0.1 UF 10% 6.3 V X5R 402

C6R10 1 2 0.1 UF 10% 6.3 V X5R 402
C5T29 1 2 0.1 UF 10% 6.3 V X5R 402
C5R47 1 2 0.1 UF 10% 6.3 V X5R 402
C6R24 1 2 0.1 UF 10% 6.3 V X5R 402
C6R12 1 2 0.1 UF 10% 6.3 V X5R 402
C6R14 1 2 0.1 UF 10% 6.3 V X5R 402

C5R20 1 2 0.1 UF 10% 6.3 V X5R 402
C5R24 1 2 0.1 UF 10% 6.3 V X5R 402
C5R48 1 2 0.1 UF 10% 6.3 V X5R 402
C6T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T5 1 2 0.1 UF 10% 6.3 V X5R 402

C5R19 1 2 0.1 UF 10% 6.3 V X5R 402
C5R56 1 2 0.1 UF 10% 6.3 V X5R 402
C6R26 1 2 0.1 UF 10% 6.3 V X5R 402
C6T16 1 2 0.1 UF 10% 6.3 V X5R 402
C6T17 1 2 0.1 UF 10% 6.3 V X5R 402
C6T13 1 2 0.1 UF 10% 6.3 V X5R 402

C5R22 1 2 0.1 UF 10% 6.3 V X5R 402
C6T4 1 2 0.1 UF 10% 6.3 V X5R 402
C6R32 1 2 0.1 UF 10% 6.3 V X5R 402
C5T18 1 2 0.1 UF 10% 6.3 V X5R 402
C6R40 1 2 0.1 UF 10% 6.3 V X5R 402
C6T24 1 2 0.1 UF 10% 6.3 V X5R 402

C5R23 1 2 0.1 UF 10% 6.3 V X5R 402
C5R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6R41 1 2 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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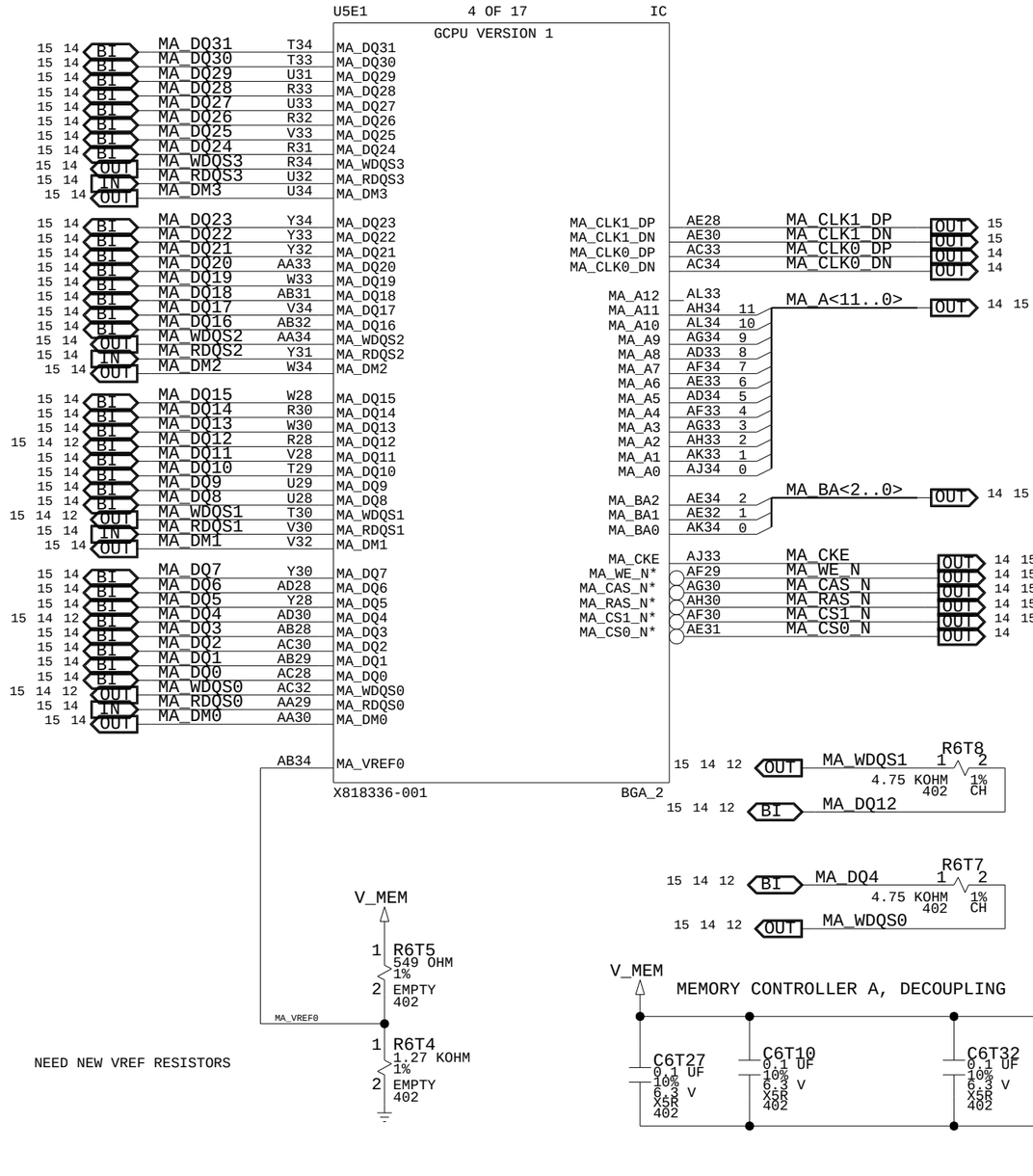
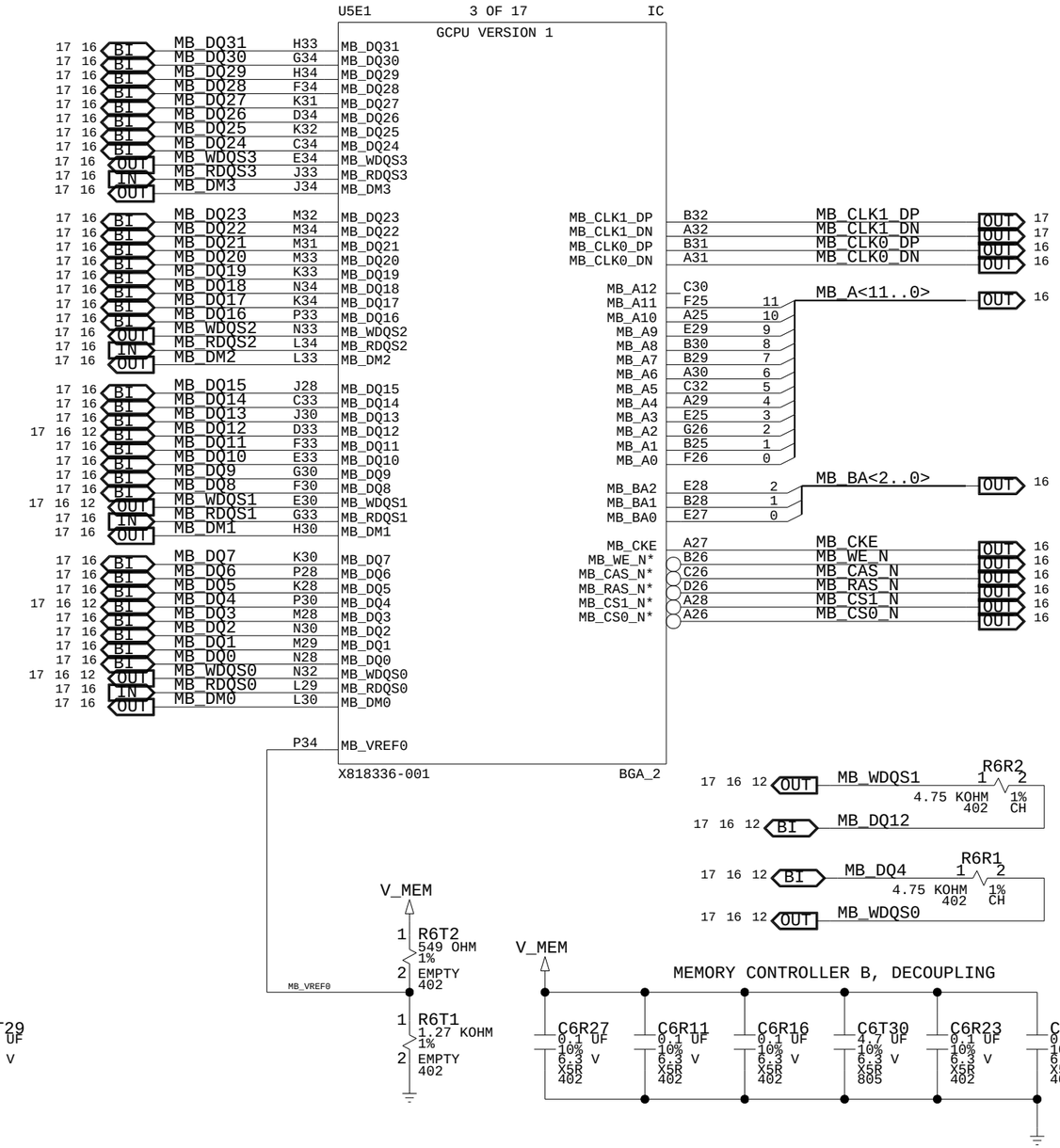
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	11/81	G	1.01

GPU, MEMORY CONTROLLER 0 PARTITION A & B





TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

DRAWING
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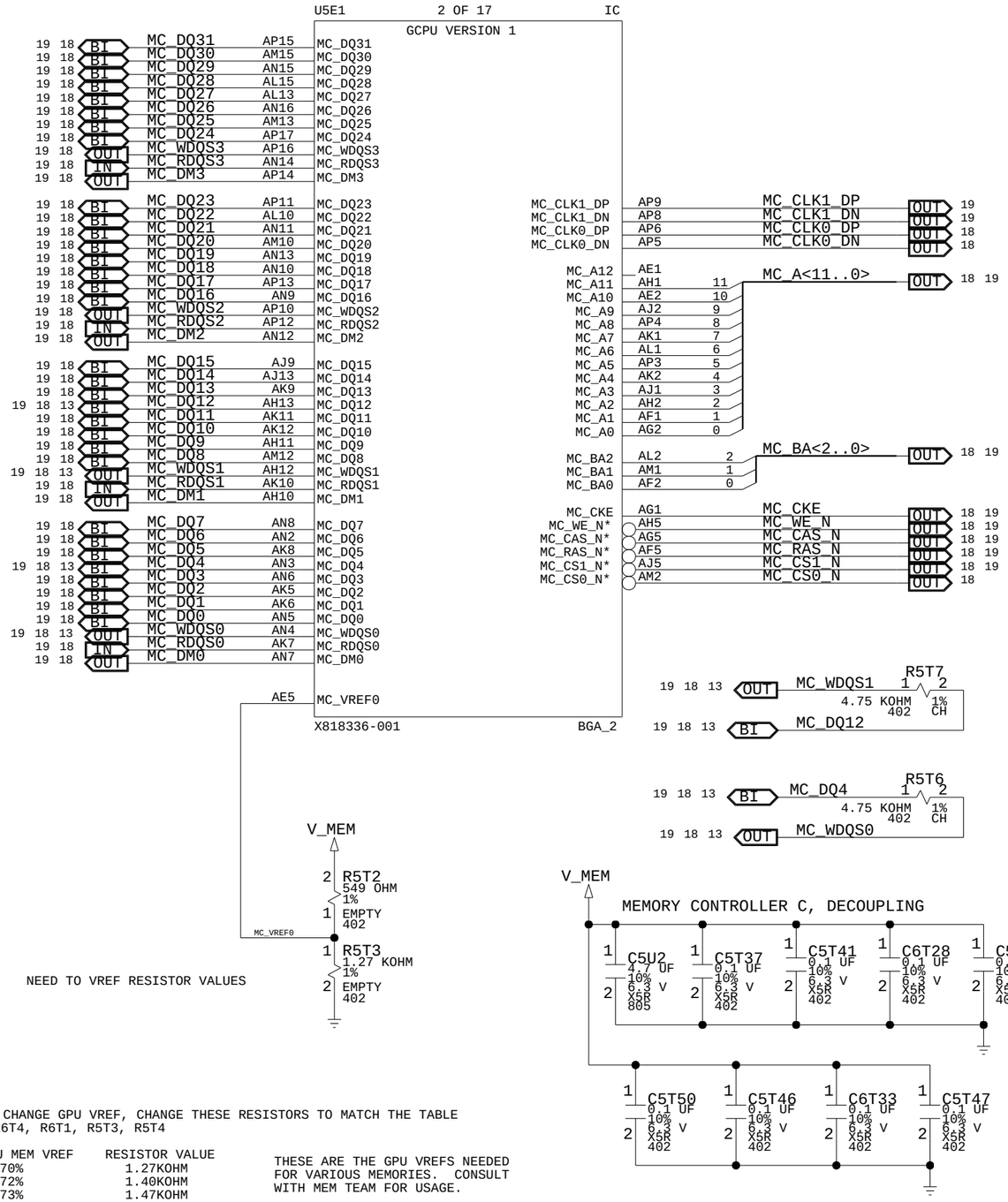
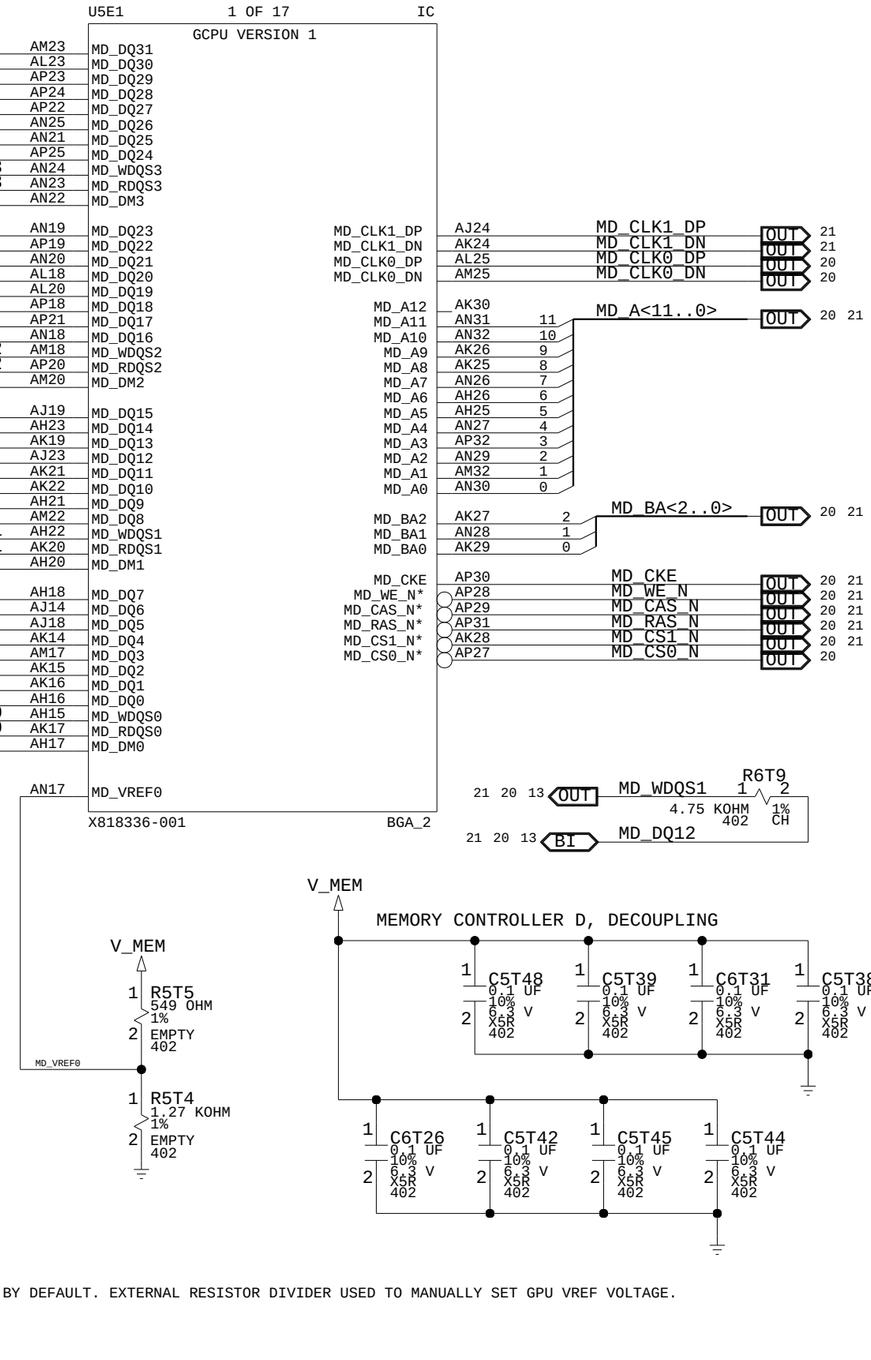
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	12/81	G	1.01

GPU, MEMORY CONTROLLER 1 PARTITION C & D





TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

GPU MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

DRAWING
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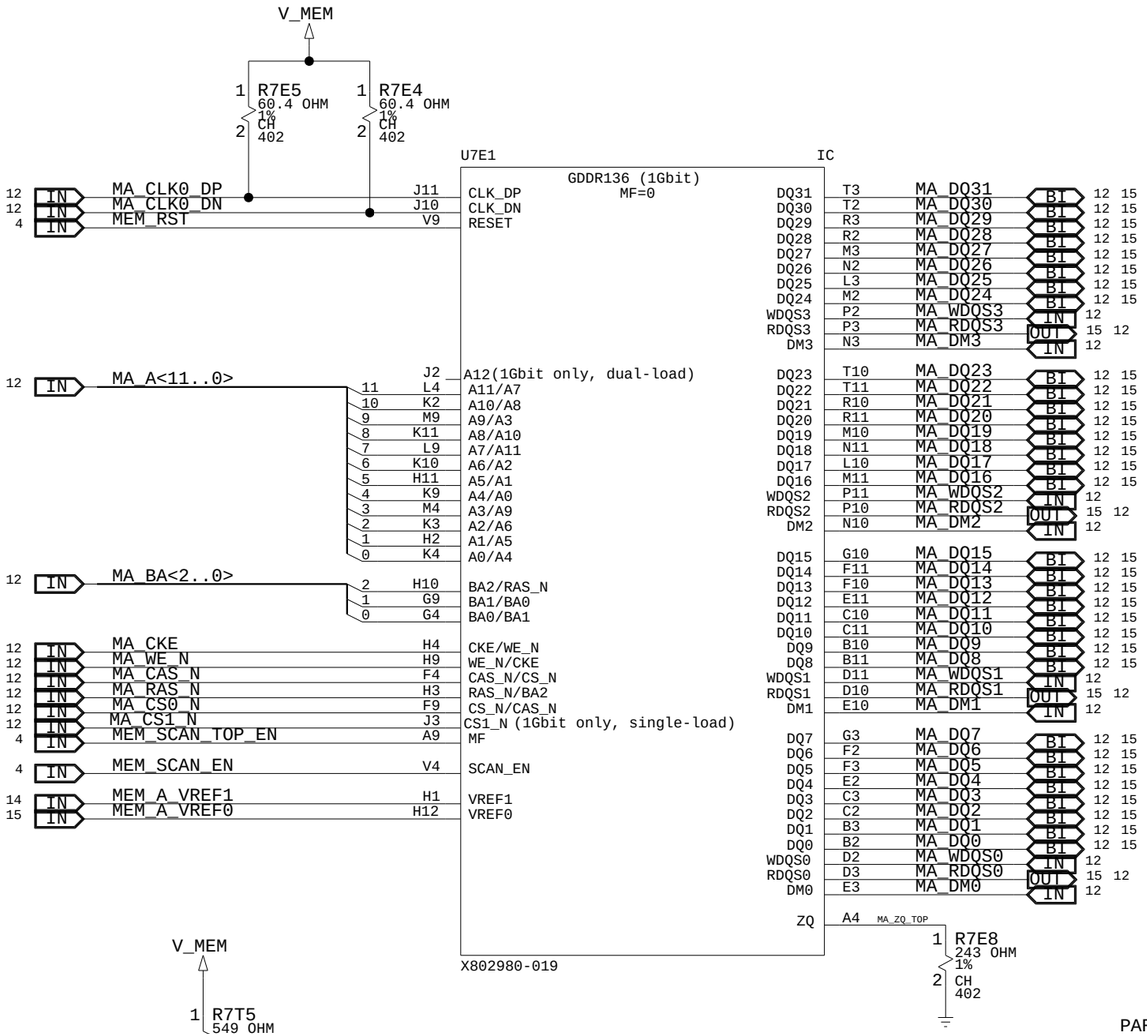
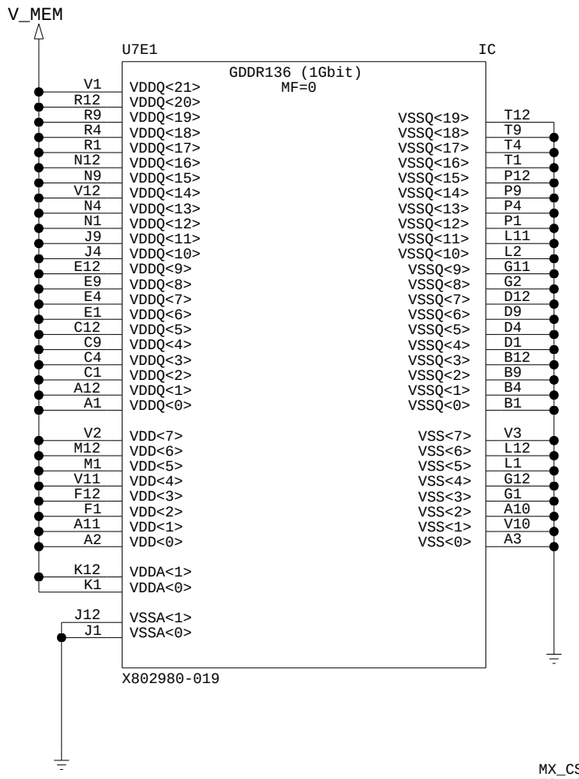
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	13/81	G	1.01

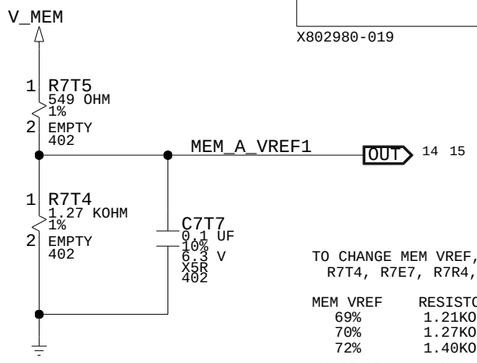
MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0





MX_CS1_N CONNECTED TO J3 TO SUPPORT 1G RAM CONFIGS.

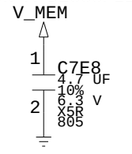


TO CHANGE MEM VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R7T4, R7E7, R7R4, R7D5, R5U4, R5F2, R6U4, R6F2

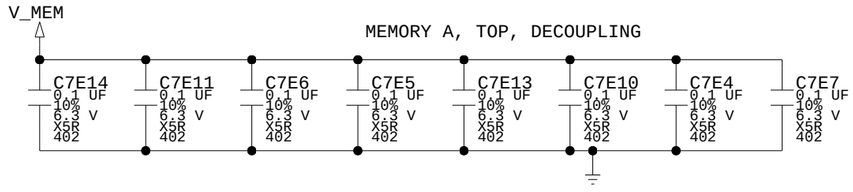
MEM VREF	RESISTOR VALUE
69%	1.21KOHM
70%	1.27KOHM
72%	1.40KOHM

THESE ARE THE MEM VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

PARTITION A DECOUPLING



MEMORY A, TOP, DECOUPLING



[PAGE_TITLE=MEMORY PARTITION A, TOP]

DRAWING
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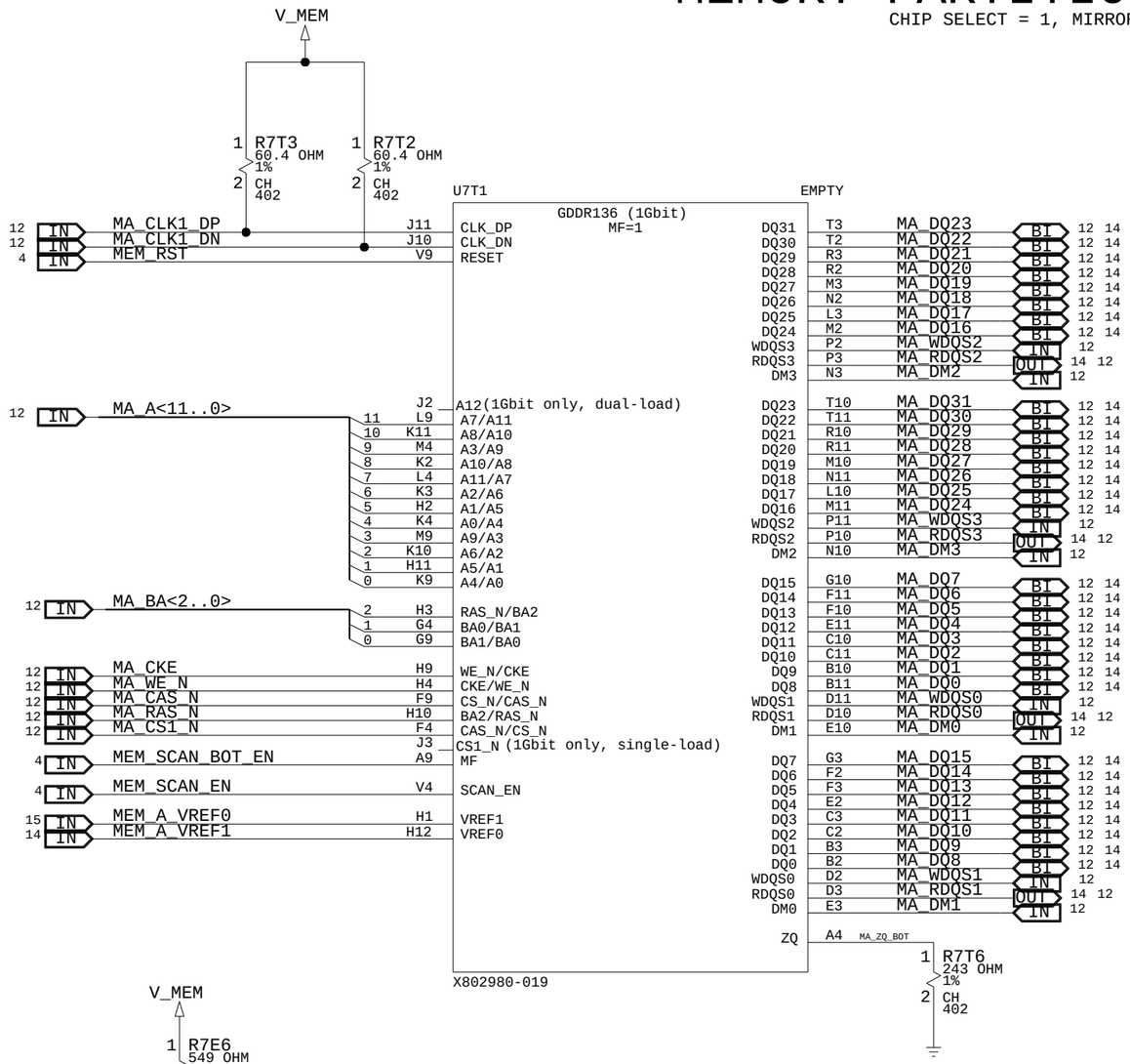
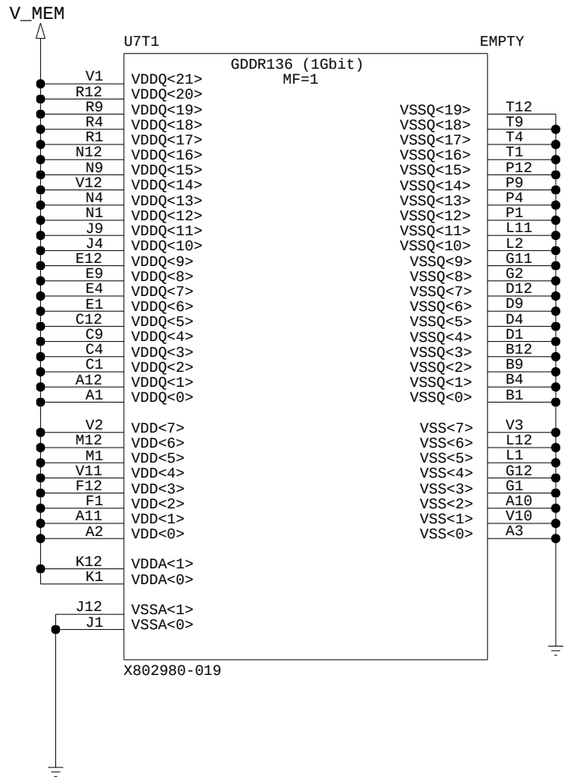
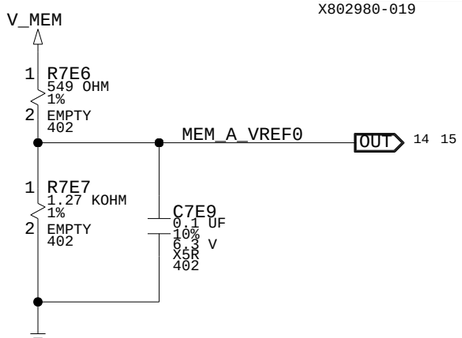
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	14/81	G	1.01

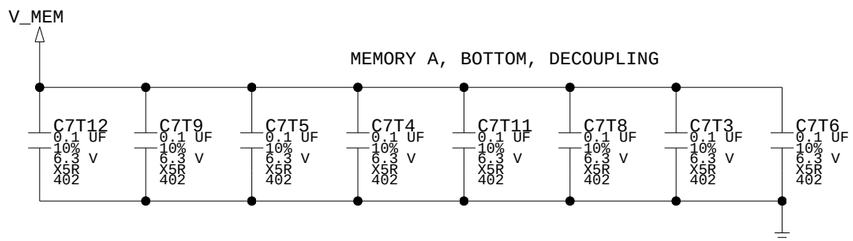
MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1









[PAGE_TITLE=MEMORY PARTITION A, BOTTOM]

DRAWING
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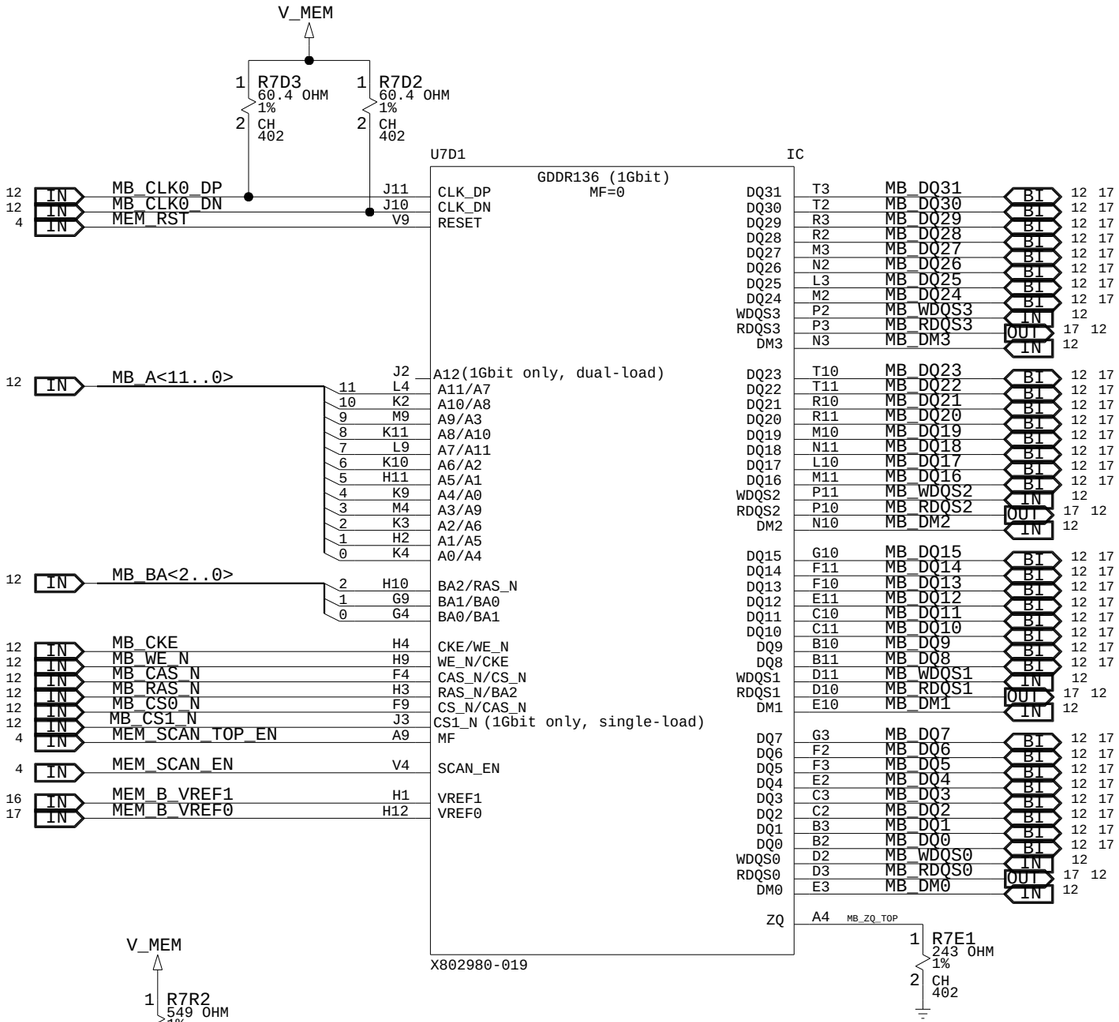
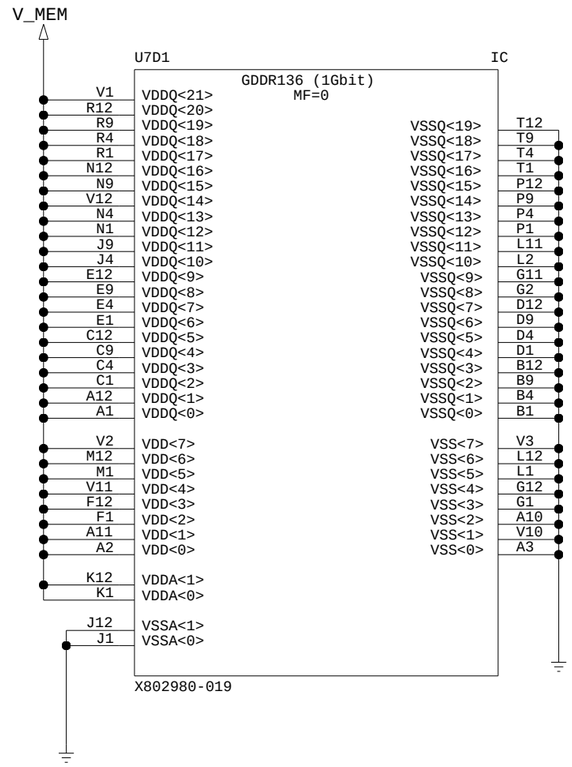
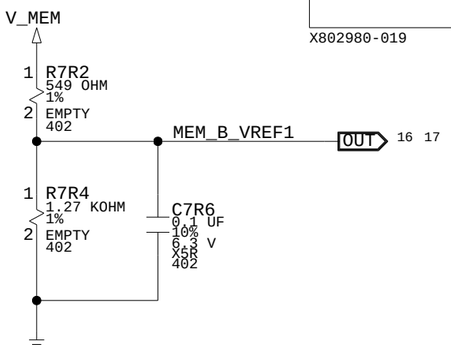
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	15/81	G	1.01

MEMORY PARTITION B, TOP

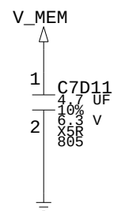
CHIP SELECT = 0, MIRROR FUNCTION = 0

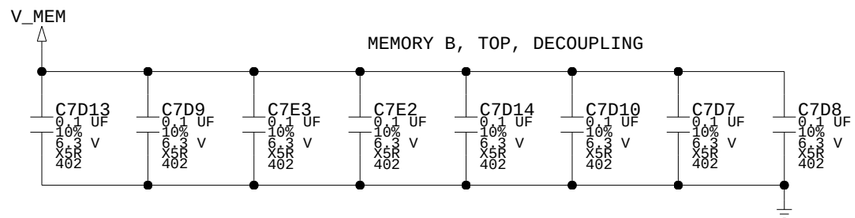






PARTITION B DECOUPLING





[PAGE_TITLE=MEMORY PARITION B, TOP]

DRAWING
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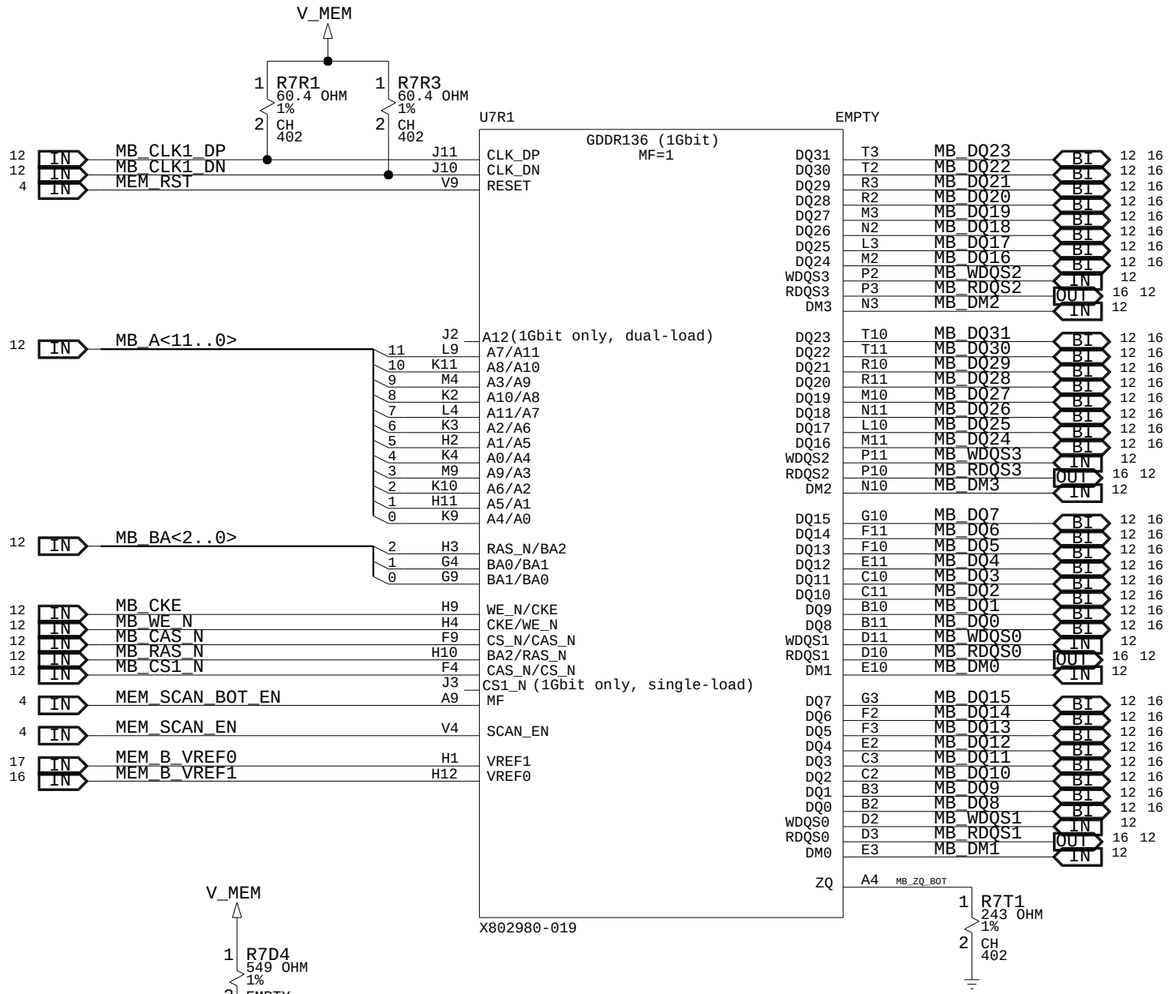
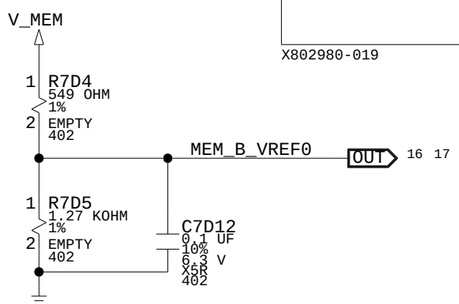
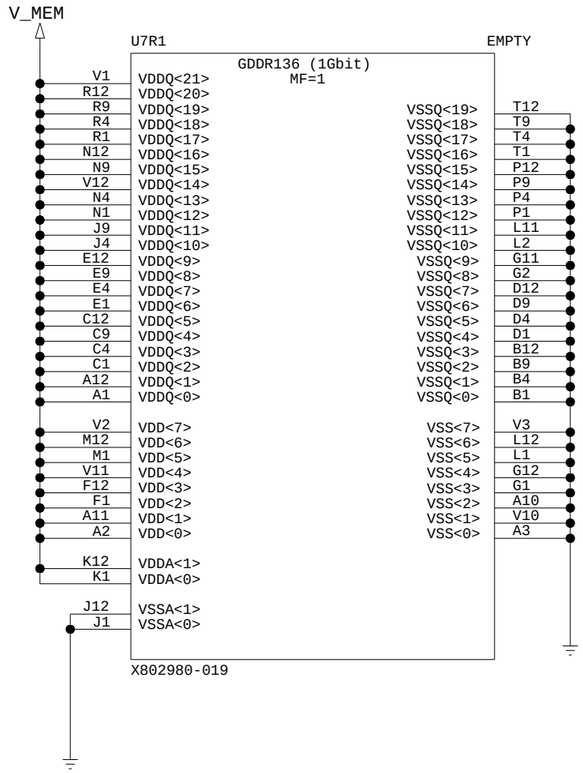
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	16/81	G	1.01

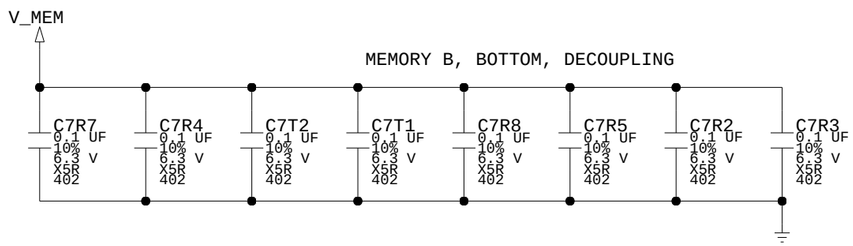
MEMORY PARTITION B, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1









[PAGE_TITLE=MEMORY PARITION B, BOTTOM]

DRAWING
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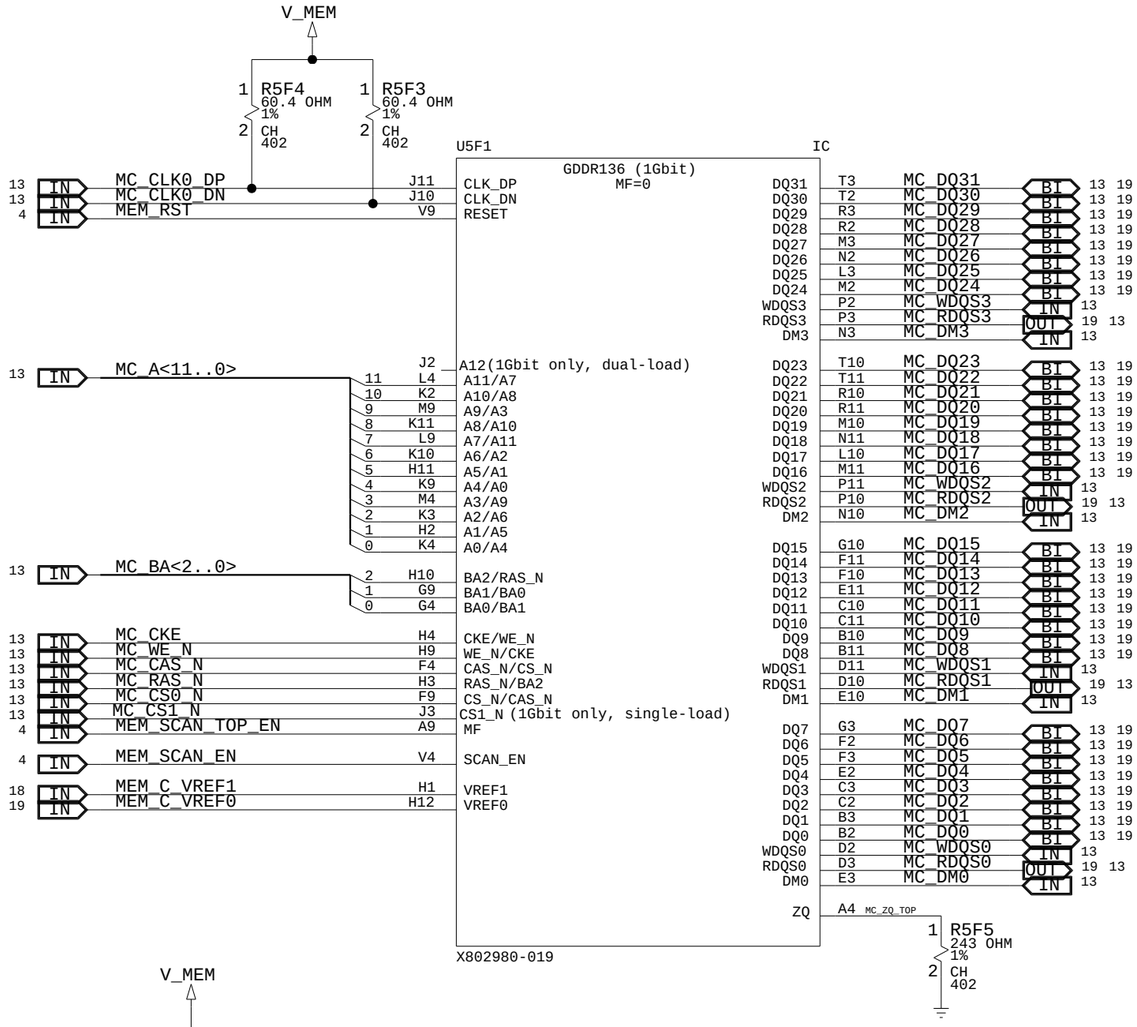
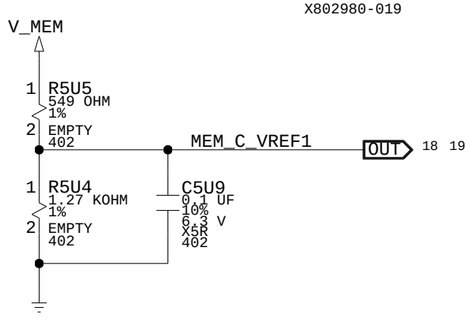
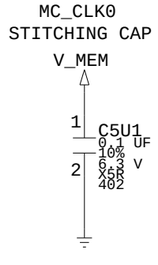
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	17/81	G	1.01

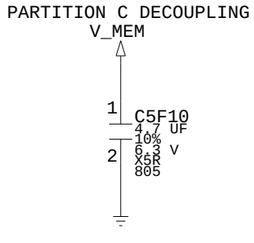
MEMORY PARTITION C, TOP

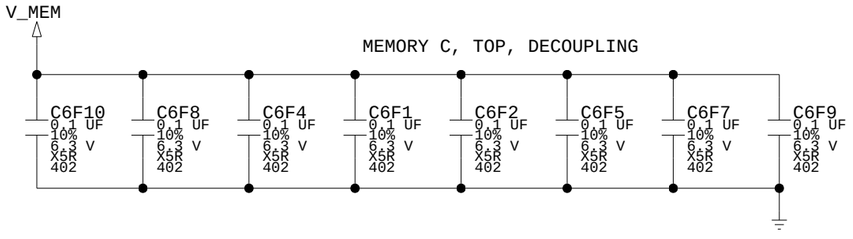
CHIP SELECT = 0, MIRROR FUNCTION = 0











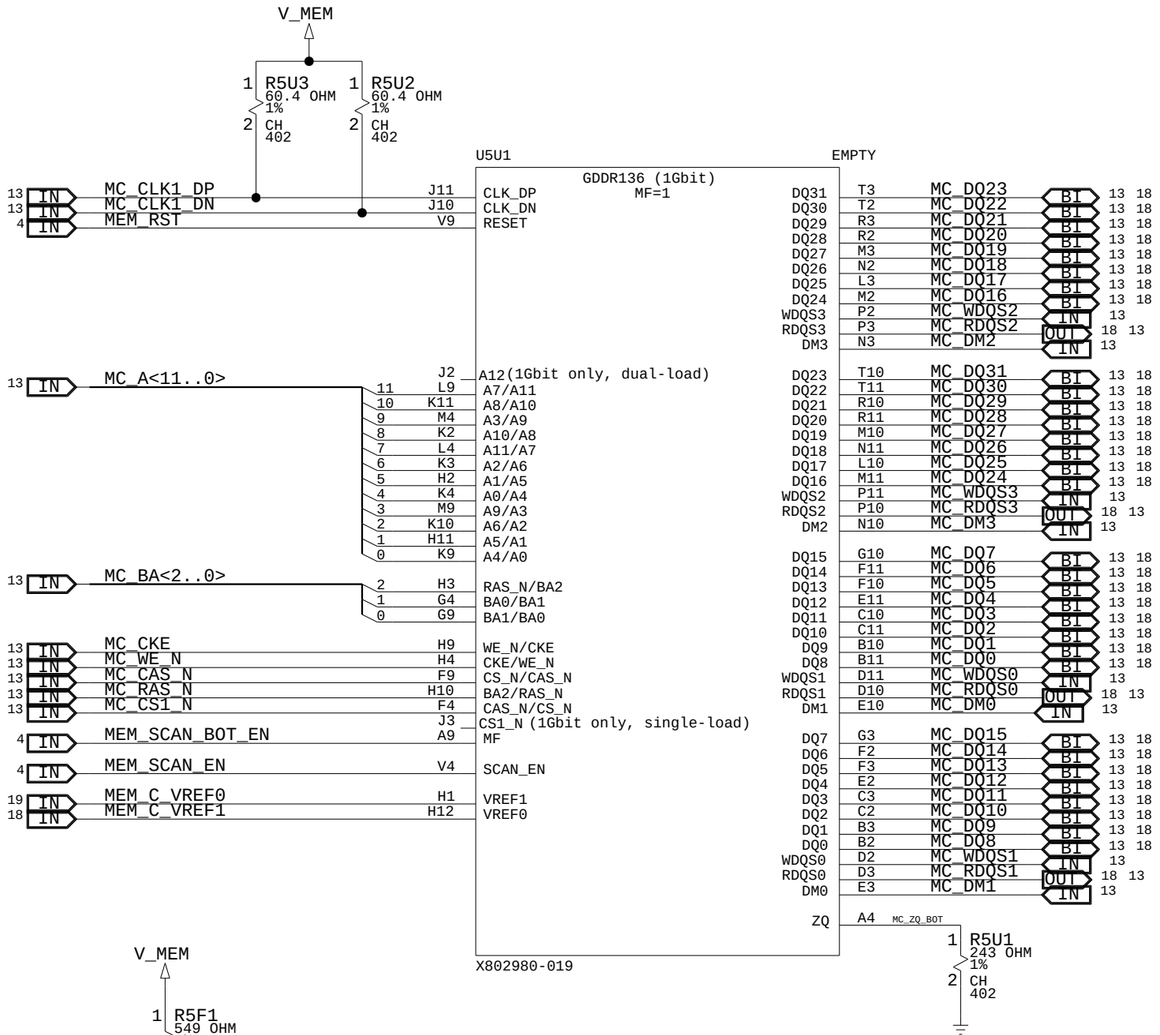
[PAGE_TITLE=MEMORY PARTITION C, TOP]

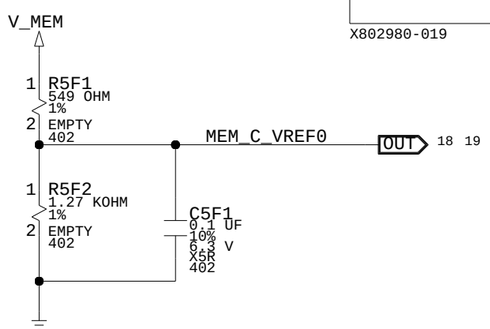
DRAWING
Wed Feb 10 16:23:27 2010

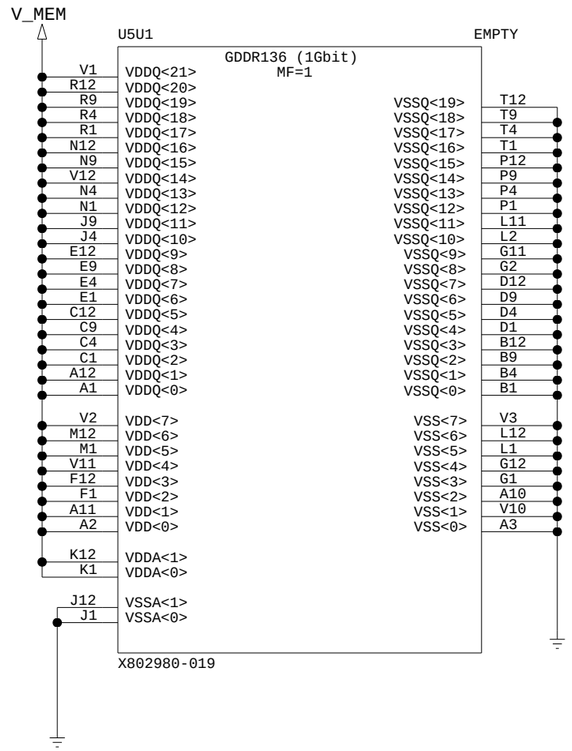
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	18/81	G	1.01

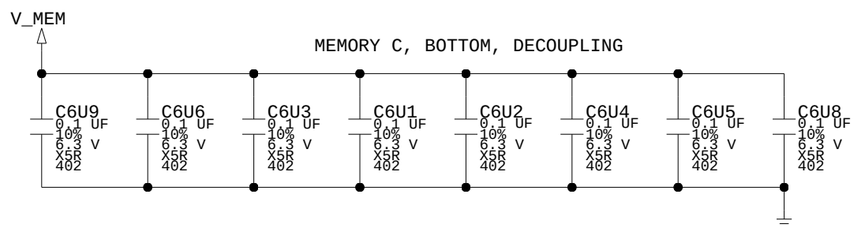
MEMORY PARTITION C, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1









[PAGE_TITLE=MEMORY PARITION C, BOTTOM]

DRAWING
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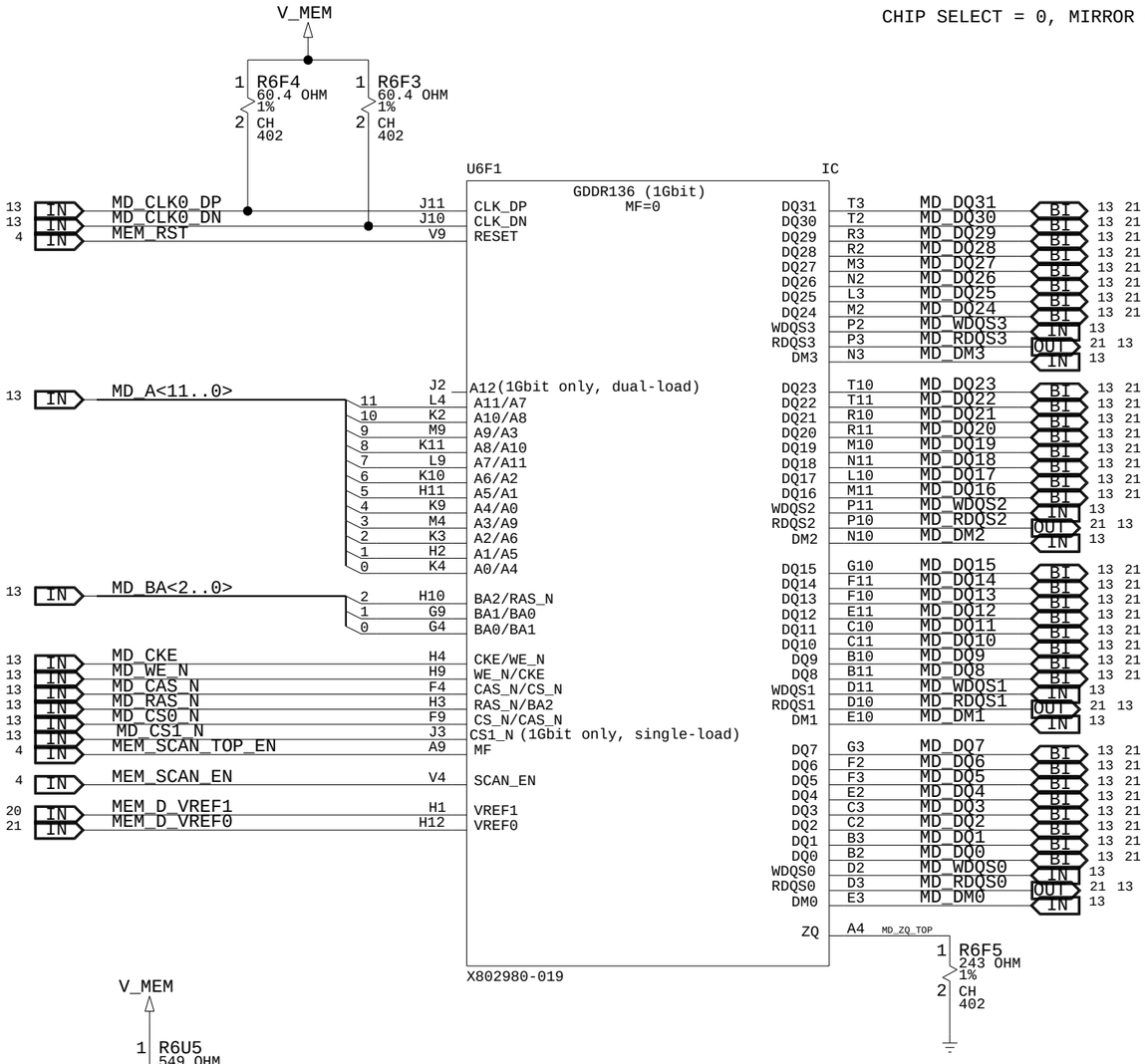
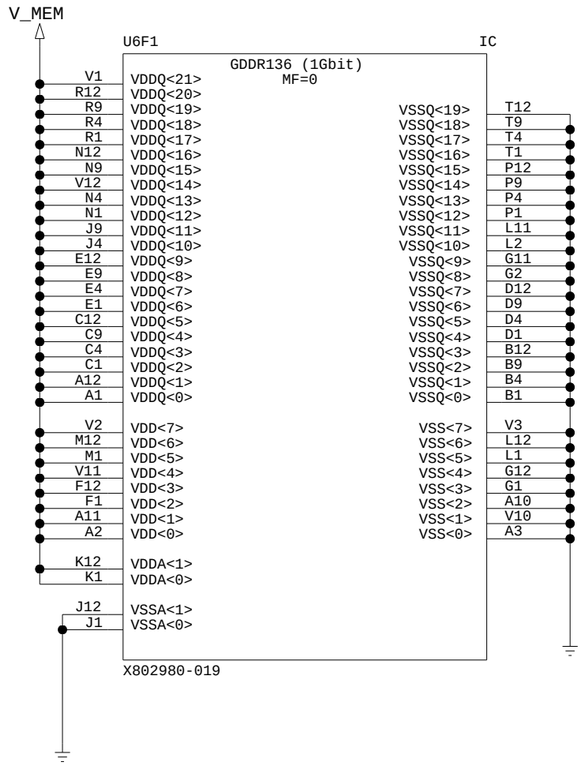
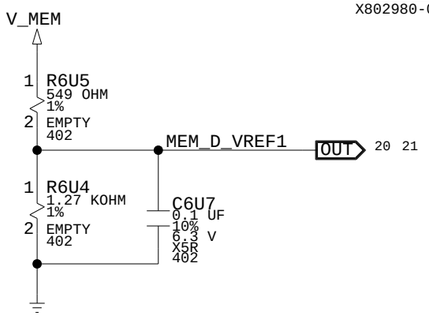
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	19/81	G	1.01

MEMORY PARTITION D, TOP

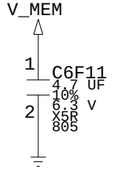
CHIP SELECT = 0, MIRROR FUNCTION = 0

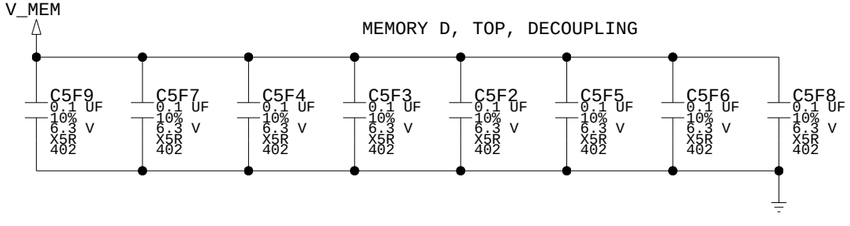






PARTITION D DECOUPLING





[PAGE_TITLE=MEMORY PARTITION D, TOP]

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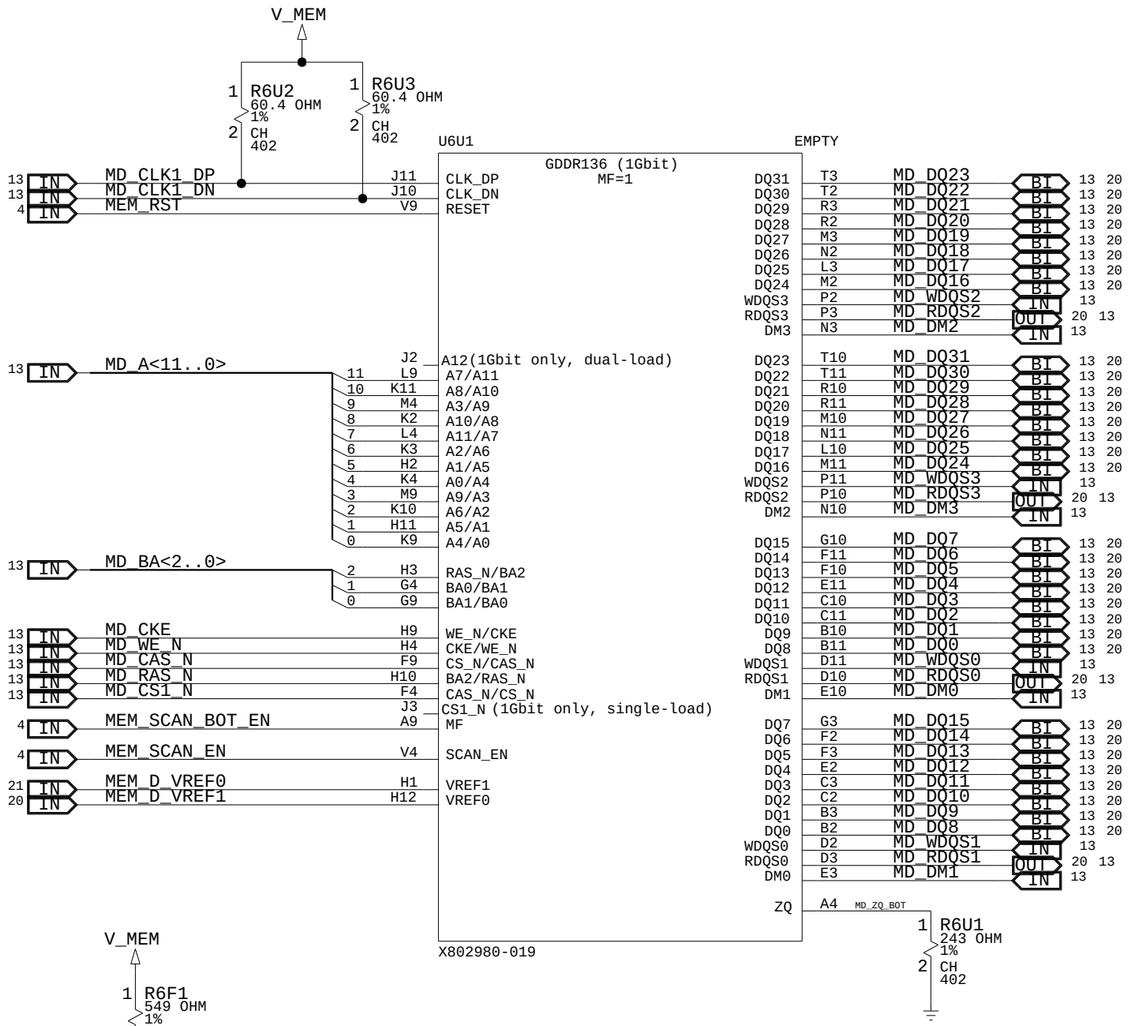
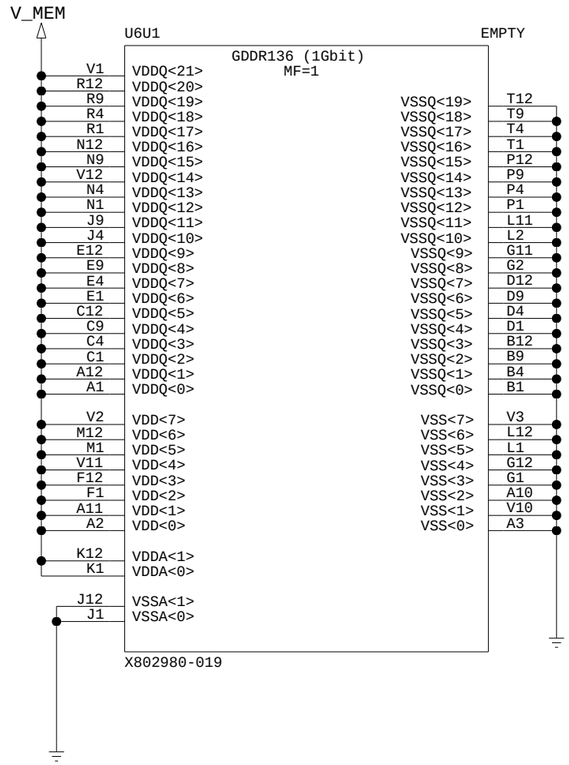
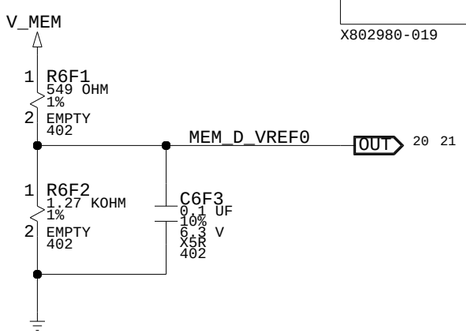
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	20/81	G	1.01

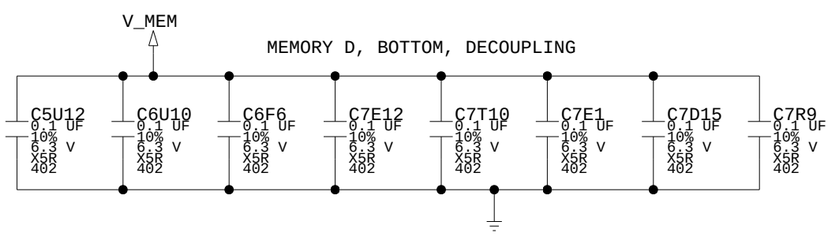
MEMORY PARTITION D, BOTTOM

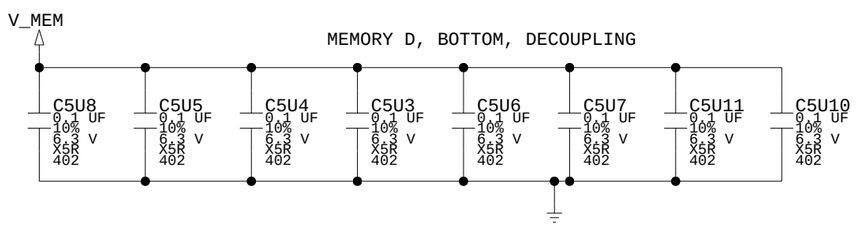
CHIP SELECT = 1, MIRROR FUNCTION = 1











[PAGE_TITLE=MEMORY PARTITION D, BOTTOM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	21/81	G	1.01

HANA, CLOCKS + STRAPPING

U3B2 — 1 OF 4 — HANA — IC

V_12P0

R4B16 11 KOHM 1% 402 CH — R4B7 787 OHM 1% 402 CH — HANA_V_12P0_DET_R — R4B6 787 OHM 1% 402 CH

R3B9 1 MOHM 5% 402 CH

Y3B1 27 MHZ SM XTAL

C3B6 22 PF 5% 50 V NPO 402 — C3B5 22 PF 5% 50 V NPO 402

C4B2 470 PF 5% 50 V EMPTY 402

R3B3 10 KOHM 5% CH 402

FT3R14 FTP — IN — ANA_RST_N

FT3P1 FTP

V_3P3STBY

R3N7 1 KOHM 5% EMPTY 402

FT3R13 FTP — IN — ANA_CLK_OE

R3B10 10 KOHM 5% EMPTY 402

R3B11 1 KOHM 5% 402 CH

R3P1 475 OHM 1% 402 CH

R3N8 475 OHM 1% 402 CH

BI/IN — SMB_DATA / SMB_CLK

IN — HANA_TCLK

OUT — HANA_TDO

IN — HANA_TDI

IN — HANA_TMS

OUT — HANA_TRST

FT3P7 FTP — FT3P6 FTP — FT3P5 FTP — FT3P8 FTP — FT3P9 FTP

HANA_V_12P0_DET	B6	V_12P0_DET	
	M2	CORE_RST_N*<DN>	
HANA_POR_BYPASS	E12	POR_BYPASS<DN>	
HANA_XTAL_IN	P2	XTAL_IN	
HANA_XTAL_OUT	R2	XTAL_OUT	
HANA_XTAL_VSS_CAP	P3	XTAL_VSS_CAP	
HANA_XTAL_BYPASS	M4	XTAL_BYPASS<DN>	
ANA_CLK_OE_R	N3	ANA_CLK_OE<DN>	
HANA_CLK_DRV_RSET2	K13	CLK_DRV_RSET2	
HANA_CLK_DRV_RSET1	R11	CLK_DRV_RSET1	
	N1	SMB_DATA	
	P1	SMB_CLK	
	G12	TCK<DN>	
	F11	TDO	
	J12	TDI<UP>	
	F12	TMS<UP>	
	H12	TRST<DN>	

	E11	V_RST_OK	
	D10	V_12P0_OK	
SMC_RST_N_R	M3	SMC_RST_N*	
CPU_CLK_DP_R	R14	CPU_CLK_DP	
CPU_CLK_DN_R	P14	CPU_CLK_DN	
GPU_CLK_DP_R	R13	NB_CLK_DP	
GPU_CLK_DN_R	P13	NB_CLK_DN	
PCIEX_CLK_DP_R	R10	PCIEX_CLK_DP	
PCIEX_CLK_DN_R	P10	PCIEX_CLK_DN	
SATA_CLK_DP_R	R9	SATA_CLK_DP	
SATA_CLK_DN_R	P9	SATA_CLK_DN	
SATA_CLK_REF_R	R6	SATA_CLK_REF	
HANA_PIX_CLK_2X_DP_R	M15	PIX_CLK_OUT_DP	
HANA_PIX_CLK_2X_DN_R	M14	PIX_CLK_OUT_DN	
ENET_CLK_R	P6	ENET_CLK	
STBY_CLK_R	R8	STBY_CLK	
AUD_CLK_R	R4	AUD_CLK	
HANA_AV_CLK	N2	AV_CLK	

SMC_HDMI_HPD — FT3P2 — OUT 27
ANA_V12P0_PWRGD — OUT 27 42
SMC_RST_N — OUT 27 42 59

R3R16 1 KOHM 5% CH 402 — FT3R1
R3R15 10 KOHM 5% CH 402 — FT3R3

R3C6 33 OHM 5% 402 CH — R3C10 69.8 OHM 1% 402 CH — CPU_CLK_DP / CPU_CLK_DN — OUT 2 2
R3C5 33 OHM 5% 402 CH — R3C9 69.8 OHM 1% 402 CH
R3C4 33 OHM 5% 402 CH — R3C8 49.9 OHM 1% 402 CH — GPU_CLK_DP / GPU_CLK_DN — OUT 4 4
R3C3 33 OHM 5% 402 CH — R3C7 49.9 OHM 1% 402 CH
R3C2 33 OHM 5% 402 CH — R3C1 49.9 OHM 1% 402 CH — PCIEX_CLK_DP / PCIEX_CLK_DN — FT3R11 — OUT 26 26 — FT3R10
R3B21 33 OHM 5% 402 CH — R3B20 49.9 OHM 1% 402 CH
R3B19 33 OHM 5% 402 CH — R3B18 49.9 OHM 1% 402 CH — SATA_CLK_DP / SATA_CLK_DN — FT2R4 — OUT 26 26 — FT2R3
R3B17 33 OHM 5% 402 CH — R3B16 49.9 OHM 1% 402 CH
R3B14 33 OHM 5% 402 CH — SATA_CLK_REF — FT2P2 — OUT 26
R3C12 33 OHM 5% 402 CH — R3C14 69.8 OHM 1% 402 CH — HANA_PIX_CLK_2X_DP / HANA_PIX_CLK_2X_DN — FT3P3 — FT3P4 — OUT 4 4
R3C11 33 OHM 5% 402 CH — R3C13 69.8 OHM 1% 402 CH
R3B13 33 OHM 5% 402 CH — ENET_CLK — FT2R5 — OUT 32
R3B15 33 OHM 5% 402 CH — STBY_CLK — FT3N2 — OUT 27
R3B12 33 OHM 5% 402 CH — AUD_CLK — FT2R1 — OUT 29

C3B9 10 PF 5% 50 V EMPTY 402
C3B8 10 PF 5% 50 V EMPTY 402
C3B10 10 PF 5% 50 V EMPTY 402
C3B7 10 PF 5% 50 V EMPTY 402

AV_CLK — HANA_AV_CLK — FT3N1

R3N5 10 KOHM 5% CH 402

X802478-003

I2C ADDRESS

	0011 100 R/W HEX		0111 000 R/W HEX
WRITE	0011 100 0	0X38	0111 000 0 0X70
READ	0011 100 1	0X39	0111 000 1 0X71

	0011 110 R/W HEX	
WRITE	0011 110 0	0X3C
READ	0011 110 1	0X3D

[PAGE_TITLE=HANA, CLOCKS + STRAPING, JTAG]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	22/81	G	1.01

HANA, VIDEO + FAN + AUDIO

U3B2 2 OF 4 IC
HANA

4 IN GPU_PIX_CLK_1X
4 IN PIX_DATA<14..0>

STBY_CLK STITCH
V_1P8STBY V_3P3STBY V_1P8STBY V_3P3STBY
C3T18 0.1 UF 10% 6.3 V X5R 402
C3T16 0.1 UF 10% 6.3 V X5R 402
C3T8 0.1 UF 10% 6.3 V X5R 402

SATA_CLK_REF STITCH
V_3P3 V_1P8
C2R8 0.1 UF 10% 6.3 V X5R 402

G14 PIX_CLK_IN
14 C14 PIX_DATA14
13 C15 PIX_DATA13
12 D14 PIX_DATA12
11 D15 PIX_DATA11
10 E14 PIX_DATA10
9 E15 PIX_DATA9
8 F14 PIX_DATA8
7 F15 PIX_DATA7
6 G15 PIX_DATA6
5 H14 PIX_DATA5
4 H15 PIX_DATA4
3 J14 PIX_DATA3
2 J15 PIX_DATA2
1 K14 PIX_DATA1
0 K15 PIX_DATA0

4 IN GPU_HSYNC_OUT
4 IN GPU_VSYNC_OUT
L14 HSYNC_IN
L15 VSYNC_IN

HANA_DAC_RSET
R4B10 787 OHM 1% CH 402
C8 DAC_RSET

40 IN HDMI_HPD
A4 HDMI_HPD

29 IN SB_SPDIF_OUT
M1 SPDIF_IN

29 IN I2S_BCLK
29 IN I2S_WS
K1 I2S_SCK
K2 I2S_WS

I2S_SD3 L2 I2S_SD3
I2S_SD2 K4 I2S_SD2
I2S_SD1 K3 I2S_SD1

29 IN I2S_SD
L1 I2S_SD0

R3B4 10 KOHM 5% CH 402
R3N4 10 KOHM 5% CH 402
R3N3 10 KOHM 5% CH 402

HANA_OP2_DP
R4B15 10 KOHM 5% CH 402
C11 FAN_OP2_DP
23 IN HANA_OP2_DN A11 FAN_OP2_DN

27 IN SMC_PWM0
R4C1 205 KOHM 1% 402 CH
FAN_OP1_DP
C12 FAN_OP1_DP

61 4 IN CPU_TEMP_N
ST3C5 SHORT
C4P2 0.22 UF 10% 6.3 V X5R 402
36 IN FAN1_FDBK B12 FAN_OP1_DN

61 4 IN GPU_TEMP_N
ST3C2 SHORT
A15 TEMP_N

61 4 IN EDRAM_TEMP_N
ST3C4 SHORT
BND_GAP_CAP A6 BND_GAP_CAP

38 23 IN BRD_TEMP_N
ST3C3 SHORT
TEMP_RSET A14 TEMP_RSET

23 IN CAL_TEMP_N
ST3C1 SHORT
FT4N2 FTP
DB3P1
C4B3 0.01 UF 10% 16 V X7R 402
R4C2 11 KOHM 1% CH 402
FT4N1 FTP

X802478-003

VID_INT L3 ANA_VID_INT OUT 26

DAC_D_OUT_DP A7 VID_DACD_DP OUT 37
DAC_D_OUT_DN B7 VID_DACD_DN
DAC_C_OUT_DP A8 VID_DACC_DP OUT 37
DAC_C_OUT_DN B8 VID_DACC_DN
DAC_B_OUT_DP A9 VID_DACB_DP OUT 37
DAC_B_OUT_DN B9 VID_DACB_DN
DAC_A_OUT_DP A10 VID_DACA_DP OUT 37
DAC_A_OUT_DN B10 VID_DACA_DN

R4B13 37.4 OHM 1% CH 402
R4B12 37.4 OHM 1% CH 402
R4B9 37.4 OHM 1% CH 402
R4B8 37.4 OHM 1% CH 402

BOARD TEMP SENSOR
23 IN BRD_TEMP_P
Q4G1 EMPTY
23 38 OUT BRD_TEMP_N

V_3P3STBY
R3B2 422 OHM 1% CH 402

HSYNC_OUT B5 VID_HSYNC_OUT_R OUT 37
VSYNC_OUT A5 VID_VSYNC_OUT_R OUT 37
TMDS_EXT_SWING A2 HDMI_EXT_SWING
HDMI_TXC_DP OUT 40
C3B4 0.1 UF 10% 6.3 V X5R 402
R3B8 301 OHM 1% 603 CH
TMDS_TXC_DP B1
TMDS_TXC_DN B2 HDMI_TXC_DN OUT 40

HDMI_TX2_DP OUT 40
C3B1 0.1 UF 10% 6.3 V X5R 402
R3B5 301 OHM 1% 603 CH
TMDS_TX2_DP H1
TMDS_TX2_DN H2 HDMI_TX2_DN OUT 40

HDMI_TX1_DP OUT 40
C3B2 0.1 UF 10% 6.3 V X5R 402
R3B6 301 OHM 1% 603 CH
TMDS_TX1_DP F1
TMDS_TX1_DN F2 HDMI_TX1_DN OUT 40

HDMI_TX0_DP OUT 40
C3B3 0.1 UF 10% 6.3 V X5R 402
R3B7 301 OHM 1% 603 CH
TMDS_TX0_DP D1
TMDS_TX0_DN D2 HDMI_TX0_DN OUT 40

CUSTOM THERMAL CALIBRATION PADS LOCATION MUST REMAIN LOCKED
DB4N4
DB4N6
DB4N5
DB4N7
C4C1 100 PF 5% 50 V EMPTY 402

SPDIF_OUT B4 HANA_SPDIF_OUT OUT 37 39
DDC_SCK B3 HDMI_DDC_CLK B1 27 37 40 55
DDC_SDA A3 HDMI_DDC_DATA B1 27 37 40 55
FAN_OUT2 B11 HANA_OP2_OUT
R4B14 0 OHM 5% 402 CH
HANA_OP2_DN OUT 23
FAN_OUT1 A12 FAN1_OUT OUT 36

TEMP3_P C13 CAL_TEMP_P CAL_TEMP_N OUT 23
TEMP2_P B15 CPU_TEMP_P OUT 4 61
TEMP1_P B13 GPU_TEMP_P OUT 4 61
TEMP0_P A13 EDRAM_TEMP_P OUT 4 61
TEMPCAL_P B14 BRD_TEMP_P OUT 23 38

[PAGE_TITLE=HANA, VIDEO + FAN + AUDIO]

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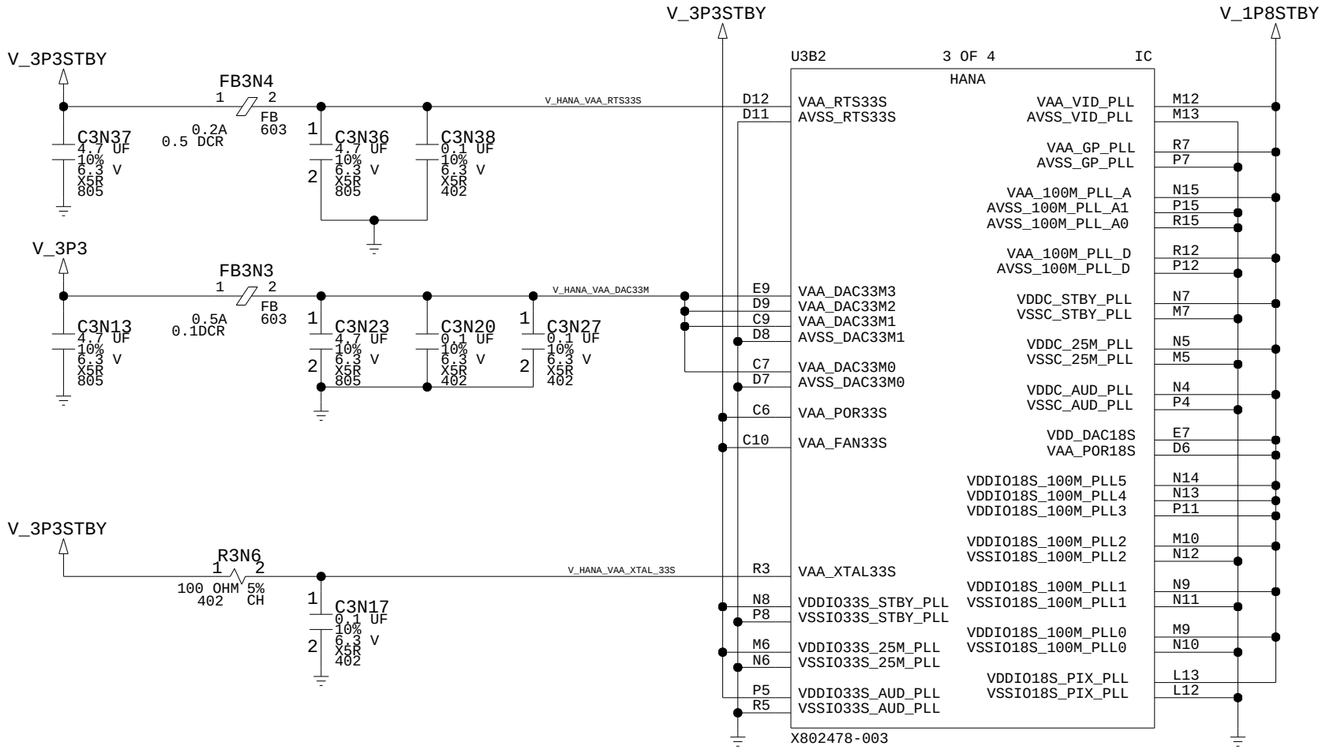
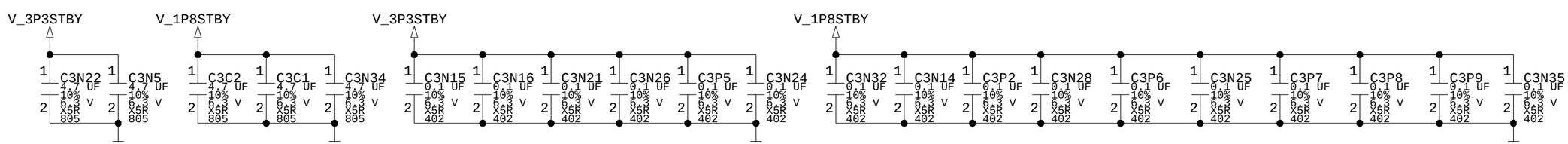
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 23/81	FAB G	REV 1.01

HANA, POWER + DECOUPLING





[PAGE_TITLE=HANA, POWER + DECOUPLING]

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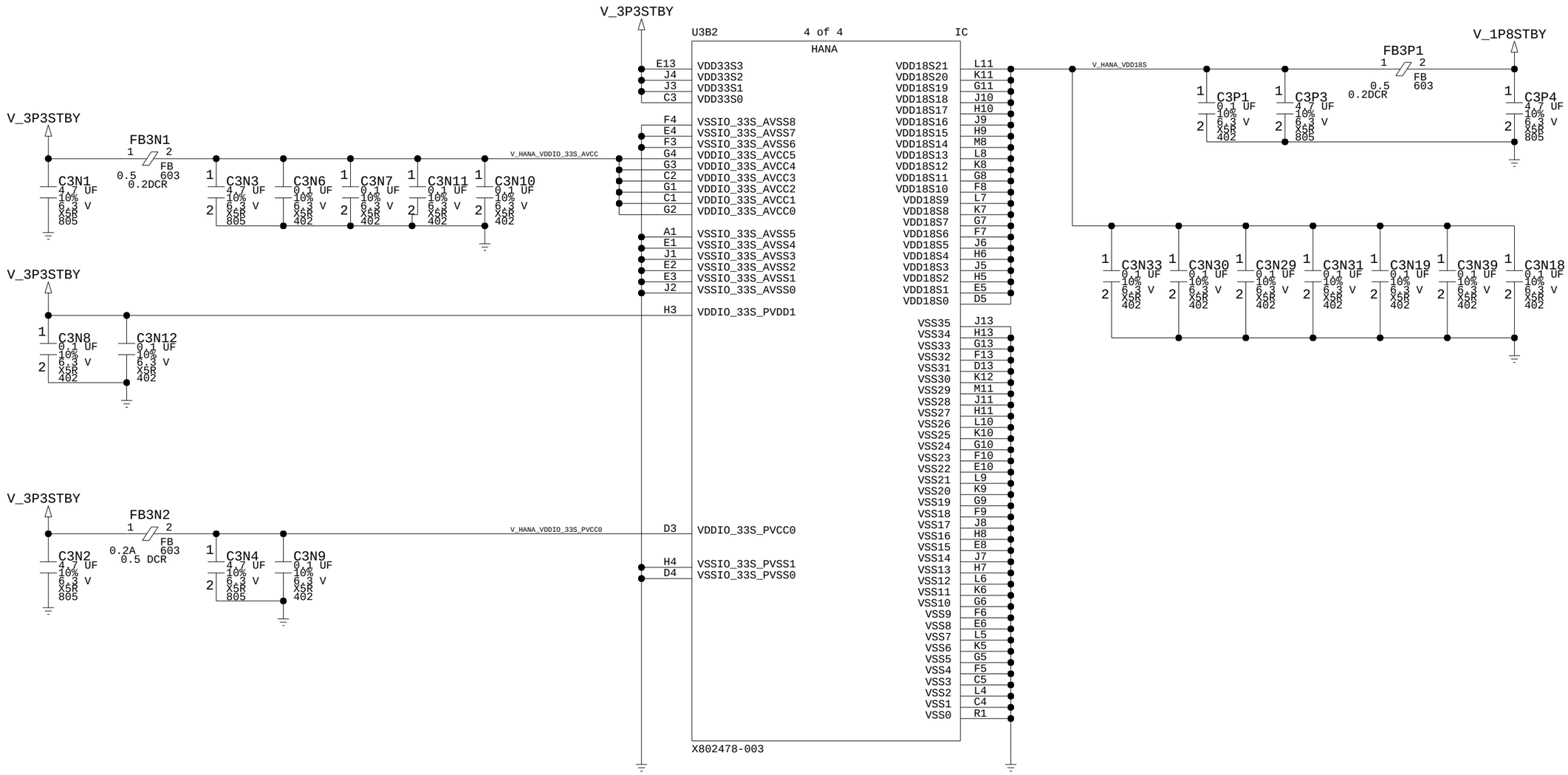
Wed Feb 10 16:23:29 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	24/81	G	1.01

HANA, POWER + DECOUPLING



[PAGE_TITLE=HANA, POWER + DECOUPLING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	25/81	G	1.01

SB, PCIEX + SMM GPIO + JTAG

U3D1 1 of 6 IC

PSB VERSION A0

SATA_CLK_DP	K1	SATA_CLK_DP	
SATA_CLK_DN	J1	SATA_CLK_DN	
SATA_CLK_REF	H3	SATA_CLK_REF	
SATA_CLK_SEL	H4	SATA_CLK_SEL<UP>	
ECB_CLK_BYP	A6	ECB_CLK_BYP<DN>	
ECB_CLK_SEL	B6	ECB_CLK_SEL<DN>	
HBEDB_CLK_BYP	U20	HBEDB_CLK_BYP<DN>	
HBEDB_CLK_SEL	V20	HBEDB_CLK_SEL<DN>	
XUSB_CLK_BYP	B15	XUSB_CLK_BYP<DN>	
XUSB_CLK_SEL	C15	XUSB_CLK_SEL<DN>	
PCIEX_CLK_DN	L22	PEX_CLK_DP	
PCIEX_CLK_DP	L21	PEX_CLK_DN	
PEX_GPU_SB_L1_DP	P22	PEX_RX1_DP	
PEX_GPU_SB_L1_DN	N22	PEX_RX1_DN	
PEX_GPU_SB_L0_DP	T21	PEX_RX0_DP	
PEX_GPU_SB_L0_DN	R21	PEX_RX0_DN	
PEX_RBIAS1	K20	PEX_RBIAS1	
PEX_RBIAS0	K19	PEX_RBIAS0	
KER_DBG_RXD	D15	UART0_RXD<UP>	
PEX_TX1_DP	N20		
PEX_TX1_DN	M20		
PEX_TX0_DP	R19		
PEX_TX0_DN	P19		
UART0_TXD	D14		
GPIO23	D10		
GPIO22	D11		
GPIO21	D12		
GPIO20	D13		
GPIO19	C8		
GPIO18	D9		
GPIO17	C9		
GPIO16	B9		
GPIO15	A9		
GPIO14	C10		
GPIO13	B10		
GPIO12	A10		
GPIO11	C11		
GPIO10	B11		
GPIO9	A11		
GPIO8	C12		
GPIO7	B12		
GPIO6	A12		
GPIO5	C13	SCART_RGB	
GPIO4	B13	AUD_RST_N	
GPIO3	A13		
GPIO2	C14	ANA_VID_INT	
GPIO1	B14	WSS_CNTL0	
GPIO0	A14	WSS_CNTL1	
	E3	PCIEX_INT	
	F1	SB_GPIO_RESERVED6	
	F2		
	F3	ENET_RST_N	
	G1		
	G2		
	G3		
	G4		
TCK<DN>	W20		
TDO	V22		
TDI<UP>	V21		
TMS<UP>	W22		
TRST<DN>	W21		

X817692-001

GPIO<1> = 0 ENABLE DEBUG OUTPUT
1 DISABLE DEBUG OUTPUT

GPIO<0,2,3> = 111 XENON
110 ZEPHYR A
101 ZEPHYR B
100 ZEPHYR C
011 FALCON
010 JASPER
001 TRINITY

GPIO<5> = 0 LESS THEN 1GB SYSTEM FLASH
1, 1GB SYSTEM FLASH

SB_GPIO<0..15> BI 26

SATA_CLK V_3P3 STITCH

[PAGE_TITLE=SB, PCIEX + SMM GPIO + JTAG]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	26/81	G	1.01

SB, SMC

U3D1 2 of 6 IC

SB VERSION 106

22 IN STBY_CLK — Y12 STBY_CLK
22 IN SMC_RST_N — C17 SMC_RST_N*
C3R2 1 UF 10% 16 V X5R 603
V_3P3STBY
FT3R15 FTP 1
27 IN SB_RST_N — G20 SB_RST_N*
27 IN SB_MAIN_PWRGD — G19 MAIN_PWR_OK
D16 SMC_UART1_RXD<UP>
59 IN SMC_DBG_EN — C16 SMC_DBG<DN>

41 OUT TRAY_OPEN — R3R6 33 OHM 5% 402 CH — TRAY_OPEN_R — A18 SMC_P4_GPIO7
41 IN TRAY_STATUS — B18 SMC_P4_GPIO6
60 59 37 IN EXT_PWR_ON_N — R2C5 10 KOHM 5% 402 CH — EXT_PWR_ON_R — C18 SMC_P4_GPIO5
50 BI VREG_VMEM_PWRGD_CPU_TRST_N_R — D18 SMC_P4_GPIO4
55 40 37 23 BI HDMI_DDC_DATA — A19 SMC_P4_GPIO3
60 BI SMC_CPU_CHKSTOP_DETECT — B19 SMC_P4_GPIO2
FT3R4 FTP 1

V_3P3STBY
R3R18 1.27 KOHM 1% CH 402
R3R17 1.27 KOHM 1% CH 402
FT3R6 FTP 1
59 55 41 22 BI SMB_DATA — C19 SMC_P4_GPIO1
55 41 22 59 BI SMB_CLK — A20 SMC_P4_GPIO0
FT3R5 FTP 1

37 IN AV_MODE2 — R3R3 10 KOHM 5% 402 CH — AV_MODE2_R — B20 SMC_P3_GPIO7
37 IN AV_MODE1 — R3M1 10 KOHM 5% 402 CH — AV_MODE1_R — B21 SMC_P3_GPIO6
37 IN AV_MODE0 — R3R4 10 KOHM 5% 402 CH — AV_MODE0_R — C20 SMC_P3_GPIO5
55 40 37 23 BI HDMI_DDC_CLK — C22 SMC_P3_GPIO4
47 IN VREG_V5P0_PWRGD — C21 SMC_P3_GPIO3
FT4R10 FTP 1
22 IN SMC_HDMI_HPD — D22 SMC_P3_GPIO2
48 IN VREG_V3P3_PWRGD — D21 SMC_P3_GPIO1
FT3R9 FTP 1
D20 SMC_P3_GPIO0

V_3P3STBY
R3D1 2 KOHM 1% CH 402
DB2G3 1
OUT DBG_LED0
R3D2 2 KOHM 1% EMPTY 402
FT2V1 FTP 1

N: DBG_LED0 PULLDOWN = SMC PRODUCTION MODE
DBG_LED0 PULLUP = SMC DEVELOPMENT MODE

A16 SMC_IR_IN
TP DB3R7 1 EN_TEST1_N — G22 ENTEST1_N*<UP>
TP DB3R6 1 EN_TEST0_N — G21 ENTEST0_N*<UP>
35 IN IR_DATA

X817692-001

SMC_UART1_TXD — B16 SMC_DBG_TXD — R2C1 47 OHM 5% 402 CH — SMC_DBG_TXD — OUT 59

SMC_P2_GPIO7 E22 PWRSW_N — IN 38
SMC_P2_GPIO6 E21 VREG_V3P3_EN — OUT 48
SMC_P2_GPIO5 E20 ANA_V12P0_PWRGD — IN 22
SMC_P2_GPIO4 E19 VREG_VEDRAM_PWRGD — IN 49
SMC_P2_GPIO3 F22 ANA_RST_N — OUT 22
SMC_P2_GPIO2 F21 VREG_VEDRAM_EN — OUT 49
SMC_P2_GPIO1 F20 PSU_V12P0_EN — OUT 38 42
SMC_P2_GPIO0 F19 ANA_CLK_OE — OUT 22

SMC_P1_GPIO7 Y21 VREG_CPU_EN — OUT 44
SMC_P1_GPIO6 Y22 VREG_CPUCORE_VCS_PWRGD — IN 44 51
SMC_P1_GPIO5 AA20 VREG_V5P0_EN — OUT 47
SMC_P1_GPIO4 AA21 VREG_V5P0_SEL — OUT 46
SMC_P1_GPIO3 AB20 VREG_VMEM_EN — OUT 50
SMC_P1_GPIO2 Y20 BINDSW_N — IN 38
SMC_P1_GPIO1 AA19 TILTSW_N — IN 35
SMC_P1_GPIO0 AB19 EJECTSW_N — IN 38

SMC_P0_GPIO7 J20 GPU_RST_DONE — R3R19 1 KOHM 5% 402 CH — R3R20 10 KOHM 5% 402 CH — IN 4
SMC_P0_GPIO6 H21 CPU_RST_N — OUT 2
SMC_P0_GPIO5 H19 SB_MAIN_PWRGD — R3R21 10 KOHM 5% 402 CH — R3R23 1 KOHM 5% 402 CH — FT3R12 — OUT 27
SMC_P0_GPIO4 H20 SB_RST_N — OUT 27

V_1P8STBY
R3T2 100 KOHM 5% 402 CH
R3T3 100 KOHM 5% 402 CH
SMC_P0_GPIO3 J19 BORONFPM_DATA — BI 38
SMC_P0_GPIO2 J22 BORONFPM_CLK — BI 38
SMC_P0_GPIO1 J21 GPU_RST_N — OUT 4
SMC_P0_GPIO0 H22 CPU_PWRGD — OUT 2
SMC_PWM1 A17 SMC_PWM1 — OUT 36
SMC_PWM0 B17 SMC_PWM0 — OUT 23

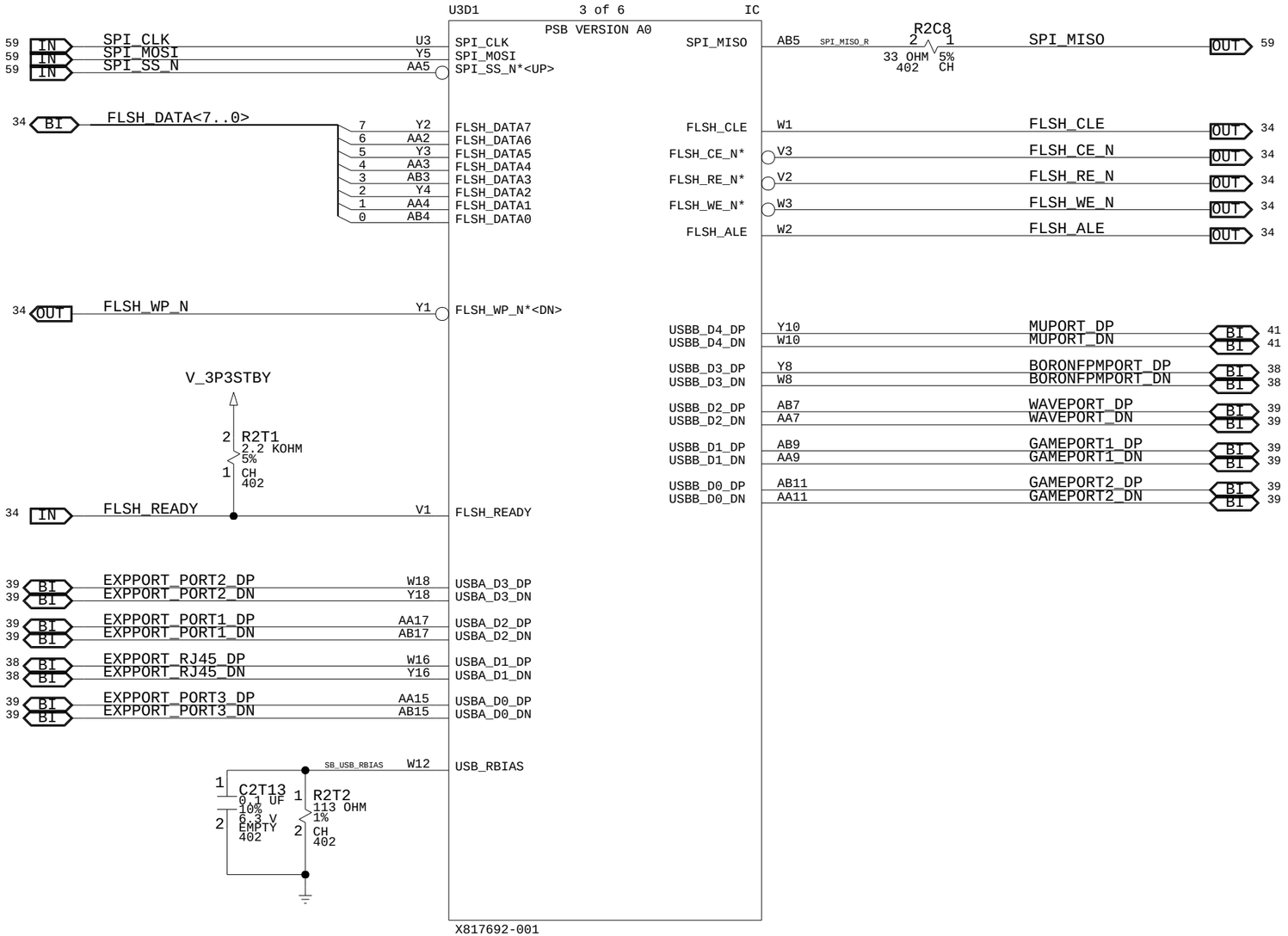
[PAGE_TITLE=SB, SMC]

DRAWING
Wed Feb 10 16:23:29 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	27/81	G	1.01

SB, FLASH + USB + SPI

N: ALL PORTS ARE DIFFERENTIAL USB PAIRS ON THIS PAGE



[[PAGE_TITLE=SB, FLASH + USB + SPI]]

DRAWING
Wed Feb 10 16:23:29 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	28/81	G	1.01

SB, ETHERNET + AUDIO + SATA

U3D1 4 of 6 IC

PSB VERSION A0

32	IN	MII_TX_CLK	R2D8 33 OHM 5% 402 CH	MII_TX_CLK_R	B3	MII_TX_CLK	
32	IN	MII_RX_CLK	R2D7 33 OHM 5% 402 CH	MII_RX_CLK_R	C3	MII_RX_CLK	
32	IN	MII_RXD3			D1	MII_RXD3	
32	IN	MII_RXD2			D2	MII_RXD2	
32	IN	MII_RXD1			D3	MII_RXD1	
32	IN	MII_RXD0			C1	MII_RXD0	
32	IN	MII_RXDV			C2	MII_RXDV	
32	IN	MII_RXER			B2	MII_RXER	
32	IN	MII_COL			B5	MII_COL	
32	IN	MII_CRS			A5	MII_CRS	
32	BI	MII_MDIO			E1	MII_MDIO	
22	IN	AUD_CLK			A8	AUD_CLK	
41	IN	HDD_RX_DP			N4	SATA1_RX_DP	
41	IN	HDD_RX_DN			P4	SATA1_RX_DN	
41	IN	ODD_RX_DP			L3	SATA0_RX_DP	
41	IN	ODD_RX_DN			M3	SATA0_RX_DN	

SATA_RBIAS U2 SATA_RBIAS

C2E1 0.1 UF 10% 6.3 V X5R 402

R2E1 374 OHM 1% CH 402

X817692-001

MII_MDC_CLK_OUT	E2	MII_MDC_CLK_OUT_R	R2D13 33 OHM 5% 402 CH	MII_MDC_CLK_OUT	OUT	32	
MII_TXD3	C5			MII_TXD3	OUT	32	
MII_TXD2	A4			MII_TXD2	OUT	32	
MII_TXD1	B4			MII_TXD1	OUT	32	
MII_TXD0	C4			MII_TXD0	OUT	32	
MII_TXEN	A3			MII_TXEN	OUT	32	
I2S_MCLK_OUT	C7	I2S_MCLK_R	R2D9 47 OHM 5% 402 CH	I2S_MCLK	OUT	33	
I2S_BCLK_OUT	B8	I2S_BCLK_R	R2D12 47 OHM 5% 402 CH	I2S_BCLK	OUT	23 33	
I2S_SD	A7	I2S_SD_R	R2D11 47 OHM 5% 402 CH	I2S_SD	OUT	23 33	
I2S_WS	B7	I2S_WS_R	R2D10 47 OHM 5% 402 CH	I2S_WS	OUT	23 33	
SPDIF	C6	SPDIF_R	R2D5 47 OHM 5% 402 CH	SB_SPDIF_OUT	OUT	23	
SATA1_TX_DP	R2			HDD_TX_DP	OUT	41	
SATA1_TX_DN	P2			HDD_TX_DN	OUT	41	
SATA0_TX_DP	N1			ODD_TX_DP	OUT	41	
SATA0_TX_DN	M1			ODD_TX_DN	OUT	41	

R2R14 10 KOHM 5% CH 402

R2R17 10 KOHM 5% CH 402

R2R16 10 KOHM 5% CH 402

R2R18 10 KOHM 5% CH 402

[PAGE_TITLE=SB, ETHERNET + AUDIO + SATA]

DRAWING
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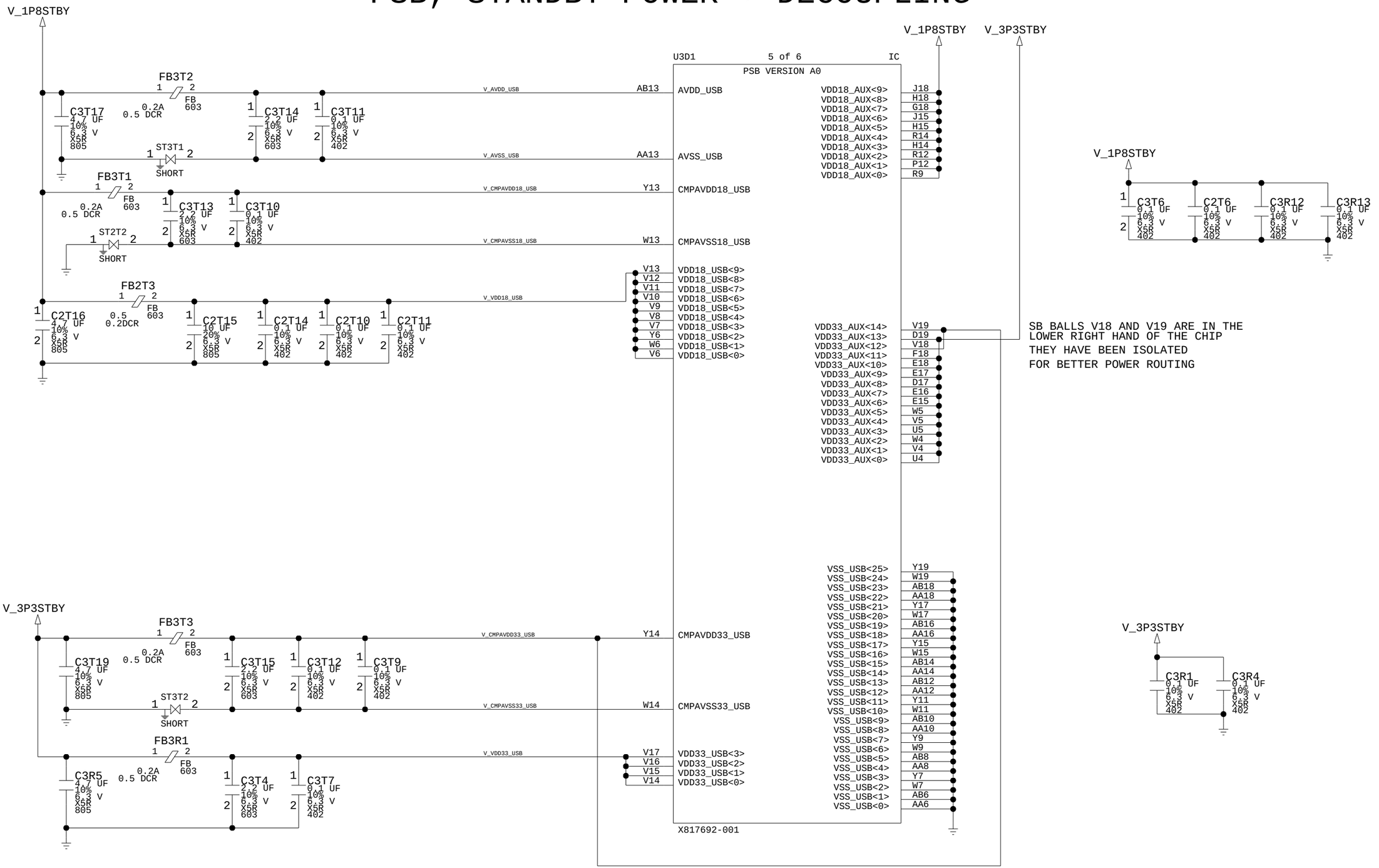
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 29/81	FAB G	REV 1.01

PSB, STANDBY POWER + DECOUPLING



[PAGE_TITLE=PSB, STANDBY POWER + DECOUPLING]

DRAWING
Wed Feb 10 16:23:30 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	30/81	G	1.01

PSB, MAIN POWER + DECOUPLING

U3D1 6 of 6 IC

PSB VERSION A0

V_SBPCIE

FB3R2 FB 603 0.2A 0.5 DCR

C3T2 4.7 UF 10% 6.3 V X5R 805

C3R16 2.2 UF 10% 6.3 V X5R 603

C3R15 0.01 UF 10% 16 V X7R 402

ST3R1 SHORT

R3T1 0 OHM % 805 CH

C3T5 4.7 UF 10% 6.3 V X5R 805

C3T3 0.1 UF 10% 16 V X5R 402

C3T1 0.01 UF 10% 16 V X7R 402

V_AVDD_PEX L19 AVDD_PEX

V_AVSS_PEX L20 AVSS_PEX

V_VDD_PEX_FB

T18 VDD_PEX<4>
R18 VDD_PEX<3>
P18 VDD_PEX<2>
N18 VDD_PEX<1>
M18 VDD_PEX<0>

U22 VSS_PEX<15>
T22 VSS_PEX<14>
R22 VSS_PEX<13>
M22 VSS_PEX<12>
K22 VSS_PEX<11>
U21 VSS_PEX<10>
P21 VSS_PEX<9>
N21 VSS_PEX<8>
M21 VSS_PEX<7>
K21 VSS_PEX<6>
T20 VSS_PEX<5>
R20 VSS_PEX<4>
P20 VSS_PEX<3>
T19 VSS_PEX<2>
N19 VSS_PEX<1>
M19 VSS_PEX<0>

V_1P8

VDD18<17> U19
VDD18<16> U18
VDD18<15> R15
VDD18<14> P15
VDD18<13> M15
VDD18<12> M14
VDD18<11> J12
VDD18<10> H12
VDD18<9> R11
VDD18<8> J11
VDD18<7> H11
VDD18<6> M9
VDD18<5> H9
VDD18<4> R8
VDD18<3> P8
VDD18<2> M8
VDD18<1> J8
VDD18<0> H8

V_3P3

VDD33<13> E14
VDD33<12> E13
VDD33<11> E12
VDD33<10> E11
VDD33<9> E10
VDD33<8> E9
VDD33<7> D8
VDD33<6> D7
VDD33<5> D6
VDD33<4> G5
VDD33<3> D5
VDD33<2> F4
VDD33<1> E4
VDD33<0> D4

V_1P8

C3R11 0.1 UF 10% 6.3 V X5R 402
C3R10 0.1 UF 10% 6.3 V X5R 402
C3R7 0.1 UF 10% 6.3 V X5R 402
C2R20 0.1 UF 10% 6.3 V X5R 402
C3R18 0.1 UF 10% 6.3 V X5R 402
C3R8 0.1 UF 10% 6.3 V X5R 402
C2R14 0.1 UF 10% 6.3 V X5R 402
C2T4 0.1 UF 10% 6.3 V X5R 402
C3R17 0.1 UF 10% 6.3 V X5R 402

V_1P8

C2T9 1 UF 10% 16 V X5R 603
C2R17 1 UF 10% 16 V X5R 603
C2T12 4.7 UF 10% 6.3 V X5R 805

V_3P3

C2R12 0.1 UF 10% 6.3 V X5R 402
C2R11 0.1 UF 10% 6.3 V X5R 402
C2R13 0.1 UF 10% 6.3 V X5R 402
C3R6 0.1 UF 10% 6.3 V X5R 402
C2R9 0.1 UF 10% 6.3 V X5R 402

V_3P3

C3R3 1 UF 10% 16 V X5R 603
C2R7 4.7 UF 10% 6.3 V X5R 805

V_1P8

C2R10 4.7 UF 10% 6.3 V X5R 805
C2T7 4.7 UF 10% 6.3 V X5R 805

FB2R3 FB 603 0.2A 0.5 DCR

C2R19 2.2 UF 10% 6.3 V X5R 603
C2R18 0.1 UF 10% 6.3 V X5R 402

ST2R2 SHORT

V_AVDD1_SATA J3 AVDD1_SATA
V_AVSS1_SATA J2 AVSS1_SATA

V_AVDD0_SATA H1 AVDD0_SATA
V_AVSS0_SATA H2 AVSS0_SATA

V_CMPAVDD_SATA U1 CMPAVDD_SATA
V_CMPAVSS_SATA T1 CMPAVSS_SATA

V_VDD_SATA

T5 VDD_SATA<5>
R5 VDD_SATA<4>
P5 VDD_SATA<3>
N5 VDD_SATA<2>
M5 VDD_SATA<1>
L5 VDD_SATA<0>

FB2R2 FB 603 0.2A 0.5 DCR

C2R15 2.2 UF 10% 6.3 V X5R 603

C2R16 0.1 UF 10% 6.3 V X5R 402

ST2R1 SHORT

FB2T2 FB 603 0.2A 0.5 DCR

C2T8 2.2 UF 10% 6.3 V X5R 603

C2T5 0.1 UF 10% 6.3 V X5R 402

ST2T1 SHORT

FB2T1 FB 603 0.5 0.2DCR

C2T1 10 UF 20% 6.3 V X5R 805

C2T3 0.1 UF 10% 6.3 V X5R 402

C2T2 0.1 UF 10% 6.3 V X5R 402

T4 VSS_SATA<18>
R4 VSS_SATA<17>
M4 VSS_SATA<16>
L4 VSS_SATA<15>
K4 VSS_SATA<14>
J4 VSS_SATA<13>
T3 VSS_SATA<12>
R3 VSS_SATA<11>
P3 VSS_SATA<10>
N3 VSS_SATA<9>
K3 VSS_SATA<8>
T2 VSS_SATA<7>
N2 VSS_SATA<6>
M2 VSS_SATA<5>
L2 VSS_SATA<4>
K2 VSS_SATA<3>
R1 VSS_SATA<2>
P1 VSS_SATA<1>
L1 VSS_SATA<0>

VSS<41> N15
VSS<40> L15
VSS<39> K15
VSS<38> P14
VSS<37> N14
VSS<36> L14
VSS<35> K14
VSS<34> J14
VSS<33> R13
VSS<32> P13
VSS<31> N13
VSS<30> M13
VSS<29> L13
VSS<28> K13
VSS<27> J13
VSS<26> H13
VSS<25> N12
VSS<24> M12
VSS<23> L12
VSS<22> K12
VSS<21> P11
VSS<20> N11
VSS<19> M11
VSS<18> L11
VSS<17> K11
VSS<16> R10
VSS<15> P10
VSS<14> N10
VSS<13> M10
VSS<12> L10
VSS<11> K10
VSS<10> J10
VSS<9> H10
VSS<8> P9
VSS<7> N9
VSS<6> L9
VSS<5> K9
VSS<4> J9
VSS<3> N8
VSS<2> L8
VSS<1> K8
VSS<0> A15

X817692-001

[PAGE_TITLE=PSB, MAIN POWER + DECOUPLING]

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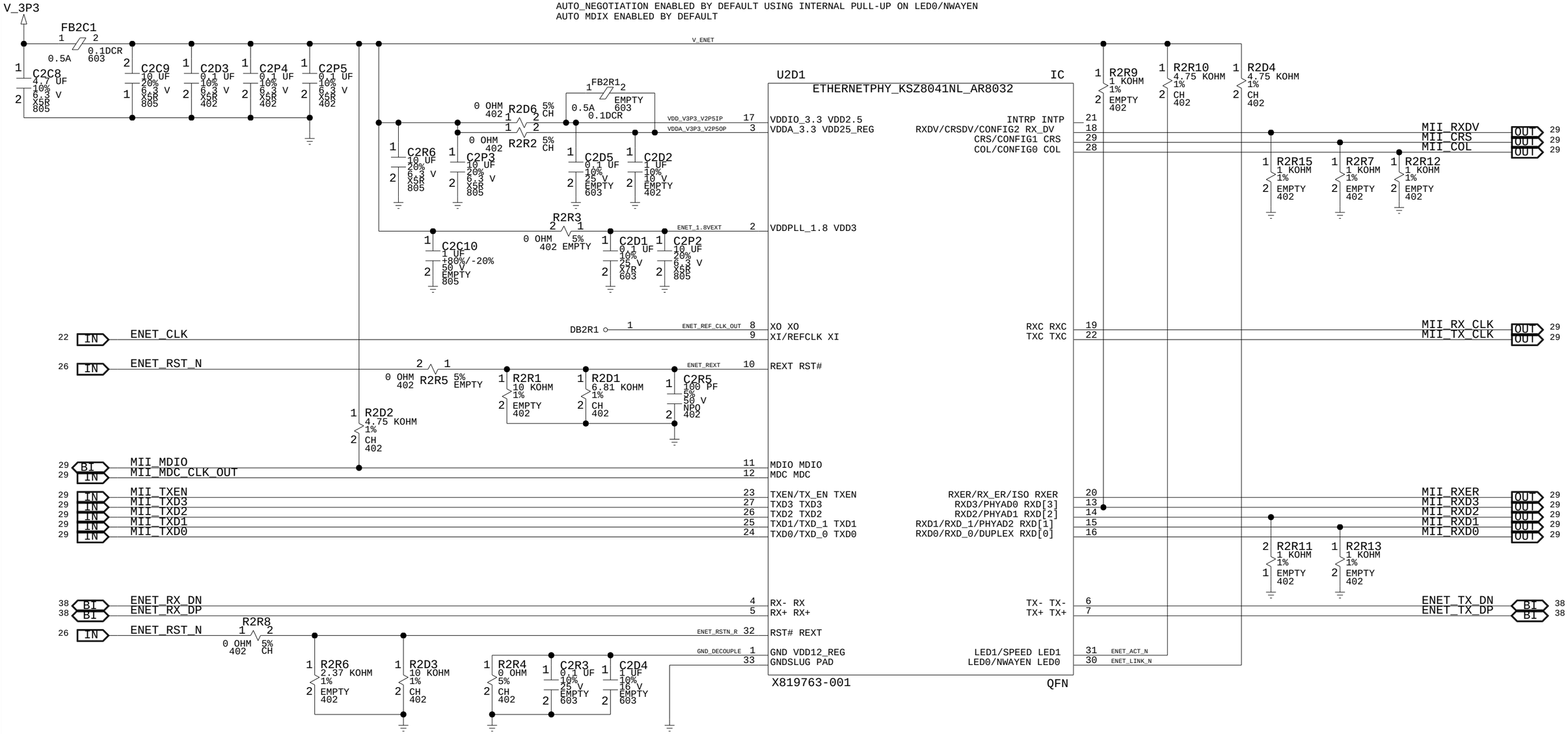
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	31/81	G	1.01

PSB OUT, ETHERNET

MICREL AND ATHEROS ENET PHY

NOTE : THIS PAGE OF THE SCHEMATIC DISPLAYS ONLY THE MICREL PART AND ITS ASSOCIATED STUFFING OPTIONS.
THE NO STUFF PARTS WILL BE STUFFED ALONG WITH THE ATHEROS PHY AND WILL BE IMPLEMENTED AS A BOM STUFFING OPTION..

DEFAULT ETHERNET PHY ADDRESS = 00001
AUTO_NEGOTIATION ENABLED BY DEFAULT USING INTERNAL PULL-UP ON LED0/NWAYEN
AUTO MDIX ENABLED BY DEFAULT



[PAGE_TITLE=PSB OUT, ETHERNET]

DRAWING
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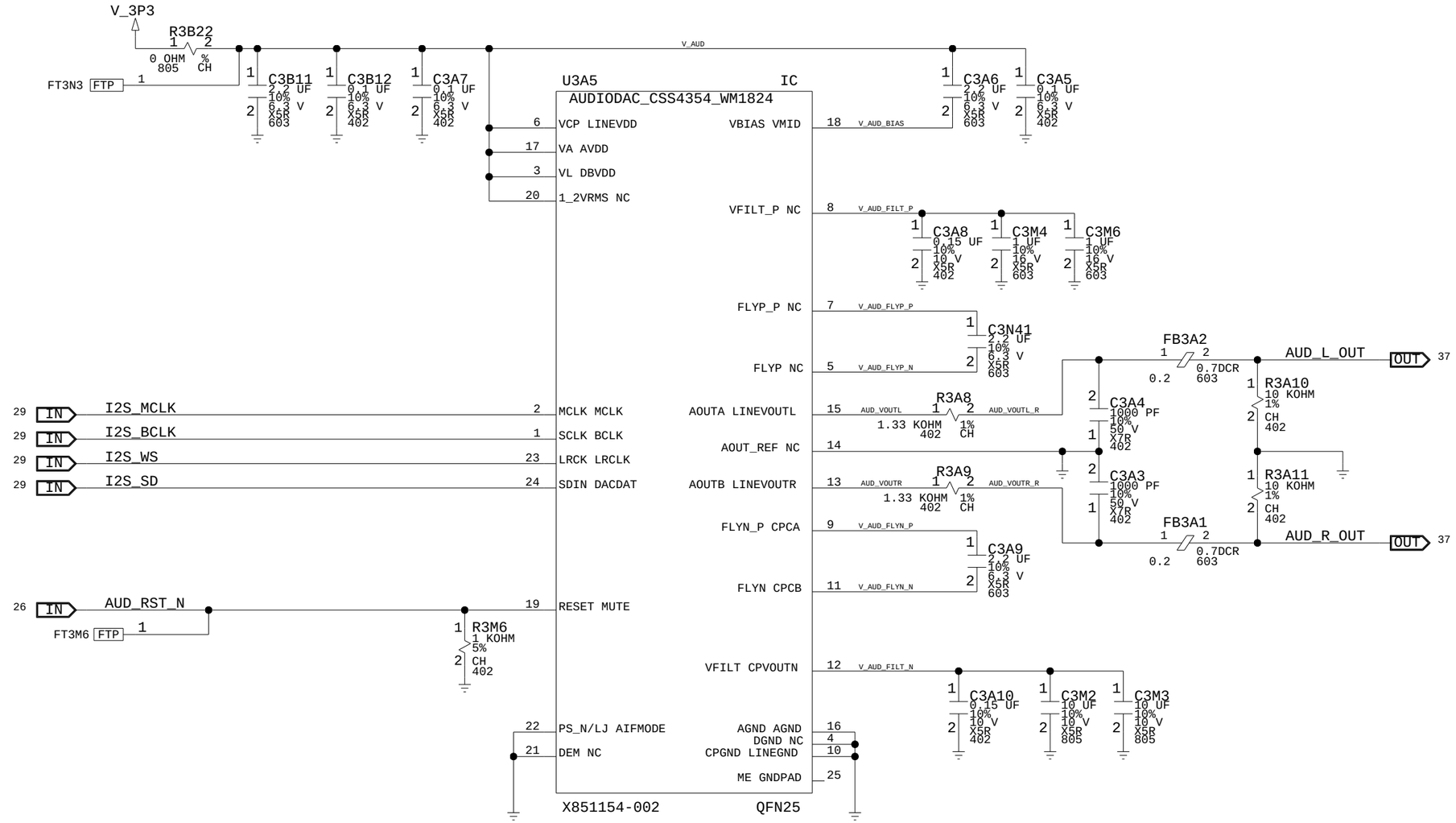
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	32/81	G	1.01

PSB OUT, AUDIO



[PAGE_TITLE=PSB OUT, AUDIO]

DRAWING
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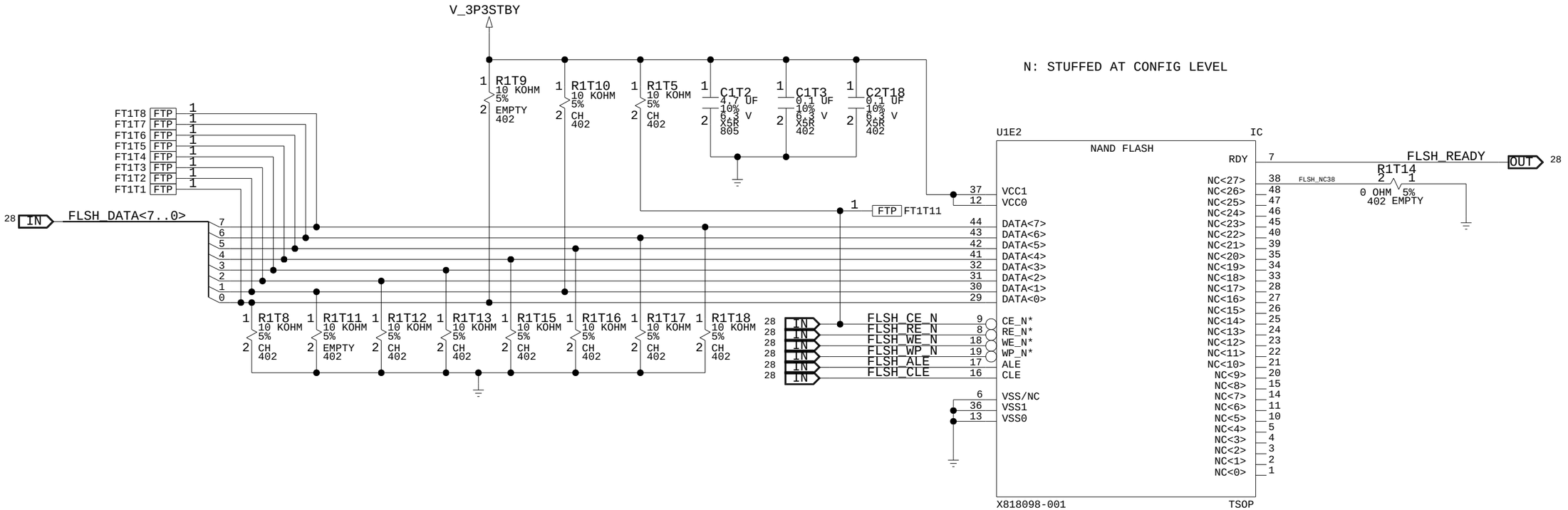
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	33/81	G	1.01

PSB OUT, FLASH



XSB SOUTHBRIDGE

FLSH_DATA1 \ FLSH_DATA0	0	1
0	8MB	16MB
1	32MB	64MB

N: RETAIL=16MB
N: XDK=64MB

PSB SOUTHBRIDGE

FLSH_DATA[1:0]	FLASH CONFIGURATION	
0X0	0.5KB, 16KB BLOCKS, 16MB	
0X1	0.5KB, 16KB BLOCKS, 16MB	RETAIL
0X2	2KB PAGES, 128KB BLOCKS, VARIOUS SIZES (256MB)	XDK
0X3	4KB PAGES, 256KB BLOCKS, VARIOUS SIZES	

[PAGE_TITLE=PSB OUT, FLASH]

DRAWING
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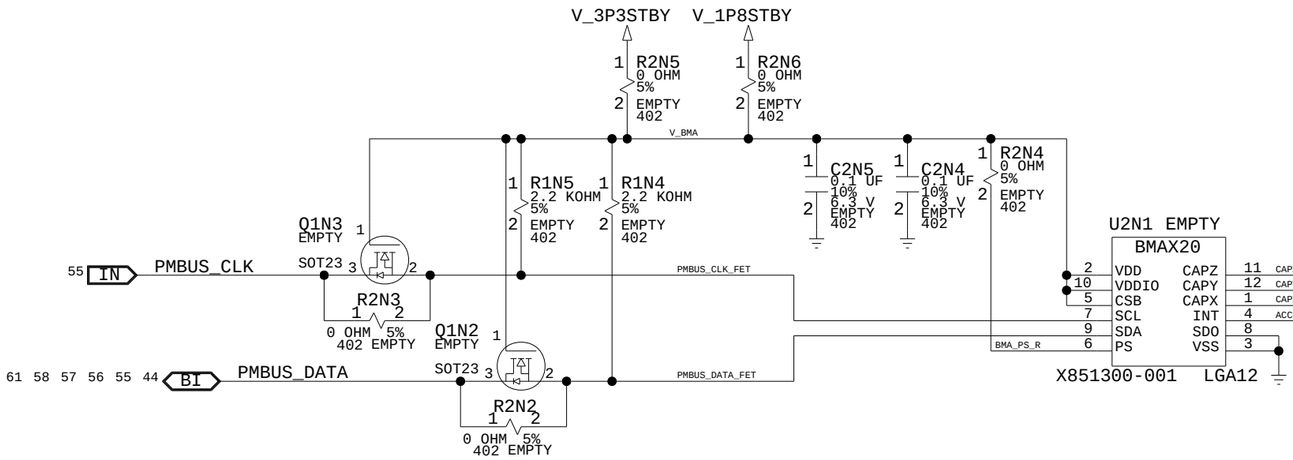
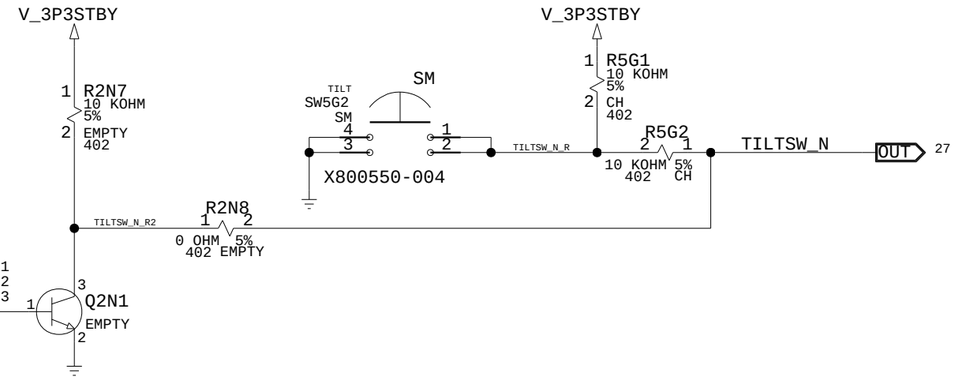
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	34/81	G	1.01

CONN, INFARED + ACCELEROMETER + SWITCHES + AUDIBLE F/B

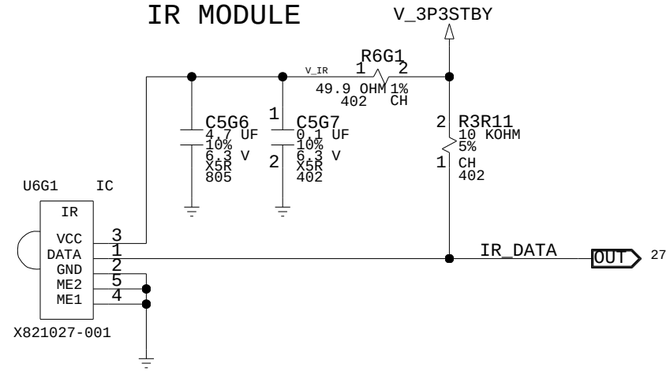
ACCELEROMETER



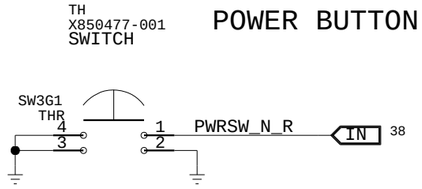
TILT SWITCH, SOLICO

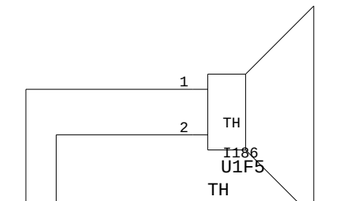


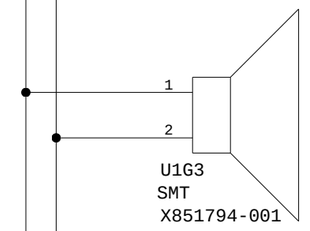
IR MODULE



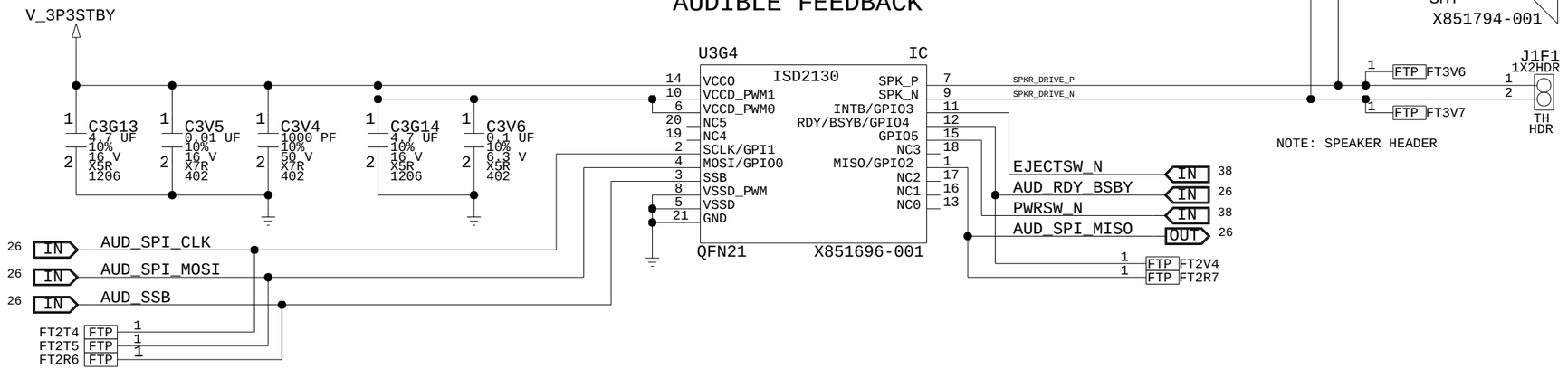
POWER BUTTON







AUDIBLE FEEDBACK

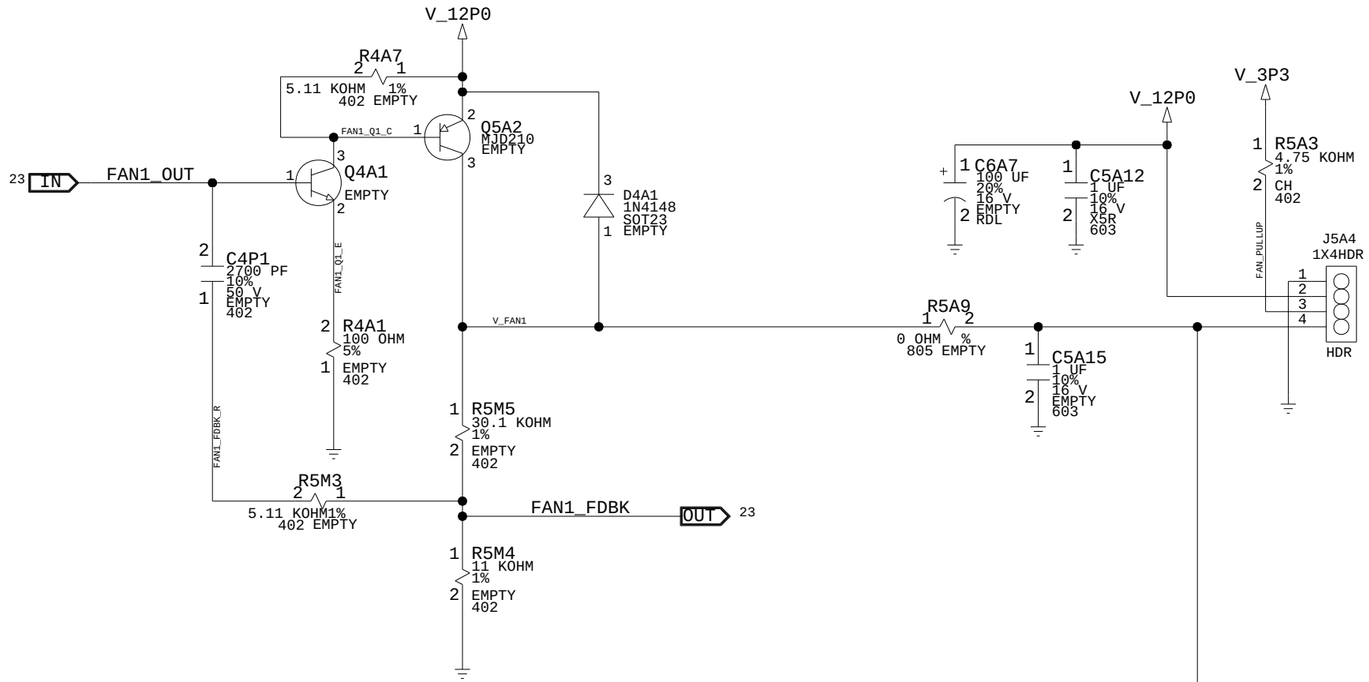


[PAGE_TITLE=CONN,INFARED+ACCELEROMETER+SWITCHES+AUDIBLE F/B]

DRAWING
Wed Feb 10 16:23:31 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	35/81	G	1.01

CONN, FAN



FAN CONTROL

[PAGE_TITLE= CONN, FAN]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	36/81	G	1.01

CONN, AVIP

DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS

V_5P0 — RT3A1 01.10 A THRMSTR 1206 — C2A8 4.7 UF 10% 6.3 V X5R 805 — C2A2 470 PF 5% 50 V X7R 402 — V_AVIP OUT 39 40

23 IN HANA_SPDIF_OUT — C2A3 22 PF 5% 50 V NPO 402 — EG2A1 X807267-001 ESDB-MLP7 DIO 402

J4A2 CONN — XENON AVIP CONNECTOR — X806743-001 TH

29	V_AVIP		
27	V_AVIP_RET		
37 IN	VID_DACA_OUT	4	VID_DACA_OUT
		2	VID_DACA_RET
37 IN	VID_DACB_OUT	3	VID_DACB_OUT
		1	VID_DACB_RET
37 IN	VID_DACC_OUT	8	VID_DACC_OUT
		6	VID_DACC_RET
37 IN	VID_DACD_OUT	7	VID_DACD_OUT
		5	VID_DACD_RET
37 IN	VID_HSYNC_OUT	11	VID_HSYNC_OUT
		9	VID_HSYNC_RET
37 IN	VID_VSYNC_OUT	12	VID_VSYNC_OUT
		10	VID_VSYNC_RET
		25	SPDIF
33 IN	AUD_R_OUT	15	AUD_R_OUT
		13	AUD_R_RET
33 IN	AUD_L_OUT	16	AUD_L_OUT
		14	AUD_L_RET
		17	WSS_CNTL
		19	SCART_RGB
EXT_PWR_ON	30	EXT_PWR_ON_N	OUT 59 60 27 37 61
DDC_CLK	21	HDMI_DDC_CLK	BI 23 27 40 55
DDC_DATA	23	HDMI_DDC_DATA	BI 23 27 40 55
AV_MODE2	28	AV_MODE2	OUT 27 37
AV_MODE1	24	AV_MODE1	OUT 27 37
AV_MODE0	20	AV_MODE0	OUT 27 37
GND<2>	26		
GND<1>	22		
GND<0>	18		
SHIELD<3>	34		
SHIELD<2>	33		
SHIELD<1>	32		
SHIELD<0>	31		
MTGB<8-1>			
MTGA<8-1>			

V_12P0 — R3A5 1.82 KOHM 1% CH 402

26 IN WSS_CNTL1 — R3A3 5.36 KOHM 1% CH 402 — Q3A1 XSTR — WSS_CNTL_B

26 IN WSS_CNTL0 — R3A4 4.75 KOHM 1% CH 402

WSS_CNTL_OUT_R — R3A2 1 KOHM 5% CH 402 — WSS_CNTL_OUT

WSS_CNTL_F — R3A6 301 OHM 1% CH 603 — R3A1 10 KOHM 5% CH 402

V_3P3 — C3A1 75 PF 5% 50 V NPO 402

26 IN SCART_RGB — R3M3 10 KOHM 5% CH 402 — SCART_RGB_R — Q3M1 XSTR — SCART_RGB_OUT_R — R3M7 33 OHM 5% CH 402 — SCART_RGB_OUT

R3M2 10 KOHM 5% CH 402 — C3M1 0.01 UF 10% 16 V X7R 402

V_3P3STBY

60 59 37 IN EXT_PWR_ON_N — R3R2 10 KOHM 5% CH 402

37 IN AV_MODE2 — R2N1 10 KOHM 5% CH 402

37 IN AV_MODE1 — R3R1 10 KOHM 5% CH 402

37 IN AV_MODE0 — R2C3 10 KOHM 5% CH 402

C3A2 470 PF 5% 50 V X7R 402 — C2M2 470 PF 5% 50 V X7R 402 — C2M1 470 PF 5% 50 V X7R 402 — C2C2 470 PF 5% 50 V X7R 402

LAYOUT:PLACE CLOSE TO CONNECTOR
EMI CAPS

23 IN VID_DACA_DP — L4A4 IND 1210 — VID_DACA_OUT OUT 37 — EG4A8 X807267-001 ESDB-MLP7 DIO 402 — R4A5 75 OHM 1% CH 402 — C4A10 62 PF 5% 50 V NPO 402 — C4A3 75 PF 5% 50 V NPO 402

23 IN VID_DACB_DP — L4A3 IND 1210 — VID_DACB_OUT OUT 37 — EG4A7 X807267-001 ESDB-MLP7 DIO 402 — R4A4 75 OHM 1% CH 402 — C4A9 62 PF 5% 50 V NPO 402 — C4A6 75 PF 5% 50 V NPO 402

23 IN VID_DACC_DP — L4A2 IND 1210 — VID_DACC_OUT OUT 37 — EG4A6 X807267-001 ESDB-MLP7 DIO 402 — R4A3 75 OHM 1% CH 402 — C4A8 62 PF 5% 50 V NPO 402 — C4A5 75 PF 5% 50 V NPO 402

23 IN VID_DACD_DP — L4A1 IND 1210 — VID_DACD_OUT OUT 37 — EG4A5 X807267-001 ESDB-MLP7 DIO 402 — R4A2 75 OHM 1% CH 402 — C4A7 62 PF 5% 50 V NPO 402 — C4A4 75 PF 5% 50 V NPO 402

23 IN VID_VSYNC_OUT_R — R4B20 49.9 OHM 1% CH 402 — VID_VSYNC_OUT OUT 37 — EG4A9 X807267-001 ESDB-MLP7 DIO 402

23 IN VID_HSYNC_OUT_R — R3B24 49.9 OHM 1% CH 402 — VID_HSYNC_OUT OUT 37 — EG4A10 X807267-001 ESDB-MLP7 DIO 402

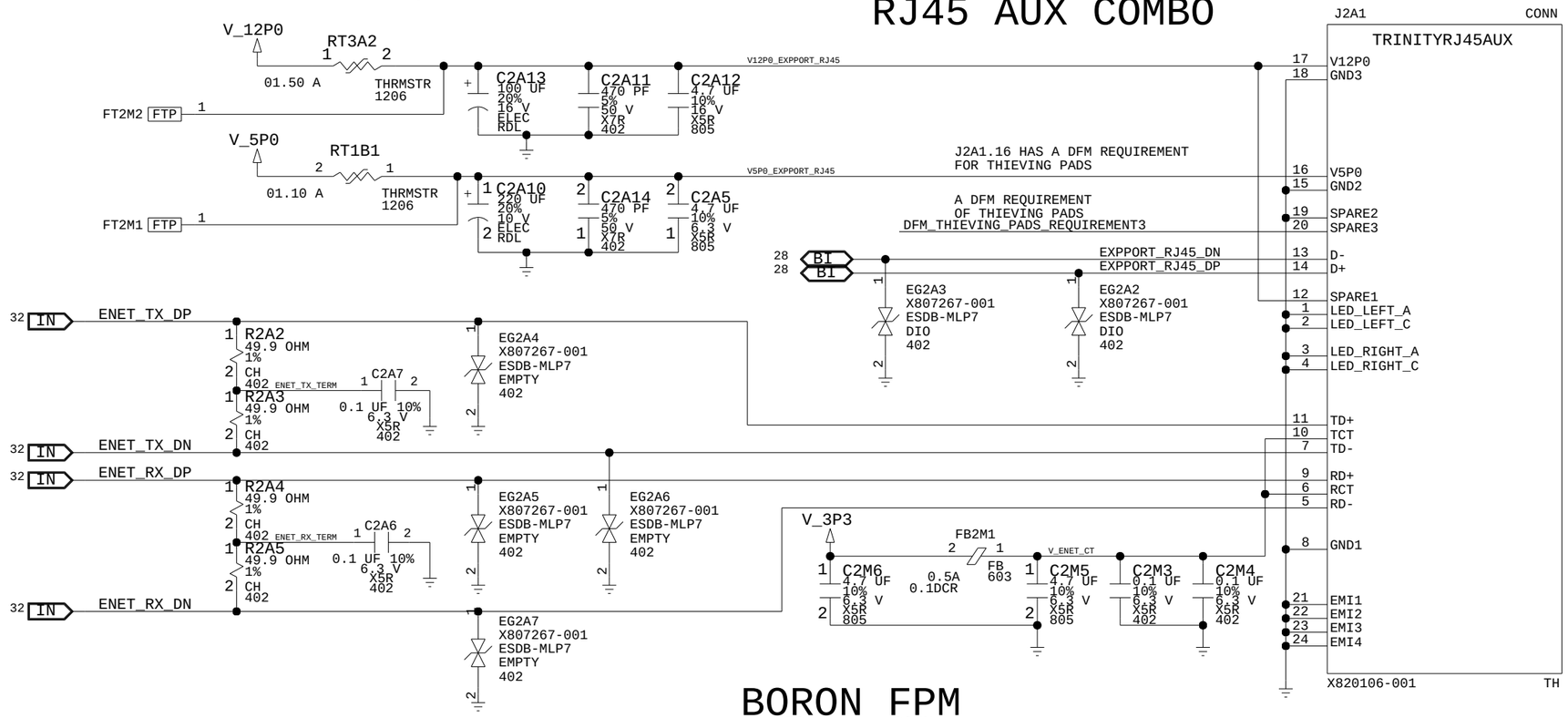
[PAGE_TITLE=[CONN, AVIP]

DRAWING
Wed Feb 10 16:23:31 2010

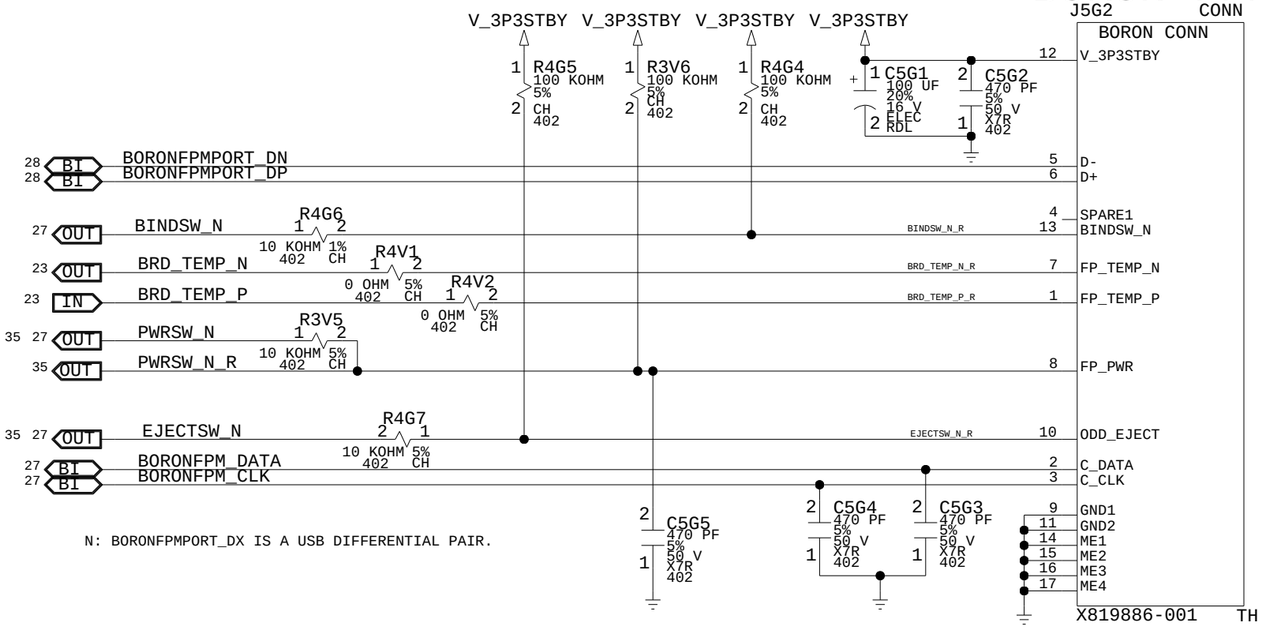
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	37/81	G	1.01

CONN, RJ45 USB AUX COMBO + BORON + PWR

RJ45 AUX COMBO

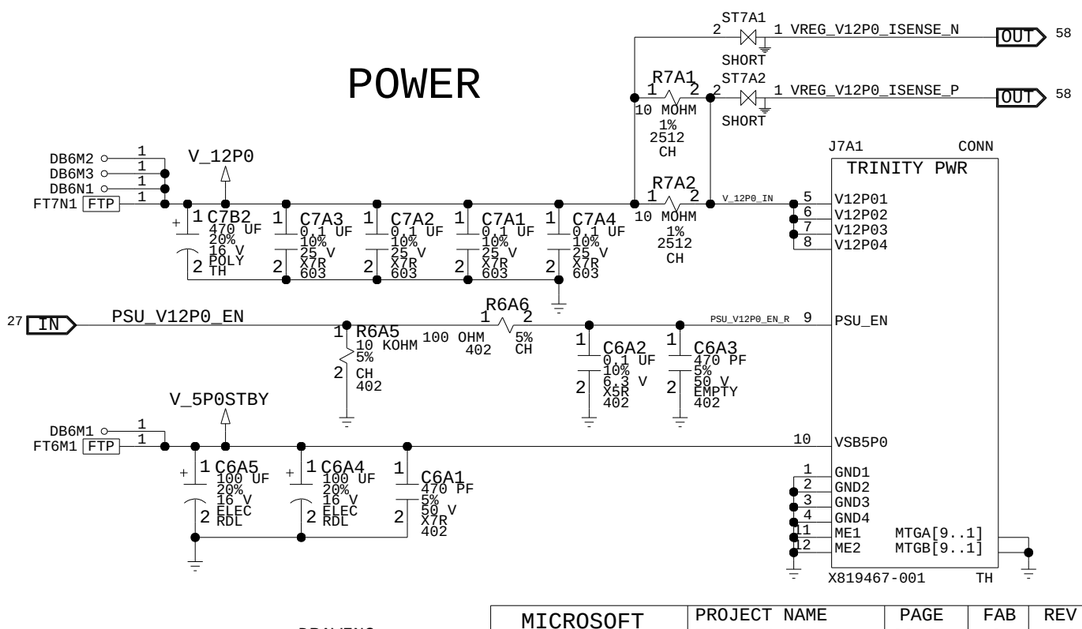


BORON FPM



N: BORONFPMPORT_DX IS A USB DIFFERENTIAL PAIR.

POWER



[PAGE_TITLE=CONN, RJ45 AUX COMBO + BORON + PWR]

DRAWING
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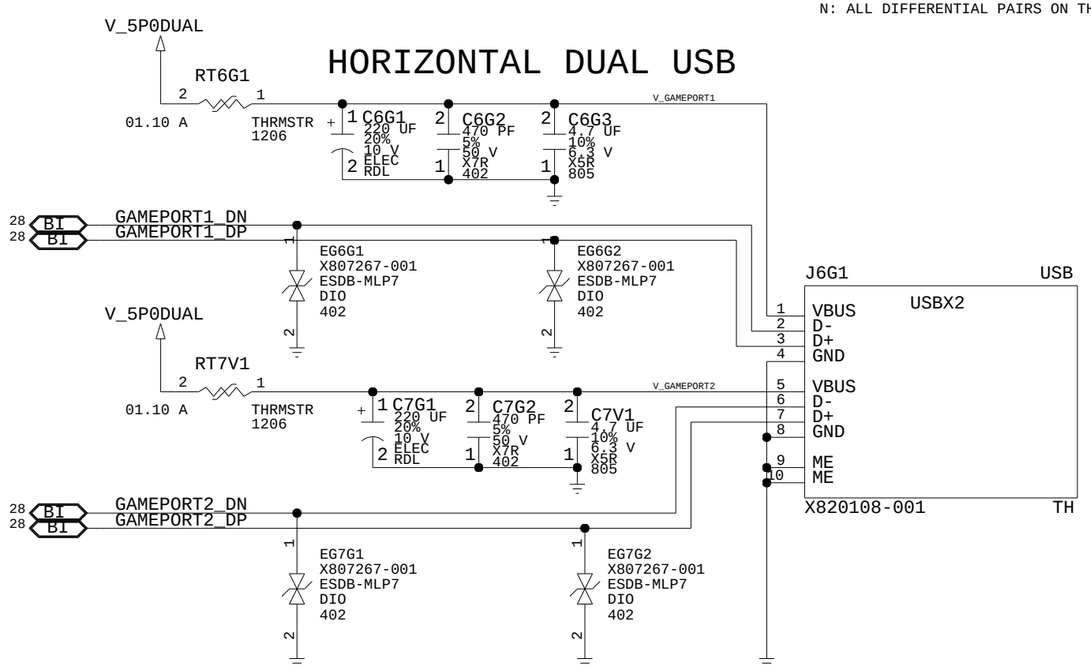
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	38/81	G	1.01

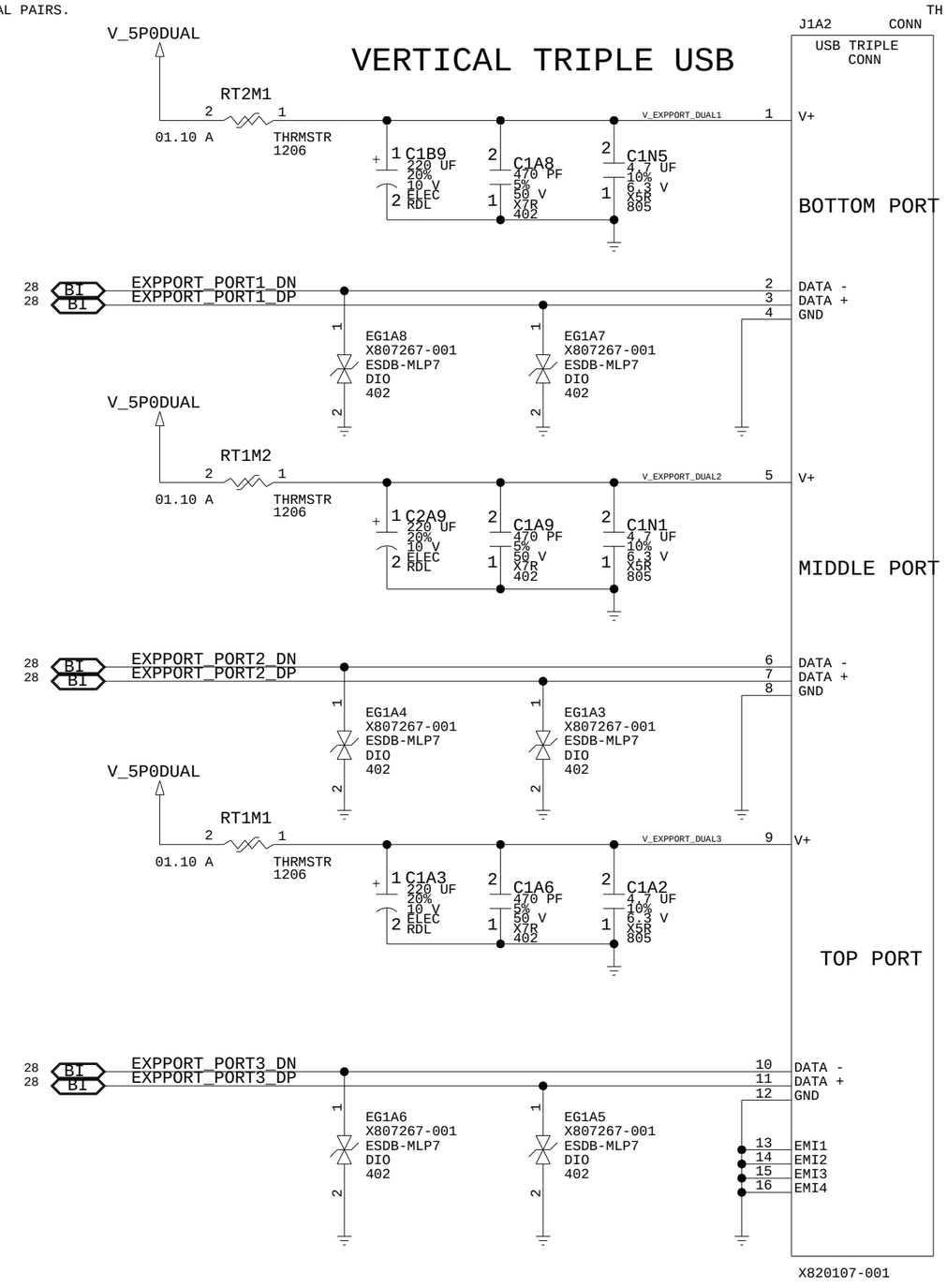
CONN, USB + MEM PORTS + TOSLINK + WAVEPORT

N: ALL DIFFERENTIAL PAIRS ON THIS PAGE ARE USB DIFFERENTIAL PAIRS.

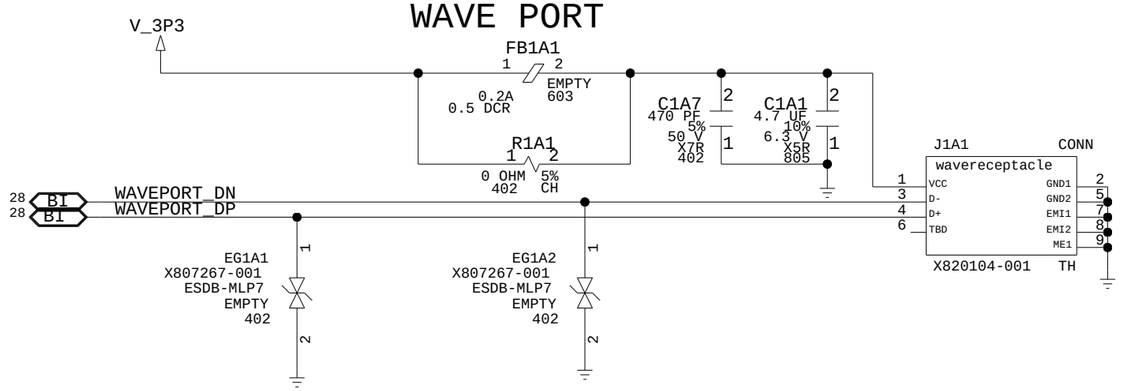
HORIZONTAL DUAL USB



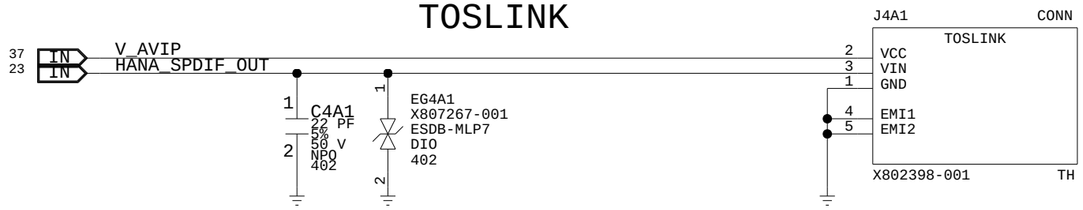
VERTICAL TRIPLE USB



WAVE PORT



TOSLINK



[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	39/81	G	1.01

CONN, HDMI

FT3M7 FTP 1
FT3M1 FTP 1
23 IN HDMI_TX2_DP
23 IN HDMI_TX2_DN
FT3M2 FTP 1
FT3M8 FTP 1
EG3A2 X807267-001 ESDB-MLP7 DIO 402
EG3A1 X807267-001 ESDB-MLP7 DIO 402

FT3M9 FTP 1
FT3M3 FTP 1
23 IN HDMI_TX1_DP
23 IN HDMI_TX1_DN
FT3M4 FTP 1
FT3M10 FTP 1
EG3A4 X807267-001 ESDB-MLP7 DIO 402
EG3A3 X807267-001 ESDB-MLP7 DIO 402

FT3M11 FTP 1
FT3M5 FTP 1
23 IN HDMI_TX0_DP
23 IN HDMI_TX0_DN
FT4M2 FTP 1
FT4M7 FTP 1
EG4A2 X807267-001 ESDB-MLP7 DIO 402
EG3A5 X807267-001 ESDB-MLP7 DIO 402

FT4M8 FTP 1
FT4M3 FTP 1
23 IN HDMI_TXC_DP
23 IN HDMI_TXC_DN
FT4M4 FTP 1
FT4M9 FTP 1
EG4A4 X807267-001 ESDB-MLP7 DIO 402
EG4A3 X807267-001 ESDB-MLP7 DIO 402

V_5P0STBY
R4M2 2 KOHM 1% 2 CH 402
R4M1 2 KOHM 1% 2 CH 402
FT4M5 FTP 1
37 27 23 IN HDMI_DDC_CLK
55 37 27 23 BI HDMI_DDC_DATA
FT4M1 FTP 1
EG4M2 X807267-001 ESDB-MLP7 DIO 402
EG4M1 X807267-001 ESDB-MLP7 DIO 402

37 IN V_AVIP
C2A1 0.1 UF 10% 6.3 V X5R 402

J3A1 HDR
HDMI
1 TMDS_DATA2_DP
2 TMDS_DATA2_SHD
3 TMDS_DATA2_DN
4 TMDS_DATA1_DP
5 TMDS_DATA1_SHD
6 TMDS_DATA1_DN
7 TMDS_DATA0_DP
8 TMDS_DATA0_SHD
9 TMDS_DATA0_DN
10 TMDS_CLK_DP
11 TMDS_CLK_SHD
12 TMDS_CLK_DN
13 CEC
14 RESERVED
15 SCL
16 SDA
17 DDC_CEC_GND
18 5VCC
19 HOT_PLUG_DET
23 ME4
22 ME3
21 ME2
20 ME1
X806395-002

DB3M1 1 HDMI_CEC

HDMI_HPD_PIN
R4M6 10 KOHM 5% 402 CH
1 FTP FT4M6
HDMI_HPD OUT 23
R4M5 47.5 KOHM 1% 2 CH 402
EG4M5 X807267-001 ESDB-MLP7 DIO 402

[PAGE_TITLE=CONN, HDMI]

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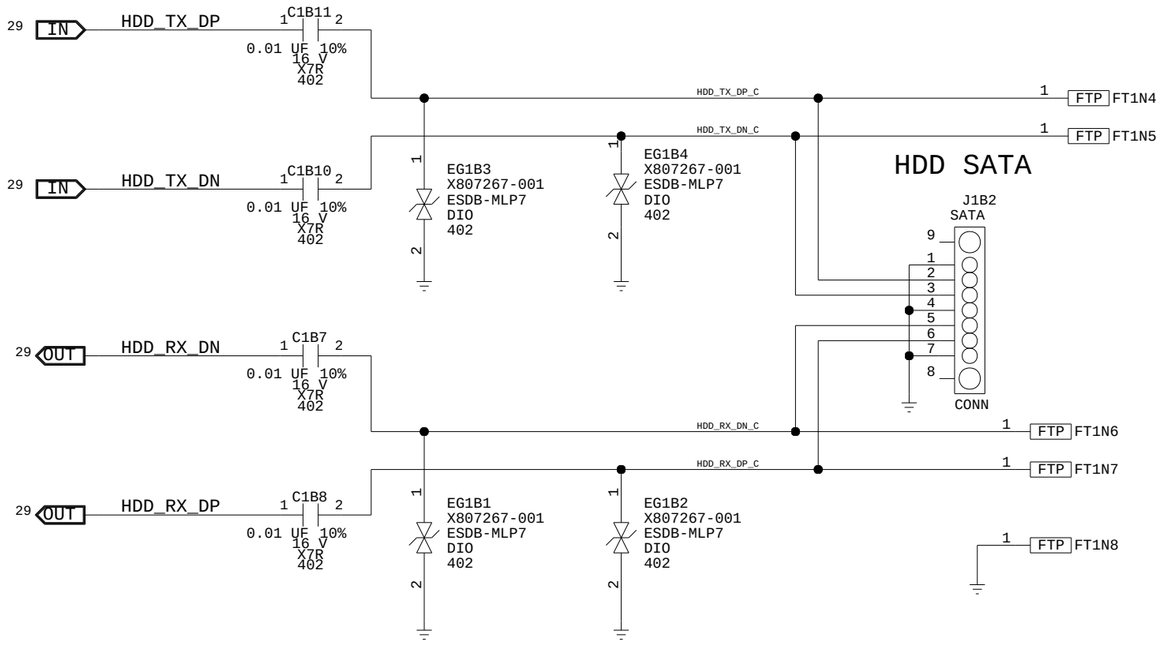
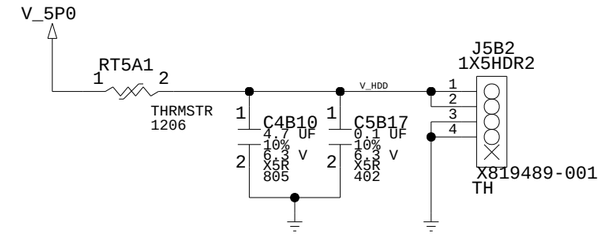
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	40/81	G	1.01

CONN, ODD + HDD + MU

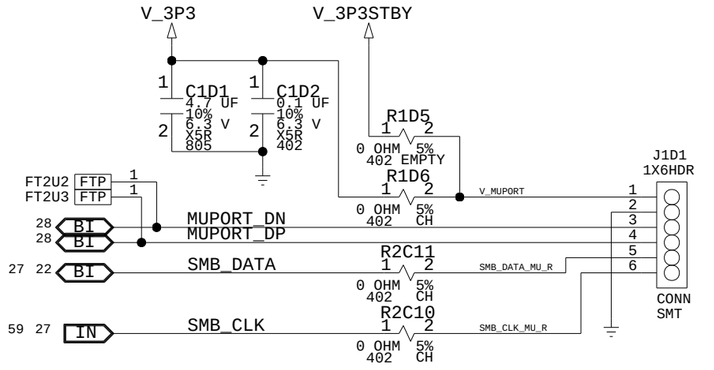
HDD SATA



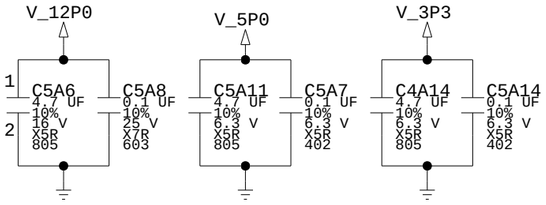
HDD POWER



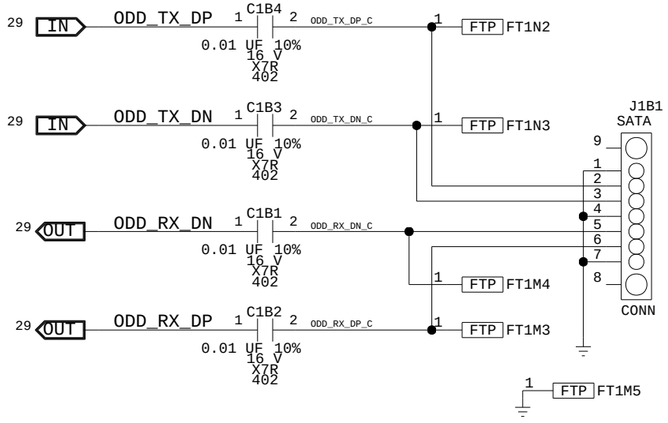
MEMORY UNIT



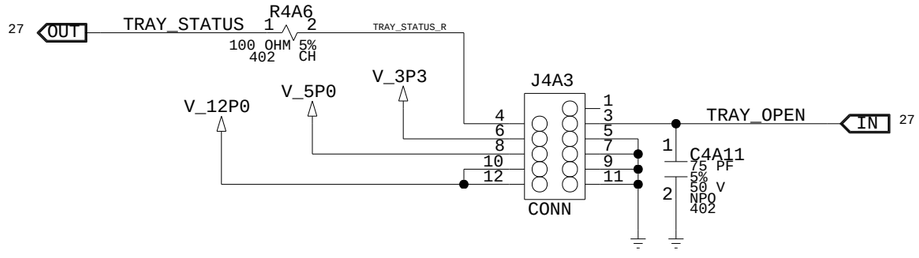
ODD POWER DECOUPLING



ODD SATA



ODD POWER AND CONTROL



[PAGE_TITLE=CONN, ODD + HDD + MU]

DRAWING
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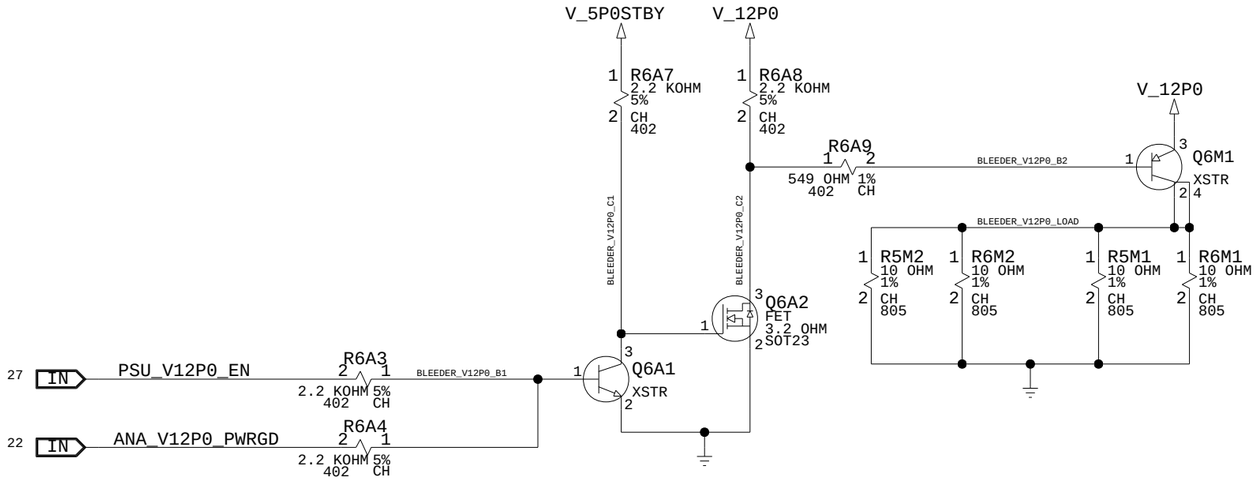
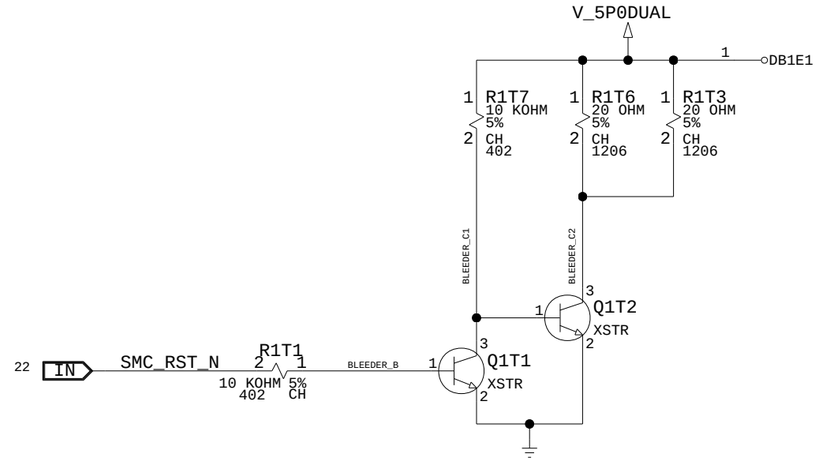
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	41/81	G	1.01

VREG, BLEEDERS



V_12P0 & V_5P0 BLEEDERS



V_5P0DUAL BLEEDER

[PAGE_TITLE= VREGS,_BLEEDERS]

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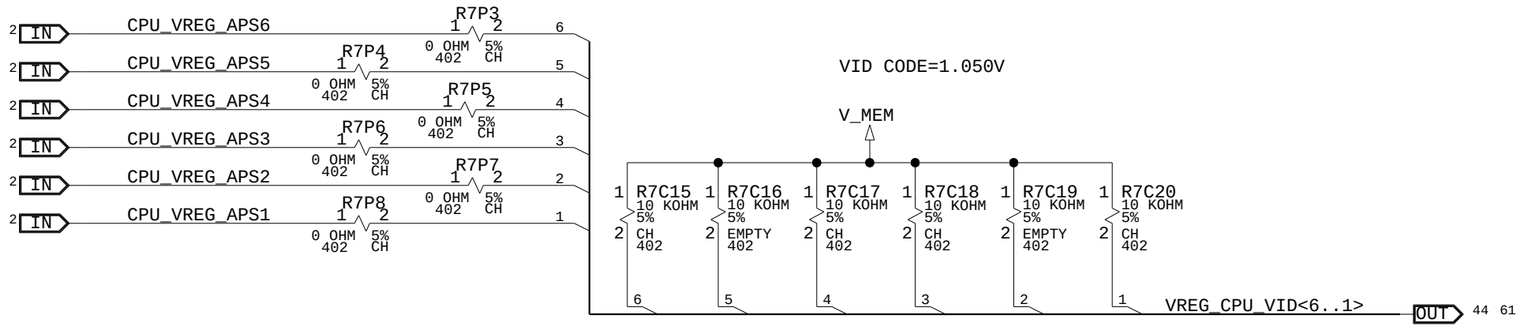
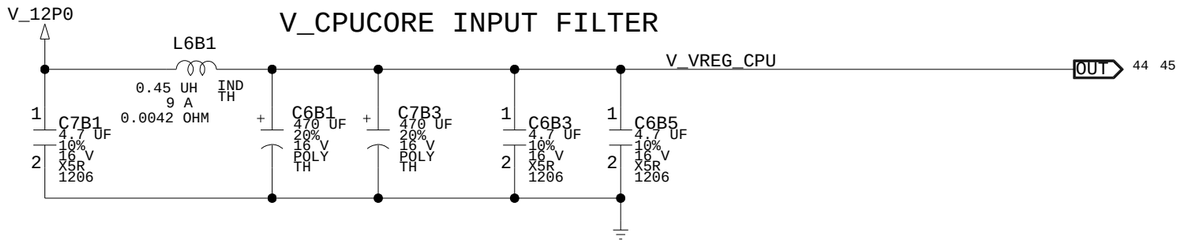
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	42/81	G	1.01

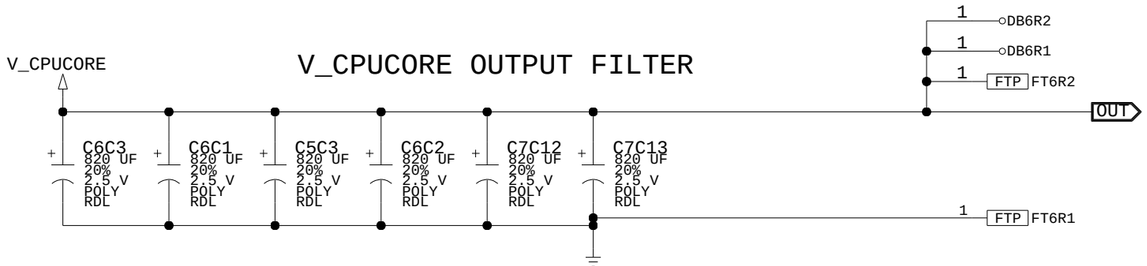
VREGS, INPUT + OUTPUT FILTERS



V_CPUCORE INPUT FILTER



V_CPUCORE OUTPUT FILTER



[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

DRAWING
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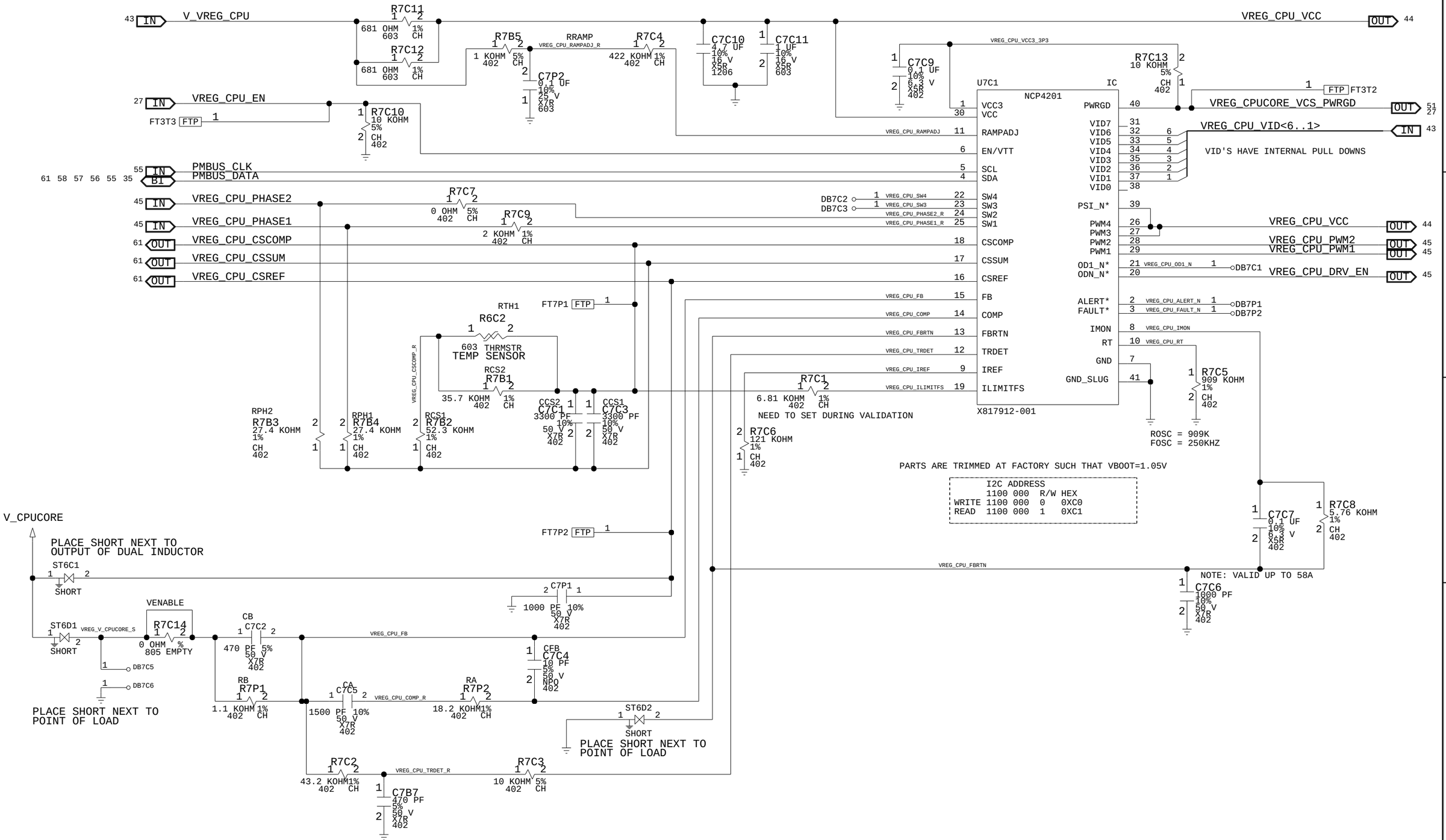
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	43/81	G	1.01

VREGS, CPU CONTROLLER



[PAGE_TITLE=VREGS, CPU CONTROLLER]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	44/81	G	1.01

VREG, CPU OUTPUT PHASE 1 & 2

43 IN V_VREG_CPU

R6N1 2.2 OHM 1% 805 CH — VREG_CPU2_VCC — C6B4 1 UF 10% 16 V X5R 603

D6B1 1N4148 SOT23 DIO

VREG_CPU_BST2 — C6N1 0.01 UF 10% 50 V EMPTY 805

R6N2 2.2 OHM 1% 805 CH — VREG_CPU_BST2_R — C6N2 0.1 UF 10% 25 V X7R 603

U6B1 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

44 IN VREG_CPU_PWM2
44 IN VREG_CPU_DRV_EN

VREG_CPU_DRVH2

Q6B2 X819086-001 DPAK FET

C7B5 4.7 UF 10% 16 V X5R 1206

C7N1 4.7 UF 10% 16 V EMPTY 1206

VREG_CPU_DRVL2

Q6C2 X819087-001 DPAK FET

Q6C1 X819087-001 DPAK FET

R6C1 1 OHM 1% CH 805 — VREG_CPU_SW2_R — C7C8 2200 PF 10% 50 V X7R 805

VREG_CPU_PHASE2 OUT 44

V_CPUCORE
NOM.VOLTAGE: 0.9-1.2V

V_CPUCORE

L6C1 SM EMPTY — DUAL INDUCTOR — X820048-001 420NH

DCR +/-8%

DB7C4

V_CPUCORE

L6C2 IND — DUAL INDUCTOR — X850592-001 420NH 40 A 0.66 +/-4%

NOTE: THRUHOLE PART IS 2% IMPROVEMENT ON DCR

R5N7 2.2 OHM 1% 805 CH — VREG_CPU1_VCC — C5B10 1 UF 10% 16 V X5R 603

D5B1 1N4148 SOT23 DIO

VREG_CPU_BST1 — C5N5 0.01 UF 10% 50 V EMPTY 805

R5N8 2.2 OHM 1% 805 CH — VREG_CPU_BST1_R — C5N6 0.1 UF 10% 25 V X7R 603

U5B5 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

44 IN VREG_CPU_PWM1

VREG_CPU_DRVH1

Q6B1 X819086-001 DPAK FET

C6B2 4.7 UF 10% 16 V X5R 1206

C6N3 4.7 UF 10% 16 V EMPTY 1206

VREG_CPU_DRVL1

Q5C3 X819087-001 DPAK FET

Q5C1 X819087-001 DPAK FET

R5C1 1 OHM 1% CH 805 — VREG_CPU_SW1_R — C5C1 2200 PF 10% 50 V X7R 805

VREG_CPU_PHASE1 OUT 44

[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2]

DRAWING
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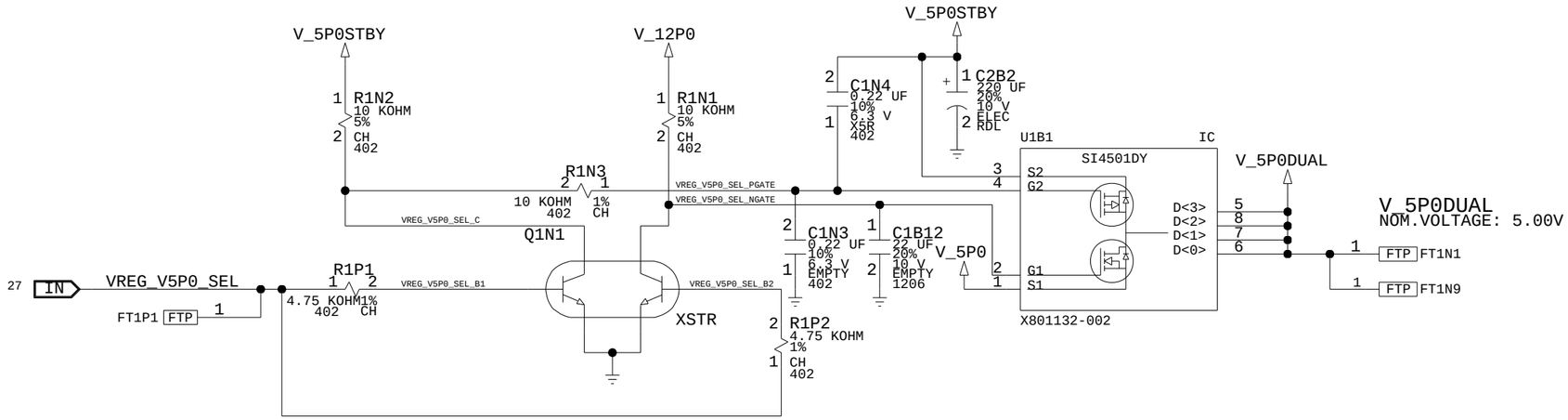
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	45/81	G	1.01

VREGS, V5P0 DUAL



VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=VREGS, V5P0 DUAL]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 46/81	FAB G	REV 1.01

VREGS, V5P0

V_12P0
L2B1
0.45 UH IND TH
9 A
0.0042 OHM
C2E8 330 UF 20% 16 V POLY TH
R1T4 10 OHM 1% CH 805
U1E1 1 OF 2 ADP1877
IC
R2T3 10 KOHM 5% CH 402
C2F3 4.7 UF 10% 16 V X5R 1206
C2F10 4.7 UF 10% 16 V EMPTY 1206
CIV1
V_VREG_V3P3_V5P0 OUT 48
VREG_V3P3_V5P0_VCCO OUT 48
VREG_V5P0_PWRGD OUT 27
VREG_V3P3_V5P0_VDL
VIN 3
VDL 5
VCCO 4
C2E2 1 UF 10% 16 V X5R 603
C1E1 1 UF 10% 16 V X5R 603
C1E2 1 UF 10% 16 V X5R 603
R1T2 0 OHM 5% CH 402
VREG_V3P3_V5P0_SYNC
SYNC 2
R1E12 0 OHM 5% EMPTY 402
PGOOD1 27
RAMP1 29 VREG_V5P0_RAMP
RR1 R2E6 820 KOHM 5% CH 402
ST2G2 SHORT
VREG_V5P0_ISENSE_P OUT 56
Q2F1 X819086-001 DPAK FET
ST2G3 SHORT
VREG_V5P0_ISENSE_N OUT 56
DH1 23 VREG_V5P0_DH
V_5P0
VOLTAGE: 5.09V
V_5P0
BST1 25 VREG_V5P0_BST
C2F1 0.1 UF 10% 25 V X7R 603
ST2U1 SHORT
VREG_V5P0_SW_S
L2F1 IND TH 1.6 UH 0.00375 OHM 10 A
VREG_V5P0_RSENSE
R2G1 10 MOHM 1% 2512 CH
C2V5 10 UF 20% 6.3 V EMPTY 805
C2V1 10 UF 20% 6.3 V EMPTY 805
C2G2 10 UF 20% 6.3 V EMPTY 805
C2V4 10 UF 20% 6.3 V EMPTY 805
C2G1 10 UF 20% 6.3 V EMPTY 805
R2G2 150 OHM 5% CH 1206
C2G5 820 UF 20% 6.3 V POLY TH
DB2G2
FTP FT2V2
DB2G4
SW1 24 VREG_V5P0_SW
FT2T2 FTP
R2E7 0 OHM 5% CH 402
VREG_V5P0_TRK
TRK1 32
C2E7 0.22 UF 10% 6.3 V EMPTY 402
27 IN VREG_V5P0_EN
R2E3 422 KOHM 1% CH 402
VREG_V5P0_EN_R
EN1 1
R2E2 10 KOHM 5% CH 402
C2E6 0.01 UF 10% 16 V X7R 402
ILIM1 26 VREG_V5P0_ILIM
RLIM1 R2F1 3.48 K 1% CH 402
Q2F2 X819086-001 DPAK FET
DL1 21 VREG_V5P0_DL
RGCS1 R1F3 22.1 KOHM 1% CH 402
RFREQ R1E17 97.6 KOHM 1% CH 402
VREG_V3P3_V5P0_FREQ
FREQ 7
PGND1 22 VREG_V5P0_PGND
ST2U2 SHORT
ST2G1 SHORT
VENABLE
R2F7 0 OHM EMPTY 805
VREG_V5P0_FB OUT 56
RF11 R2E4 7.5 KOHM 1% EMPTY 402
VREG_V5P0_COMP
COMP1 30
CC11 C2E3 3300 PF 10% 50 V X7R 402
COMP2 BW=
COMP1 BW=
CC12 C2E4 330 PF 5% 50 V NP0 402
VREG_V5P0_COMP_C
RC1 R2E5 11 KOHM 1% CH 402
VREG_V5P0_SS
SS1 28
CSS1 C2E5 0.047 UF 10% 10 V X7R 402
AGND 6
GNDSLUG 33
X817911-002
LCC32
FB1 31
FTP FT2T3
VREG_V5P0_FB_MID OUT 56
RF12 R2T4 1 KOHM 1% EMPTY 402

[PAGE_TITLE=VREGS, V5P0]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	47/81	G	1.01

VREGS, V3P3

47 IN V_VREG_V3P3_V5P0
47 IN VREG_V3P3_V5P0_VCCO

R1E14 10 KOHM 5% CH 402

U1E1 2 OF 2 IC ADP1877

PGOOD2 14 → VREG_V3P3_PWRGD OUT 27

RAMP2 12 VREG_V3P3_RAMP — RR2 R1E22 422 KOHM 1% 402 CH

DH2 18 VREG_V3P3_DH

R1E15 0 OHM 5% 402 CH — VREG_V3P3_TRK — 9 TRK2

FT1T10 FTP 1
27 IN VREG_V3P3_EN — 8 EN2

R1E16 10 KOHM 5% CH 402

BST2 16 VREG_V3P3_BST — C1F1 0.1 UF 10% 25 V X7R 603 — ST1U2 SHORT

U1F1 7 AMP FET
GATE0 SRC0 DRN0 DRN0
GATE1 SRC1 DRN1 DRN1
X807111-001 SO-8

SW2 17 VREG_V3P3_SW

RLIM2 R1F1 4.53 KOHM 1% 402 CH
ILIM2 15 VREG_V3P3_ILIM

RGCS2 R1F2 22.1 KOHM 1% 402 CH
DL2 20 VREG_V3P3_DL

RR1 ST1U1 SHORT
PGND2 19 VREG_V3P3_PGND

CIV2 C1U1 4.7 UF 10% 16 V X5R 1206

VREG_V3P3_SW_S — L1F1 0.02 2.3 UH 6 A IND TH — VREG_V3P3_RSENSE

R1F9 30 MOHM 2512 CH 1%

ST1F1 SHORT — VREG_V3P3_ISENSE_P OUT 56
ST1F3 SHORT — VREG_V3P3_ISENSE_N OUT 56

V_3P3 VOLTAGE: 3.3V
V_3P3 — FTP FT2V3 — DB2G1

C1F9 4.7 UF 10% 6.3 V X5R 805
C1F6 4.7 UF 10% 6.3 V X5R 805
C1G2 4.7 UF 10% 6.3 V X5R 805
C1F3 4.7 UF 10% 6.3 V X5R 805
DB1F2

VENABLE
R2F9 0 OHM % 805 EMPTY — ST1F2 SHORT

VREG_V3P3_FB → OUT 56

RF21 R1E20 4.53 KOHM 1% EMPTY 402

FB2 10

FTP FT1T9 — VREG_V3P3_FB_MID → OUT 56

RF22 R1E19 1 KOHM 1% EMPTY 402

VREG_V3P3_COMP — 11 COMP2
CC21 C1E3 3300 PF 10% 50 V X7R 402
CC22 C1E4 120 PF 5% 50 V NP0 402
VREG_V3P3_COMP_C
RC2 R1E21 7.87 KOHM 1% CH 402

VREG_V3P3_SS — 13 SS2
CSS2 C1E5 0.047 UF 10% 10 V X7R 402

X817911-002 — LCC32

[PAGE_TITLE=VREGS, V3P3]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	48/81	G	1.01

VREGS, VEDRAM

V_12P0
L7B1
0.45 UH IND TH
9 A
0.0042 OHM
C3F8 330 UF 20% 16 V POLY TH
C7B8 470 UF 20% 16 V POLY TH
R3G2 10 OHM 1% CH 805
U3G1 1 OF 2 ADP1877 IC
R3G16 10 KOHM 5% CH 402
C3F1 4.7 UF 10% 16 V X5R 1206
C3F7 4.7 UF 10% 16 V EMPTY 1206 CIV1
V_VREG_VMEM_VEDRAM OUT 50
VREG_VMEM_VEDRAM_VCCO OUT 50
FTP FT3V4
VREG_VEDRAM_PWRGD OUT 27
C3G1 1 UF 10% 16 V X5R 603
C3G3 1 UF 10% 16 V X5R 603
C3V1 1 UF 10% 16 V X5R 603
VREG_VMEM_VEDRAM_VDL
VIN
VDL
VCCO
SYNC HIGH=FORCED PWM MODE
SYNC LOW =PULSE SKIP MODE
R3F12 0 OHM 5% CH 402
R3F14 0 OHM 5% CH 402
VREG_VMEM_VEDRAM_SYNC
SYNC
R3F13 0 OHM 5% EMPTY 402
VREG_VEDRAM_TRK
TRK1
PGOOD1
RAMP1
VREG_VEDRAM_RAMP
RR1 R3F10 680 KOHM 5% 402 CH
ST4F2 SHORT
VREG_VEDRAM_ISENSE_P OUT 55
ST4F4 SHORT
VREG_VEDRAM_ISENSE_N OUT 55
Q3F1 X819086-001 DPAK FET
DH1
VREG_VEDRAM_DH
V_CPUEDRAM
V_CPUEDRAM VOLTAGE: 1.075V
FTP FT5T4
DB4E3
L4F1 1.7 UH 13.8 A IND TH 0.0034 OHM
VREG_VEDRAM_RSENSE
R4F1 10 MOHM 2512 1%
C4E3 820 UF 20% 2.5 V POLY RDL
C4E6 820 UF 20% 2.5 V POLY RDL
C4F7 820 UF 20% 2.5 V EMPTY RDL
BST1
C3F5 0.1 UF 10% 25 V X7R 603
ST3F1 SHORT
VREG_VEDRAM_SW_S
SW1
VREG_VEDRAM_SW
RLIM1 R3F7 3.32 KOHM 1% 402 CH
ILIM1
VREG_VEDRAM_ILIM
C5T52 4.7 UF 10% 16 V EMPTY 1206
C5E11 4.7 UF 10% 16 V EMPTY 1206
C4T7 4.7 UF 10% 16 V EMPTY 1206
C5E10 4.7 UF 10% 16 V EMPTY 1206
Q4F1 X819086-001 DPAK FET
DL1
VREG_VEDRAM_DL
RGCS1 R3V1 22.1 KOHM 1% CH 402
ST4F1 SHORT
DB4E4
DB4E5
VENABLE
R3F11 0 OHM EMPTY 805
PGND1
VREG_VEDRAM_PGND
ST4U1 SHORT
VREG_VEDRAM_FB OUT 55
RF11 R3F8 7.87 KOHM 1% EMPTY 402
FB1
FTP FT3U1
VREG_VEDRAM_FB_MID OUT 55
RF12 R3F9 10 KOHM 1% EMPTY 402
FT3V1 FTP
27 IN VREG_VEDRAM_EN
R3F15 10 KOHM 5% CH 402
EN1
RFREQ R3G4 97.6 KOHM 1% 402 CH
VREG_VEDRAM_FREQ
FREQ
VREG_VEDRAM_COMP
COMP1
CC11 C3F2 4700 PF 10% 50 V X7R 402
CC12 C3F3 62 PF 5% 50 V NPO 402
VREG_VEDRAM_COMP_C
RC1 R3F6 43.2 KOHM 1% CH 402
RC1=120K
VREG_VEDRAM_SS
SS1
CSS1 C3F4 0.047 UF 10% 10 V X7R 402
AGND
GNDSLUG
X817911-002
LCC32

[PAGE_TITLE=[VREGS, VEDRAM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	49/81	G	1.01

VREGS, VMEM

49 IN V_VREG_VMEM_VEDRAM

49 IN VREG_VMEM_VEDRAM_VCCO

U3G1 2 OF 2 ADP1877 IC

R3G15 10 KOHM 5% CH 402

CIV2 C7F3 4.7 UF 10% 16 V X5R 1206

C7U1 4.7 UF 10% 16 V EMPTY 1206

FTP FT3V5

R3R5 0 OHM 5% CH 402

PGOOD2 14 VREG_VMEM_PWRGD_R

VREG_VMEM_PWRGD_CPU_TRST_N_R OUT 27

RAMP2 12 VREG_VMEM_RAMP

RR2 R3G13 680 KOHM 5% CH 402

ST7F2 SHORT

VREG_VMEM_ISENSE_P OUT 55

ST7F3 SHORT

VREG_VMEM_ISENSE_N OUT 55

Q7G1 X819086-001 DPAK FET

V_MEM VOLTAGE: 1.8V

R3G5 0 OHM 5% CH 402

VREG_VMEM_TRK 9 TRK2

DH2 18 VREG_VMEM_DH

DB7F1

FTP FT6U1

V_MEM

FT3V3 FTP

27 IN VREG_VMEM_EN

8 EN2

R3G14 10 KOHM 5% CH 402

BST2 16 VREG_VMEM_BST

C3G9 0.1 UF 10% 25 V X7R 603

ST6V2 SHORT

VREG_VMEM_SW_S

L7F1 IND TH 1.7 UH 13.8 A 0.0034 OHM

VREG_VMEM_RSENSE

R7F1 10 MOHM 1% CH 2512

C7F2 820 UF 20% 2.5 V POLY RDL

C7F1 4.7 UF 10% 6.3 V EMPTY 805

DB7F2

SW2 17 VREG_VMEM_SW

V_MEM

RLIM2 R3G10 3.32 KOHM 1% CH 402

ILIM2 15 VREG_VMEM_ILIM

Q7G2 X819086-001 DPAK FET

C7R1 330 UF 20% 2.5 V EMPTY SM

V_MEM

DL2 20 VREG_VMEM_DL

RGCS2 R4G3 22.1 KOHM 1% CH 402

C4U4 330 UF 20% 2.5 V EMPTY SM

ST7F1 SHORT

PGND2 19 VREG_VMEM_PGND

ST6V1 SHORT

VENABLE R3G17 0 OHM 5% EMPTY 805

VREG_VMEM_FB OUT 55

RF21 R3G11 20 KOHM 1% EMPTY 402

FTP FT3V2

VREG_VMEM_FB_MID OUT 55

FB2 10

RF22 R3G12 10 KOHM 1% EMPTY 402

VREG_VMEM_COMP 11 COMP2

CC21 C3G6 4700 PF 10% 50 V X7R 402

CC22 C3G7 62 PF 5% 50 V NPO 402

VREG_VMEM_COMP_C

RC2 R3V4 43.2 KOHM 1% CH 402

VREG_VMEM_SS 13 SS2

CSS1 C3G8 0.047 UF 10% 10 V X7R 402

X817911-002 LCC32

[PAGE_TITLE=[VREGS, VMEM]

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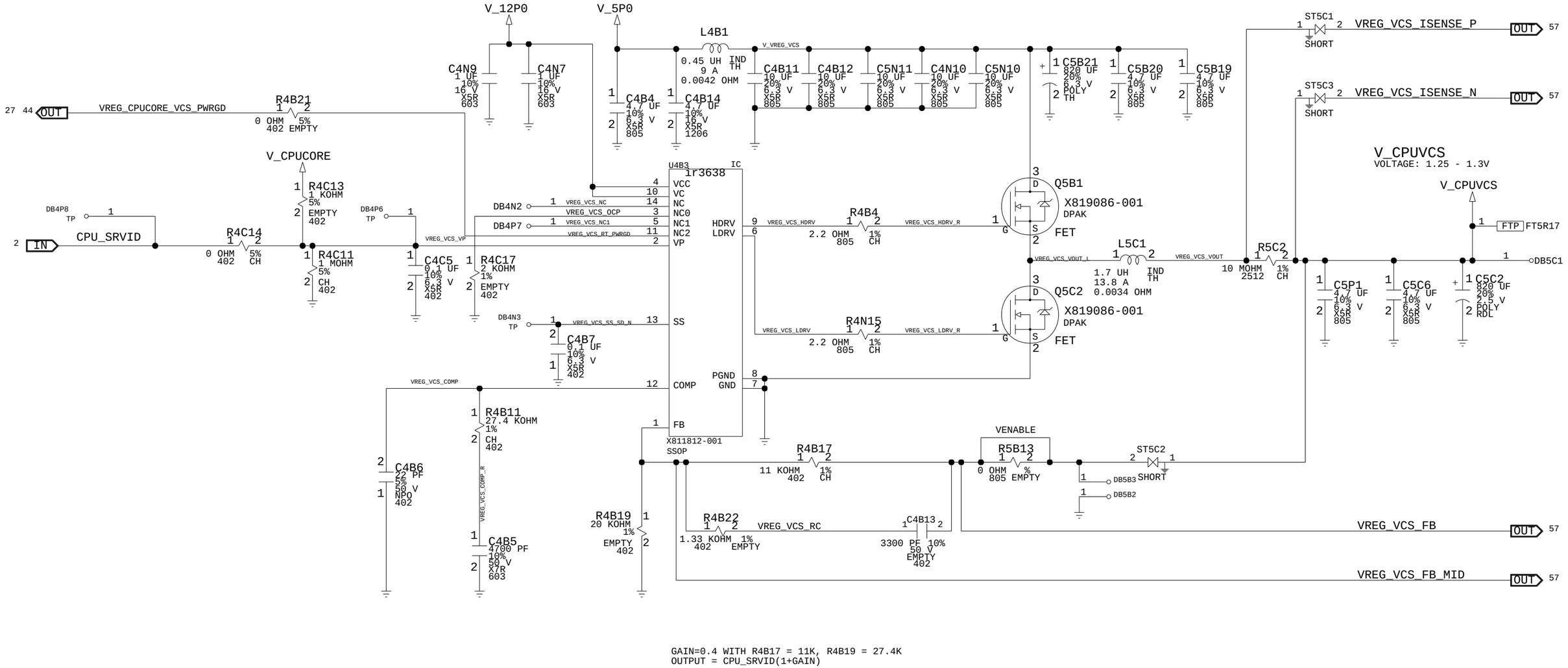
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	50/81	G	1.01

VREGS, VCS



GAIN=0.4 WITH R4B17 = 11K, R4B19 = 27.4K
OUTPUT = CPU_SRVID(1+GAIN)

[PAGE_TITLE=VREGS, VCS]

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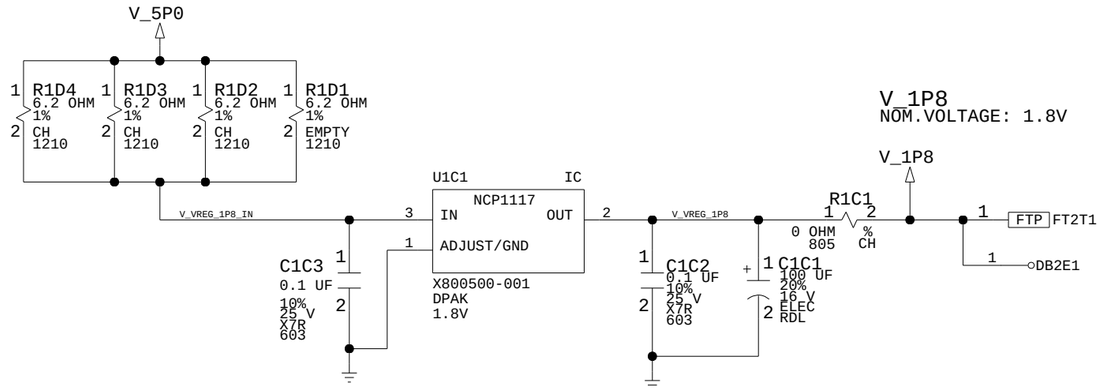
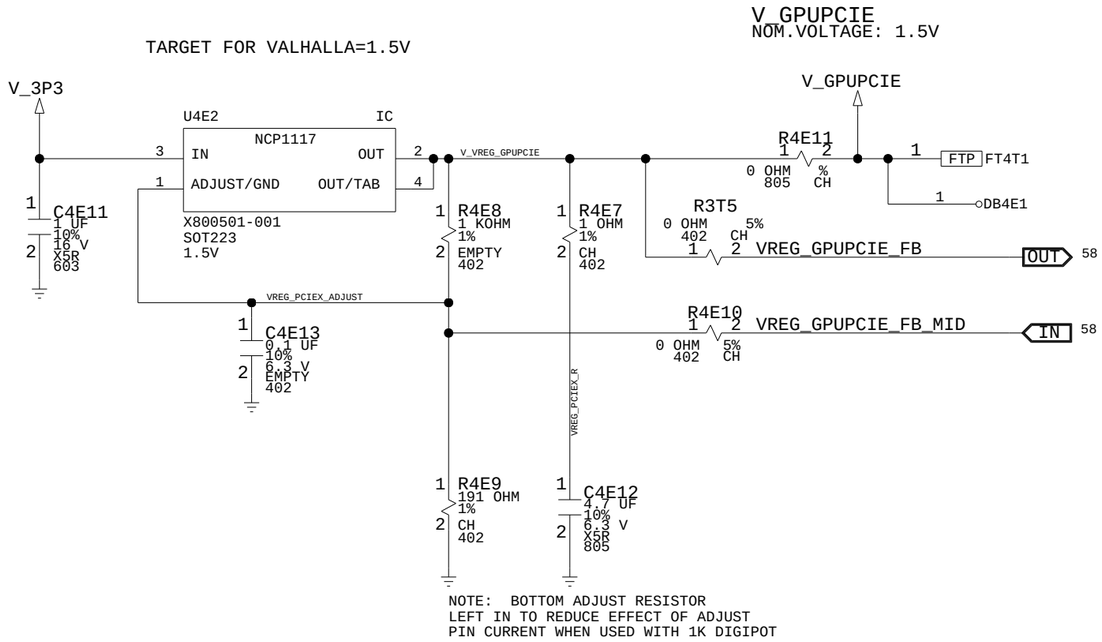
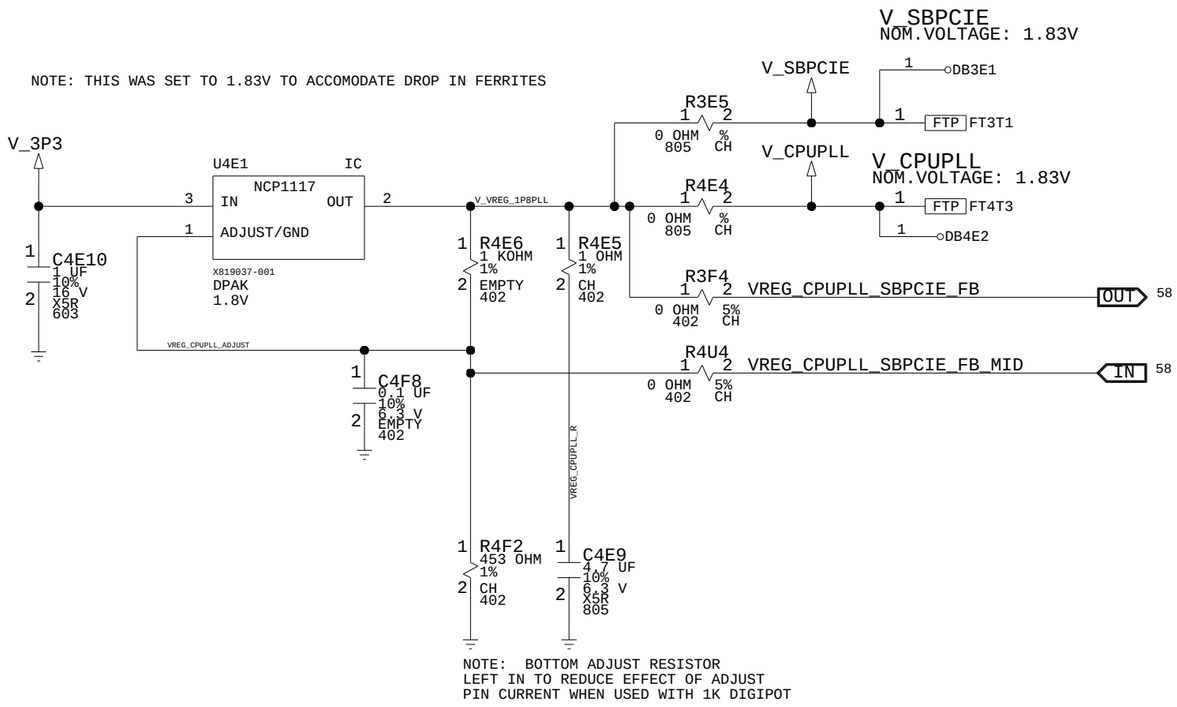
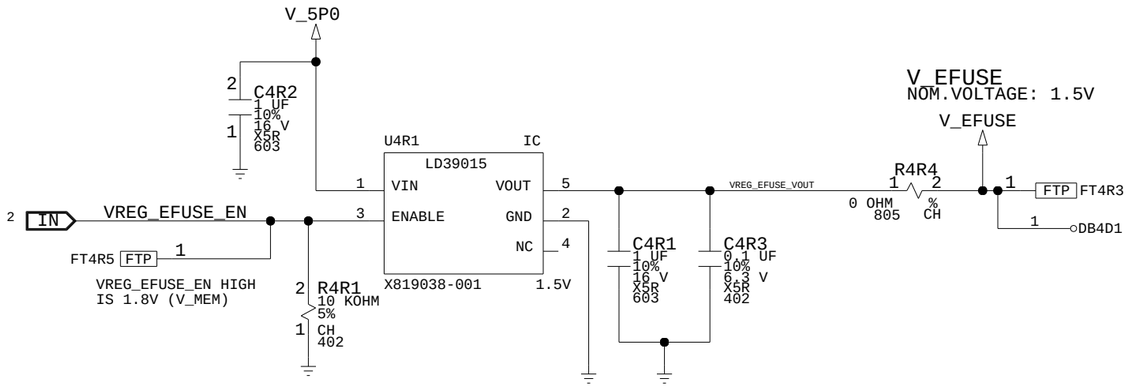
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	51/81	G	1.01

VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE









[PAGE_TITLE=VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE]

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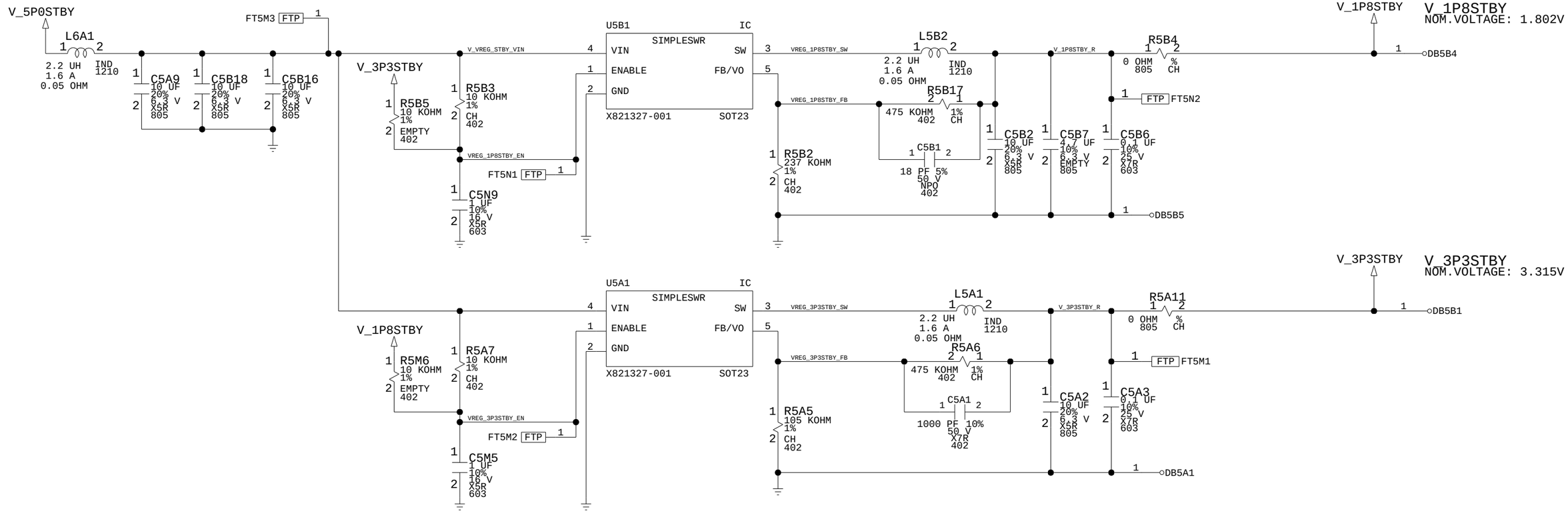
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	52/81	G	1.01

VREGS, STANDBY SWITCHERS



[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

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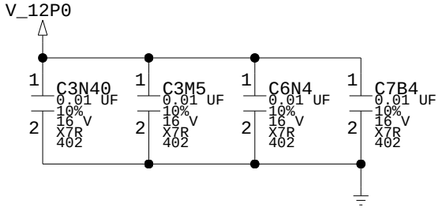
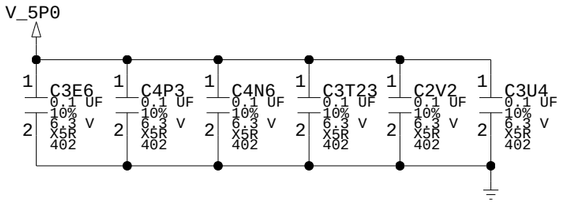
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	53/81	G	1.01

BOARD LEVEL DECOUPLING

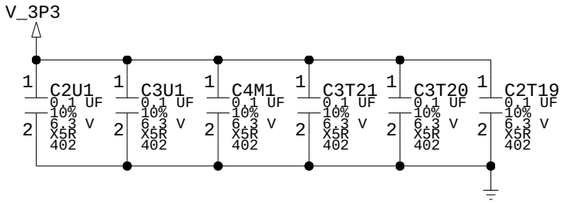
V_12P0



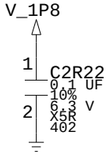
V_5P0



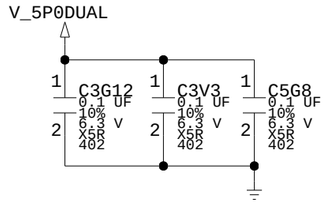
V_3P3



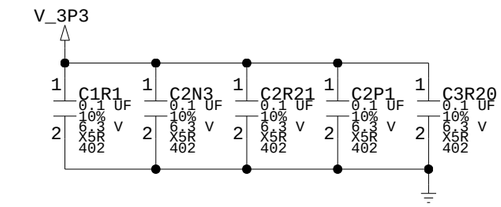
V_1P8



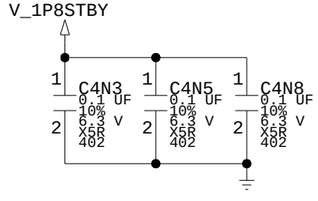
V_5P0DUAL



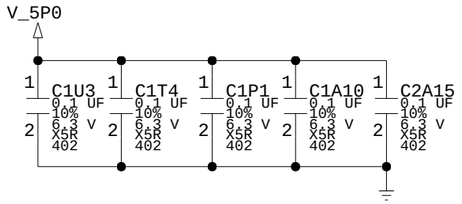
V_3P3



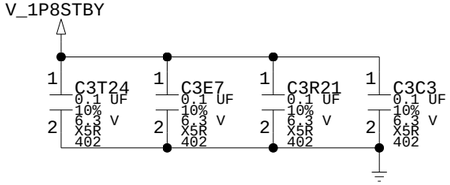
V_1P8STBY



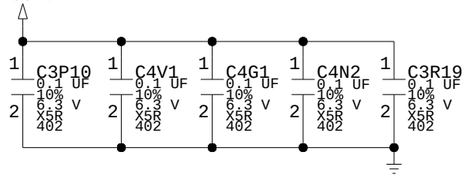
V_5P0



V_1P8STBY



V_3P3STBY



[PAGE_TITLE=BOARD, DECOUPLE]

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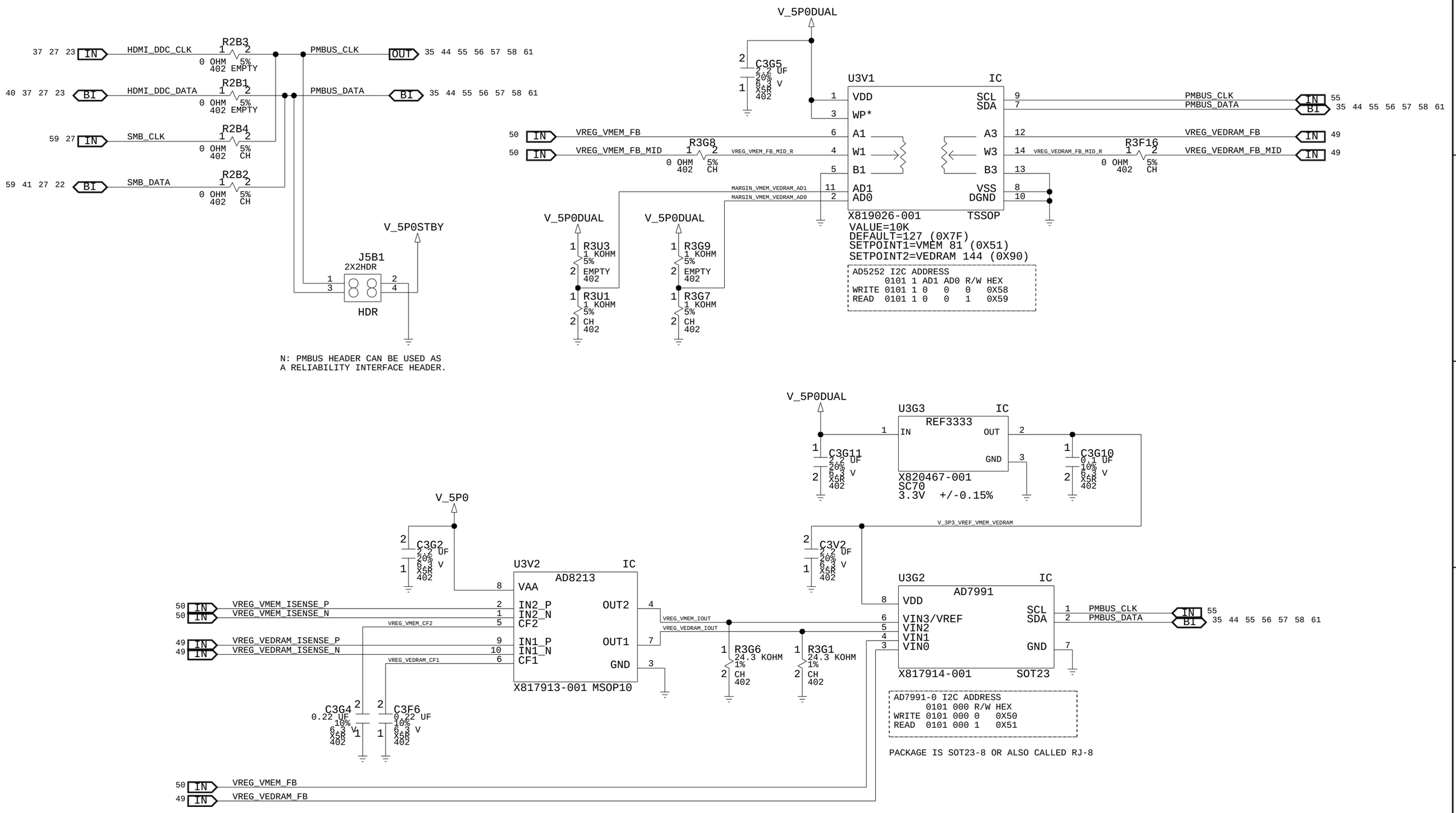
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	54/81	G	1.01

MARGIN, VMEM + VEDRAM



[PAGE_TITLE=MARGIN, VMEM + VEDRAM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	55/81	G	1.01

MARGIN, V3P3 + V5P0

47 IN VREG_V5P0_FB
R2U1 35.7 KOHM 1% CH 402
V_P Q2F3 ADR5043 NC3 X819033-001 3.0V 0.1% V_N IC
C2F4 2.2 UF 20% 6.3 V X5R 402
V_5P0DUAL

47 IN VREG_V5P0_FB_MID
R2T5 0 OHM 5% 402 CH
VREG_V5P0_FB_A1
VREG_V5P0_FB_MID_R

U1U1 IC
X819026-001 TSSOP
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=V5P0 69 (0X45)
SETPOINT2=V3P3 123 (0X7B)

1	VDD	SCL	9 PMBUS_CLK
3	WP*	SDA	7 PMBUS_DATA
6	A1	A3	12 VREG_V3P3_FB_A3
4	W1	W3	14 VREG_V3P3_FB_MID_R
5	B1	B3	13
11	AD1	VSS	8
2	AD0	DGND	10

IN 55 PMBUS_CLK
B1 35 44 55 56 57 58 61

V_P Q1F1 NC3 X819034-001 2.048V 0.1% V_N IC ADR5040A
R1U5 22.1 KOHM 1% CH 402
VREG_V3P3_FB IN 48
R1T19 0 OHM 5% 402 CH
VREG_V3P3_FB_MID IN 48

MARGIN_V3P3_V5P0_AD1
MARGIN_V3P3_V5P0_AD0

V_5P0DUAL
R1U4 1 KOHM 5% EMPTY 402
R1U3 1 KOHM 5% CH 402
V_5P0DUAL
R2F3 1 KOHM 5% CH 402
R2F2 1 KOHM 5% EMPTY 402

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W HEX
WRITE 0101 1 0 1 0 0X5A
READ 0101 1 0 1 1 0X5B

V_5P0DUAL
U1F3 IC
REF3333
X820467-001
SC70
3.3V +/-0.15%
C1F10 2.2 UF 20% 6.3 V X5R 402
C1F11 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_V5P0_V3P3

V_5P0
C1U2 2.2 UF 20% 6.3 V X5R 402
U2U1 IC
AD8213
X817913-001 MSOP10

8	VAA		
2	IN2_P	OUT2	4
1	IN2_N		
5	CF2		
9	IN1_P	OUT1	7
10	IN1_N		
6	CF1	GND	3

47 IN VREG_V5P0_ISENSE_P
47 IN VREG_V5P0_ISENSE_N
48 IN VREG_V3P3_ISENSE_P
48 IN VREG_V3P3_ISENSE_N
VREG_V5P0_CF2
VREG_V3P3_CF1
C2F6 0.22 UF 10% 6.3 V X5R 402
C1F2 0.22 UF 10% 6.3 V X5R 402
VREG_V5P0_IOUT
VREG_V3P3_IOUT
R2F5 24.3 KOHM 1% CH 402
R2F8 24.3 KOHM 1% CH 402

U1F2 IC
AD7991
X818998-001 SOT23

8	VDD	SCL	1 PMBUS_CLK
6	VIN3/VREF	SDA	2 PMBUS_DATA
5	VIN2		
4	VIN1		
3	VIN0	GND	7

AD7991-1 I2C ADDRESS
0101 001 R/W HEX
WRITE 0101 001 0 0X52
READ 0101 001 1 0X53

PACKAGE IS SOT23-8 OR ALSO CALLED RJ-8

V_5P0
R2F4 150 OHM 1% 402 CH
VREG_V5P0_FB_R
V_3P3
R1F4 150 OHM 1% 402 CH
VREG_V3P3_FB_R
R1F6 221 OHM 1% CH 402
R1F5 221 OHM 1% CH 402

[PAGE_TITLE=MARGIN, V3P3 + VP50]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	56/81	G	1.01

MARGIN, VREFS + VCS

V_5P0STBY
U5B6 IC
REF3333
IN OUT GND
X820467-001
SC70
3.3V +/-0.15%
C5N8 2.2 UF 20% 6.3 V X5R 402
C5N7 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_VCS
C4N4 2.2 UF 20% 6.3 V X5R 402

U4B2 IC
AD7992
VDD SCL SDA VIN2/REFIN VIN1 AS CONVST_N* ALERT/BUSY AGND2 AGND1
X814249-001 MSOP10
PMBUS_CLK
PMBUS_DATA
57 IN MEM_VREFS
R4N8 1 KOHM 5% CH 402
R4N13 1 KOHM 5% EMPTY 402
R4N14 1 KOHM 5% CH 402
R4N10 1 KOHM 5% CH 402
MARGIN_VREFS_AS
MARGIN_VREFS_CONVST

AD7992-1 I2C ADDRESS
AS=GND 0100011 R/W
WRITE 0100011 0 0X46
READ 0100011 1 0X47
AS=VDD 0100100 R/W HEX

57 51 IN VREG_VCS_FB
V_5P0
C5B15 2.2 UF 20% 6.3 V X5R 402
C5B5 2.2 UF 20% 6.3 V X5R 402

U5B2 IC
AD8213
VAA IN2_P IN2_N CF2 IN1_P IN1_N CF1 OUT2 OUT1 GND
X817913-001 MSOP10
VREG_VCS_CF2
VREG_VCS_CF1
VREG_VCS_IOUT2
VREG_VCS_IOUT
VREG_VCS_IN
51 IN VREG_VCS_ISENSE_P
51 IN VREG_VCS_ISENSE_N
C4B1 0.22 UF 10% 6.3 V X5R 402
C5B8 0.22 UF 10% 6.3 V X5R 402
R4B1 1 KOHM 5% CH 402
R4B2 24.3 KOHM 1% CH 402
R5N2 24.3 KOHM 1% CH 402

U5N1 IC
AD7992
VDD SCL SDA VIN2/REFIN VIN1 AS CONVST_N* ALERT/BUSY AGND2 AGND1
X814249-001 MSOP10
PMBUS_CLK
PMBUS_DATA
R4B3 1 KOHM 5% CH 402
R4N1 1 KOHM 5% EMPTY 402
R5B6 1 KOHM 5% CH 402
MARGIN_VCS_AS
MARGIN_VCS_CONVST

AD7992-1 I2C ADDRESS
AS=VDD 0100100 R/W HEX
WRITE 0100100 0 0X48
READ 0100100 1 0X49
AS=GND 0100011 R/W

V_5P0STBY
V_MEM
C4N1 2.2 UF 20% 6.3 V X5R 402

U4B1 IC
VDD WP* A1 W1 B1 AD1 AD0 SCL SDA A3 W3 B3 VSS DGND
X819026-001 TSSOP
PMBUS_CLK
PMBUS_DATA
57 OUT MEM_VREFS
R4N5 0 OHM 5% 402 CH MEM_VREFS_R
VREG_VCS_FB
R4B18 0 OHM 5% 402 CH VREG_VCS_FB_MID_R
VREG_VCS_FB_MID
MARGIN_VREFS_AD1
MARGIN_VREFS_AD0
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=VREFS 63 (0X3F)
SETPOINT2=VCS 140 (0X8C)

V_5P0STBY R4N2 1 KOHM 5% CH 402
R4N3 1 KOHM 5% EMPTY 402
V_5P0STBY R4N7 1 KOHM 5% CH 402
R4N6 1 KOHM 5% EMPTY 402
V_MEM R4N4 100 OHM 5% CH 402
MARGIN_VMEM_VREFS_BOT

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W
WRITE 0101 1 1 1 0 0X5E
READ 0101 1 1 1 1 0X5F

Q4B1 ADR510 X821158-001 1.0V 0.35% IC
V_P NC V_N

[PAGE_TITLE=MARGIN, VREFS + VCS]

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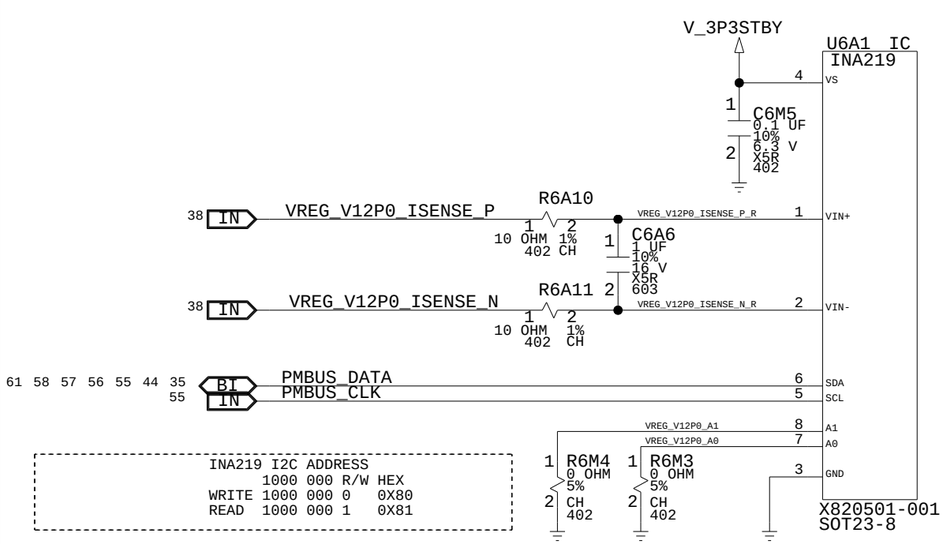
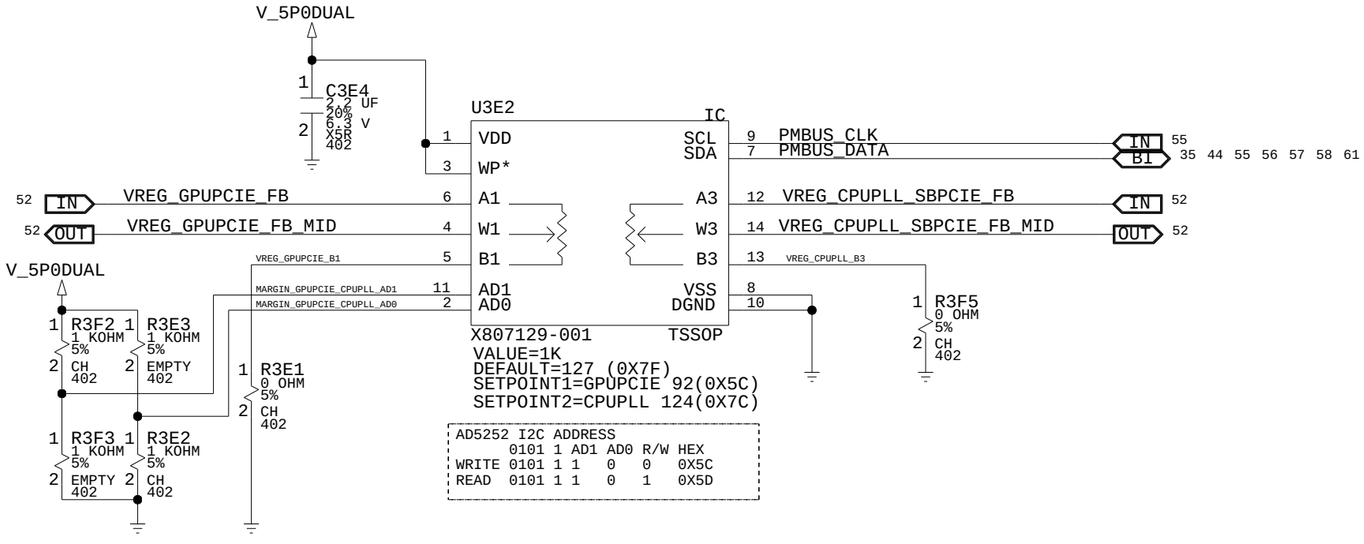
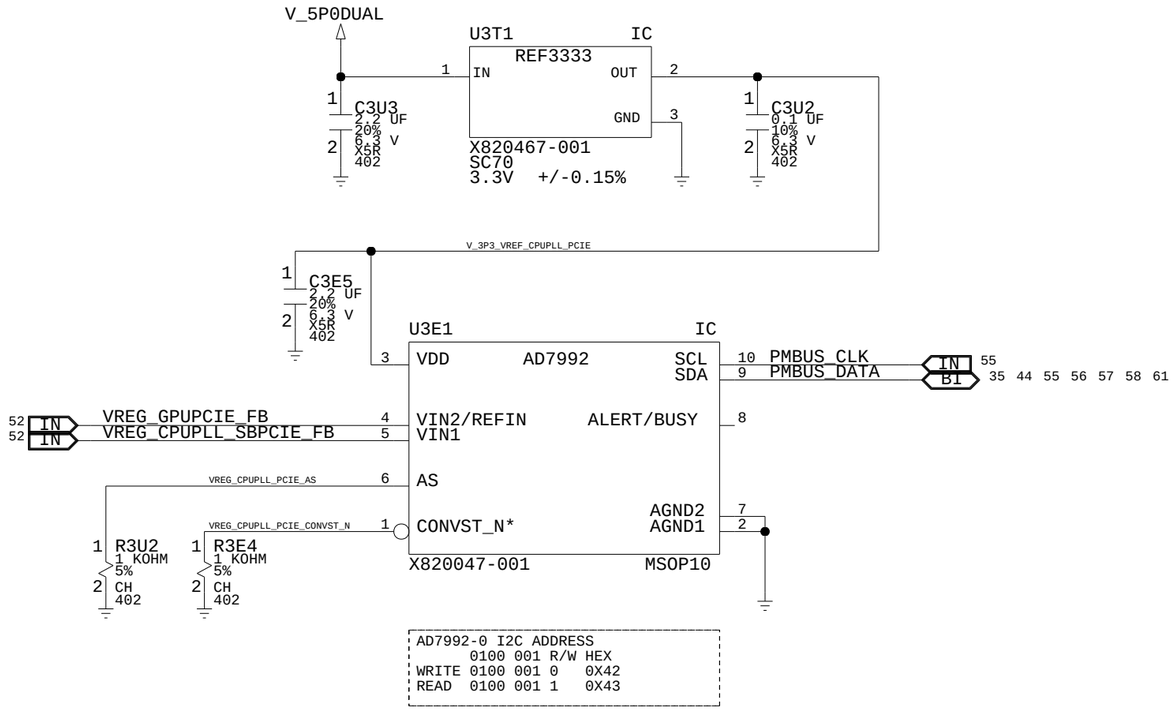
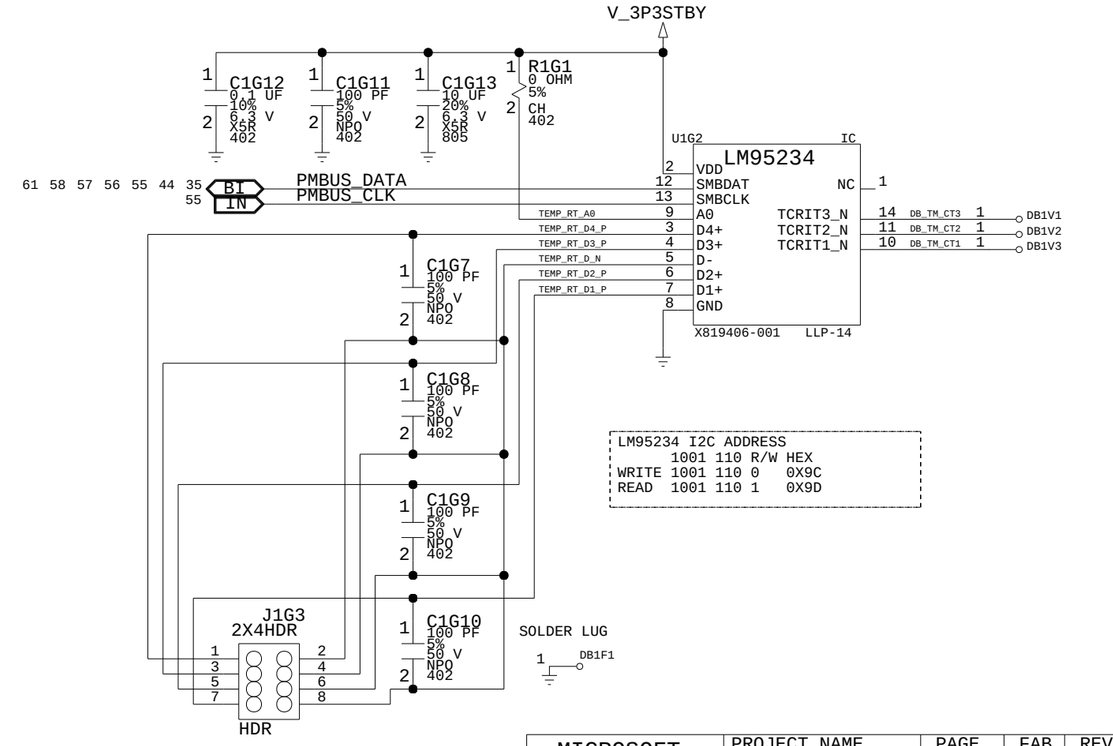
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	57/81	G	1.01

MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP







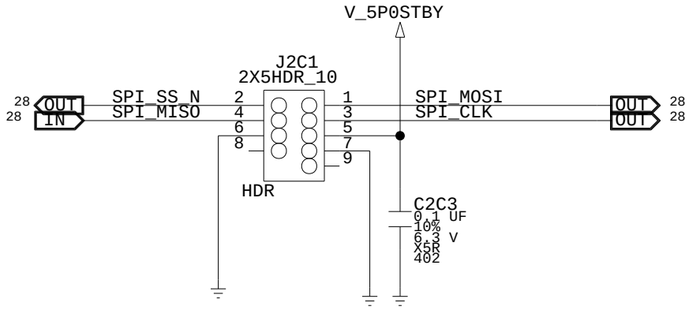


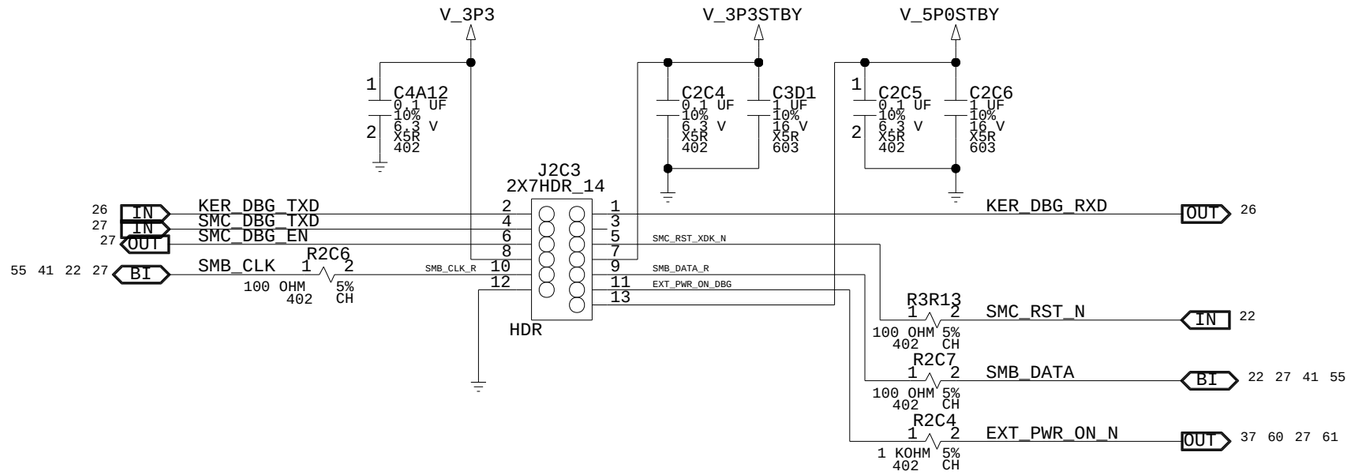
[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

DRAWING
Wed Feb 10 16:23:34 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	58/81	G	1.01

XDK, DEBUG CONNECTORS





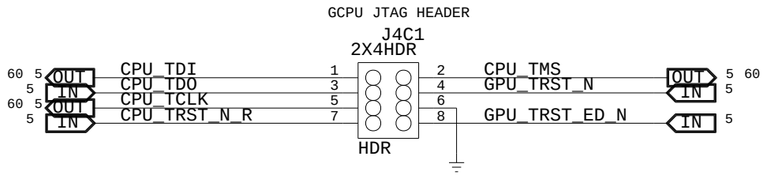
[PAGE_TITLE=XDK. DEBUG CONN]

DRAWING
Wed Feb 10 16:23:35 2010

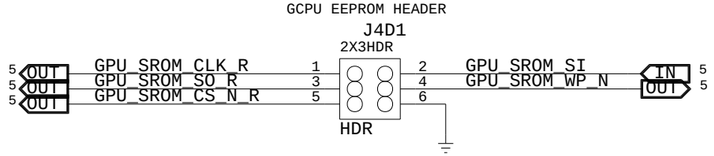
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	59/81	G	1.01

XDK DEBUG

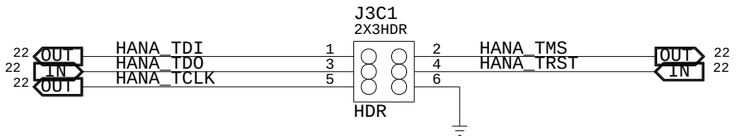
GCPU JTAG HEADER



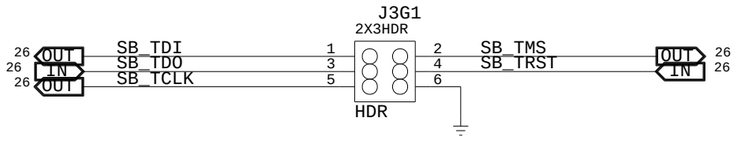
GCPU EEPROM HEADER

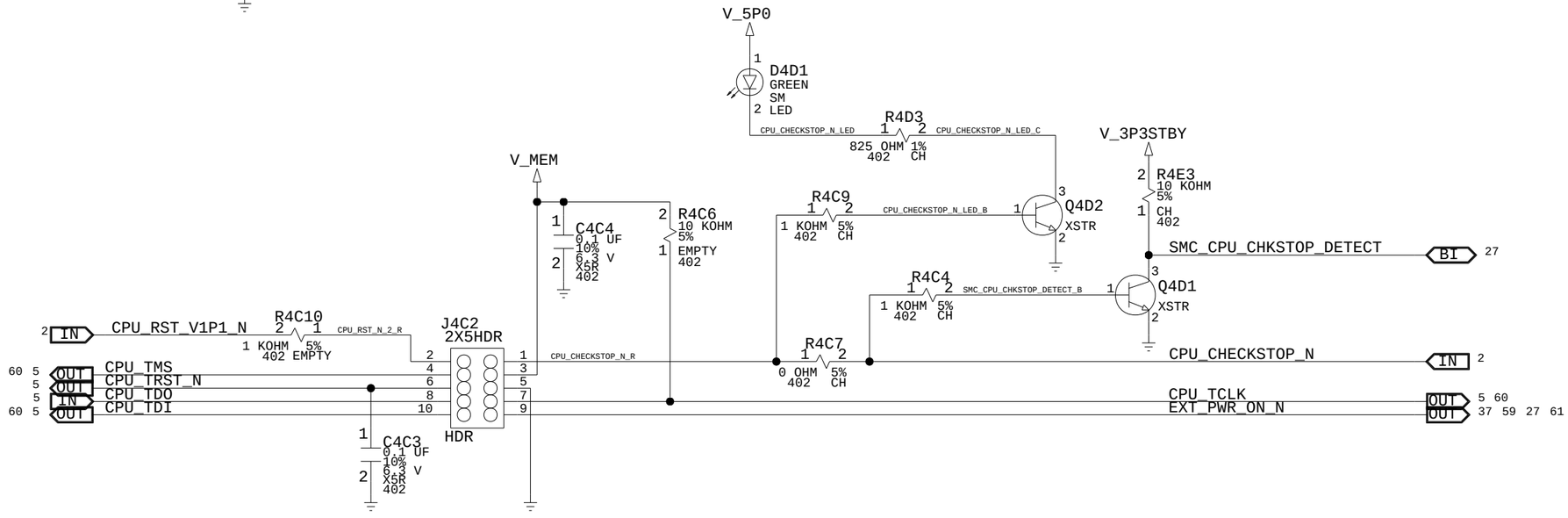


HANA JTAG HEADER



SB JTAG HEADER





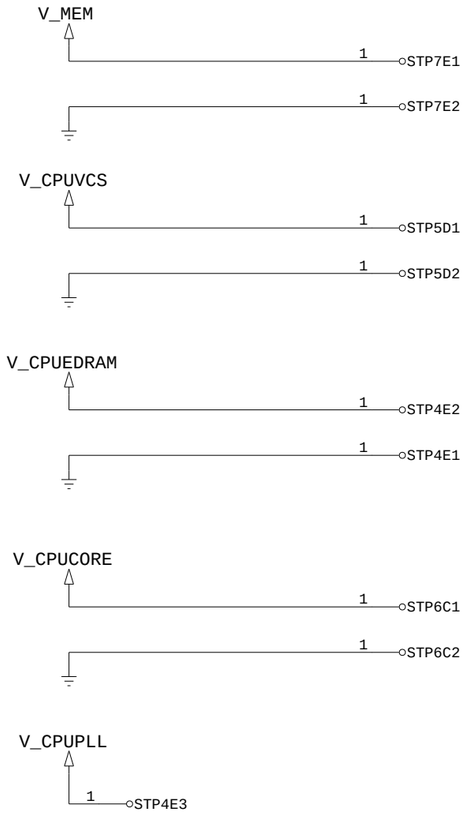
[PAGE_TITLE=XDK, DEBUG TITAN]

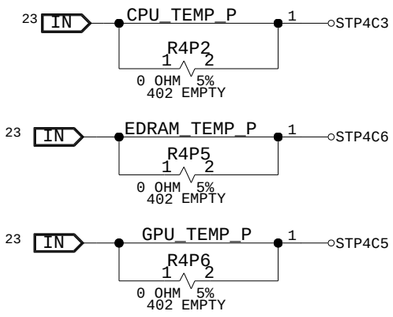
DRAWING
Wed Feb 10 16:23:35 2010

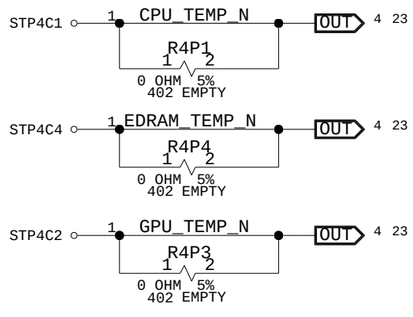
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	60/81	G	1.01

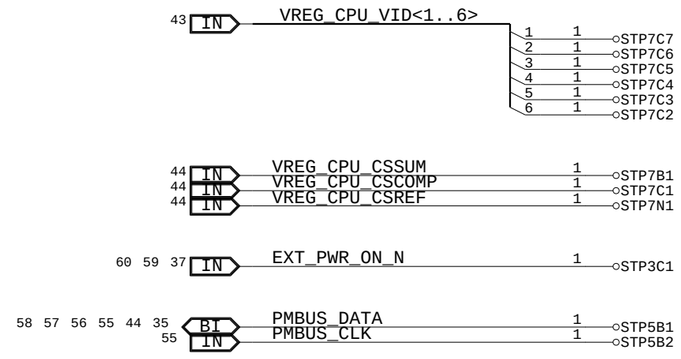
DEBUG BOARD, SPYDER CONN

ALL STP POINTS SHALL BE ADDED TO TOP SIDE IN LAYOUT









[PAGE_TITLE=DEBUG BOARD, SPYDER CONN]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	61/81	G	1.01

LABELS AND MOUNTING

INTELLIGENT SERIAL NUMBER TARGET.

LB2B1
LABEL
1
1375X250_TARGET
X801181-001

WEST PCB MOUNTING HOLES

EDGE
MTG1B1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG1G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG4G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EAST PCB MOUNTING HOLES

EDGE
MTG7G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

HEAT SINK MOUNTING HOLES

STD
MTG4F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG4D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

[PAGE_TITLE=LABELS AND MOUNTING]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	62/81	G	1.01

+12V
I=14.6A
P=175W

L1
0.4W
450nH/8A
lin_max
5.8A
0.4W
2x470uF
/16V
Poly
10mOhm
4x4.7u
F1x1uF
MLCC

2.9A
1.62W
DPAK
1.38W
DPAK
1.15W
420nH/dual
Isat 40A
250KHz/ph
L2
1.38W
DPAK
V_CPUCORE
0.9V-1.2V
43W TD/48A TD
51.6W Max/57A Max
54A TD
Min load 20%
η=82%
0.12W
6x820u
F/2.5V
Poly
7mOhm

2.9A
1.62W
DPAK
1.15W
L2
1.38W
DPAK
1.38W
DPAK

+5POSTBY
I=0.9A
P=4.5W

0.09W
2.2uH
Iin_max 0.91A
3x10uF/
6.3V
MLCC
8mOhm
1x0.1uF/
16V
MLCC
xmOhm

6.2Ohm/
0.28W
each
V_1P8
Linear
DPAK
1.2W MAX
V_1P8
0.6A TD
1.1W TD
DUAL SO8
?W
V_5P0DUAL
1.5A TD
8.4W Max
V_EFUSE
0.02A TD
0.03W TD
V_EFUSE(1.
5V)
Linear
SOT23
0.08W Max

0.45A
SOT23-5
0.24W
V_1P8STBY
1.44W TD/0.8A TD
1.6W Max/0.9A Max
0.1W
2.2uH/
1.7MHz
Isat 1.3A
1x10uF/
6.3V
MLCC
8mOhm

0.5A
SOT23-5
0.4W
V_3P3STBY
1.65W TD/0.5A TD
1.82W Max/0.55A
Max
0.08W
2.2uH/
1.7MHz
Isat 0.9A
1x10uF/
6.3V
MLCC
8mOhm

L1
0.12W
450nH/8A
Iin_max
3.4A
3x4.7uF/
6.3V
MLCC
11mOhm
2x1uF/
6.3V
MLCC
0.5W
DPAK
1.21W*
(0.81W)
DPAK
L3
1.4W
1.7uH/
400KHz
Ipk 12.4A
820uF/
2.5V
Poly
7mOhm
V_VCS
1.25-1.3V
12W TD/9.6A TD
13.2W Max/10.6A Max
η=82%
V_3P3
3.3V
2.75A TD
9.1W TD
10W Max
Min load
50%
η=88%

0 ohm
V_MEMP
ORT
0.5A TD
1.65W TD
FB
V_CPUPLL
0.45A TD
0.83W TD
V_1P83PLL
Linear DPAK
1.01W
Max(loss)
V_SBPCIE
0.2A TD
0.36W TD
V_GPUPCIE
0.11A TD
0.165W TD
V_GPUPCIE(VT
T)(1.5V)
Linear SOT223
0.22W Max(loss)

V_5P0
5.09V,
43.3W TD/ 8.5A TD
47.6W Max/ 9.4A
Max
Min load 50%
η=93%
0.91A
DUAL SO8
1W
0.13W
2.3uH/
600KHz
Isat 5.6A
L4
4x4.7u
F/6.5V
MLCC
8mohm

L1
0.26W
450nH/8A
lin_max
5.51A
0.18W
1x470uF
/16V
Poly
10mohm
4.6A
1.4W
DPAK
1.4W
1.6uH
600KHz
Ipk 13A
L3
1x4.7uF
1x0.1uF
MLCC
1.3W*
(1.05W)
DPAK
0.25W
820uF/
6.3V
E-Al
11mOhm

1.9A
V_EDRAM
1.075V
9.7W TD/9A TD
10.6W Max/9.9A Max
Min load 50%
η=88%
1W
DPAK
1.2W
1.7uH/
600KHz
Isat 11A
1.2W
1.7uH/
600KHz
Isat 11.5A
V_MEM
1.8V
16W TD/9A
17.8W Max/10A max
Min load 50%
η=84%

L1
0.16W
450nH/8A
lin_max
3.1A
1.25A
0.98W
DPAK
1.5W*
(1W)
DPAK
L3
4x4.7uF
1x1uF
MLCC
2x820u
F/2.5V
Poly
7mohm
Option
1x820u
F/2.5V
Poly
7mohm
1.4W*
(1W)
DPAK
L3
1x820u
F/2.5V
Poly
7mohm
Option
2x330uF
OsCon
7mOhm
Option
8x10uF
MLCC
11mOhm
0.19W
1x470uF
/16V
Poly
10mohm
1x330uF
/16V
Poly
10mohm

0.91W*
*=usin
g same
FET
like HS

MICROSOFT CONFIDENTIAL
VEJLE TRINITY XDK MB POWER ARCHITECTURE
MAX PWR4 DISSIPATION(+10% LOAD)
AUG 12, 2009

Legend
- Power rail from Switching Regulator
- Power rail from External PSU
- Power rail from Linear Regulator

Expected
Airflow=0.3m/s

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TRINITY_XDK	63/81	1.01

CLOCK DIAGRAM

WAVE CONN

USB TRIPPLE CONN

RJ45 AUX CONN

HDMI CONN

AVIP CONN

TOSLINK CONN

POWER CONN

ENET PHY

I2S_MCLK (12.288MHZ)

I2S_BCLK (3.072MHZ)

AUDIO DAC

XTAL

27 MHZ

FAN CONN

ODD PWR CONN

HDD PWR CONN

HDD SATA CONN

ODD SATA CONN

STANDBY SWITCHERS VR

VCS VR

CPU VR

ENET_CLK (25MHZ)

STBY_CLK (48MHZ)

SATA_CLK_REF (25MHZ)

SATA_CLK_DP/DN (100MHZ)

PCIEX_CLK_DP/DN (100MHZ)

AUD_CLK (24.576MHZ)

HANA

CPU_CLK_DP/DN (100MHZ)

GPU_CLK_DP/DN (100MHZ)

PIX_CLK_OUT_DP/DN (100MHZ)

V5P0 DUAL VR

V1P8 VR

GCPU

MA_CLK1_DP/DN (800MHZ)

MA_CLK0_DP/DN (800MHZ)

MEM A & B CLAM

MB_CLK1_DP/DN (800MHZ)

MB_CLK0_DP/DN (800MHZ)

FLASH

PSB

V5P0 V3P3 VR

VEFUSE VR

VGPUPCIE VR

VSBPCIE VR

MC_CLK1_DP/DN (800MHZ)

MC_CLK0_DP/DN (800MHZ)

MD_CLK1_DP/DN (800MHZ)

MD_CLK0_DP/DN (800MHZ)

VEDRAM VMEM VR

MEM C & D CLAM

TILT

PWR BUTTON

EJECT BUTTON

BORON FPM

IR

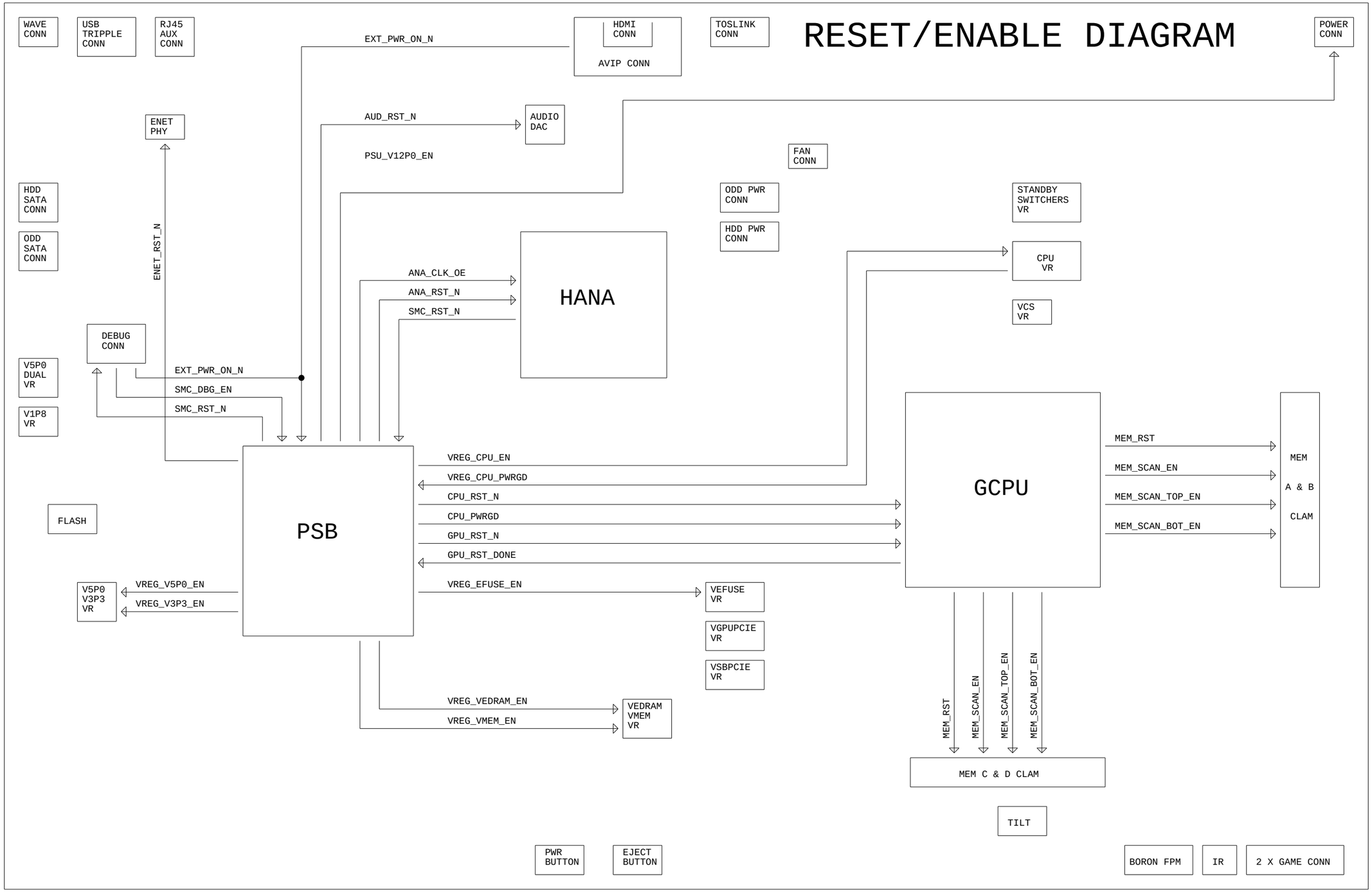
2 X GAME CONN

<PAGE_TITLE=CLOCK DIAGRAM>

DRAWING
TRINITY_FAB_A
Wed Feb 10 16:23:35 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TRINITY_XDK	64/81	1.01

RESET/ENABLE DIAGRAM



<PAGE_TITLE=CLOCK DIAGRAM>

DRAWING
TRINITY_FAB_A
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TRINITY_XDK	65/81	1.01

REFERENCE TABLE

N: MICREL STUFFED BY DEFAULT

REF DES TO STUFF MICREL	ATHEROS
C2C8	C2C8
C2C9	C2C9
C2D1	C2C10
C2D3	C2D2
C2P2	C2D3
C2P3	C2D4
C2P4	C2D5
C2P5	C2P2
C2R5	C2P4
C2R6	C2P5
FB2C1	C2R3
R2D1	FB2C1
R2D2	FB2R1
R2D3	R2D2
R2D4	R2D4
R2D6	R2R1
R2R10	R2R10
R2R2	R2R11
R2R4	R2R12
R2R8	R2R13
U2D1	R2R15
	R2R3
	R2R5
	R2R6
	R2R7
	R2R9
	U2D1

N: FOR MICREL U2D1 IS P/N X819763-001
N: FOR ATHEROS U2D1 IS P/N X820024-001

DIGITAL POTENTIOMETERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESSES
VMEM	256	0.007031V	W: 01011000 0X58, R: 01011001 0X59
VEDRAM	256	0.004199V	W: 01011000 0X58, R: 01011001 0X59
V5P0	256	0.011719V	W: 01011010 0X5A, R: 01011011 0X5B
V3P3	256	0.008V	W: 01011010 0X5A, R: 01011011 0X5B
VREF	256	0.007031V	W: 01011110 0X5E, R: 01011111 0X5F
VCS	256	?V	W: 01011110 0X5E, R: 01011111 0X5F
GPUPCIE	256	0.005859V	W: 01011100 0X5C, R: 01011101 0X5D
CPUPLL_SBPCIE	256	0.007148V	W: 01011100 0X5C, R: 01011101 0X5D

ANALOG TO DIGITAL CONVERTERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESSES
VMEM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
VEDRAM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
V5P0	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
V3P3	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
VCS	4096	0.000806V	W: 01001000 0X48, R: 01001001 0X49
MEM_VREF	4096	0.000806V	W: 01000110 0X46, R: 01000111 0X47
GPUPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
CPUPLL_SBPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43

[PAGE_TITLE=REFERENCE TABLES]

DRAWING
Wed Feb 10 16:23:35 2010

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	66/81	G	1.01

TRINITY DOC TRACKER

DOC #	DESCRIPTION
H08752	TRINITY CONSOLE MONITORING AND MARGINING
H08772	TRINITY CONSOLE FAN DRIVER / THERMAL ALGORITHM
H09297	TRINITY HS PWM FAN SPECIFICATION
H07617	TRINITY VEJLE THERMAL DESIGN AND QUAL SPECIFICATION
H05204	TRINITY PCB TECHNOLOGY SPECIFICATION
H08753	TRINITY CONSOLE HDD SPECIFICATION
H08938	ODD COMP SPEC
H08939	ODD ATA INTERFACE SPEC
H02235	ODD AP MEDIA SPECIFICATION
H08771	TRINITY CONSOLE TEST HOOK SPECIFICATION
	DFM GUIDELINES
H08756	TRINITY CONSOLE USB SPECIFICATION
H08762	TRINITY CONSOLE V_5P0 REGULATOR SPECIFICATION
	TRINITY CONSOLE V_5P0DUAL SPECIFICATION
	TRINITY CONSOLE BLEEDER SPECIFICATION
H08759	TRINITY CONSOLE V_CPUVCS REGULATOR SPECIFICATION
H08760	TRINITY CONSOLE V_3P3STBY REGULATOR SPECIFICATION
H08761	TRINITY CONSOLE V_1P8STBY REGULATOR SPECIFICATION
H08763	TRINITY CONSOLE V_3P3 REGULATOR SPECIFICATION
H08764	TRINITY CONSOLE V_MEM REGULATOR SPECIFICATION
H08765	TRINITY CONSOLE V_EDRAM REGULATOR SPECIFICATION
H08766	TRINITY CONSOLE LINEAR REGULATOR SPECIFICATION
H08767	TRINITY CONSOLE VR ARCHITECTURE
H08758	TRINITY CONSOLE V_CPUCORE REGULATOR SPECIFICATION
	SMC POR FLOWCHART
H08768	TRINITY CONSOLE SYSTEM MANAGEMENT SPECIFICATION
H08773	TRINITY CONSOLE DVD EJECT CAPACITIVE TOUCH SPECIFICATION
H09553	TRINITY CONSOLE WIFI MODULE SPECIFICATION
H08777	TRINITY CONSOLE SPECIFICATION TEMPLATE
H08776	TRINITY CONSOLE FPM REQUIREMENTS DOCUMENT
H08754	TRINITY CONSOLE AUDIO / VIDEO SPECIFICATION
H08757	TRINITY CONSOLE IR SPECIFICATION
H08770	TRINITY CONSOLE TILT SWITCH SPECIFICATION
H08775	TRINITY CONSOLE FPM LED DISPLAY SPECIFICATION
H08774	TRINITY CONSOLE EMI/ESD/SAFETY SPECIFICATION
H08676	CONSOLE USAGE MODEL AND RELIABILITY BUDGET
H08750	TRINITY CONSOLE PLATFORM DESIGN GUIDE
H08778	TRINITY CONSOLE POWER BUDGET
H08780	TRINITY CONSOLE ACOUSTICS MODEL
H09169	TRINITY RJ45 + AUX INTERFACE AND CONNECTOR SPEC
	CONSOLE RELIABILITY SPECIFICATION
H08751	TRINITY CONSOLE FLASH SPECIFICATION
H08769	TRINITY CONSOLE PLL SPECIFICATION
H08755	TRINITY CONSOLE ETHERNET SPECIFICATION
H08945	TRINITY DC CABLE AND CONNECTOR SPEC H08945
H08946	TRINITY PSU SPECS H08946

[PAGE_TITLE=DOC TRACKER]

Title: Basenet Report
Design: trinity
Date: Feb 10 16:21:00 2010

Base nets and synonyms for trinity_lib.TRINITY(@trinity_lib.trinity(sch_1))
Base Signal
Location([Zone][dir])

ACCELEROMETER_INT	35C4
ANA_CLK_OE	27D1 22C8
ANA_CLK_OE_R	22C6
ANA_RST_N	27D1 22D7
ANA_V12P0_PWRGD	22D3 27D1 42B8
ANA_VID_INT	23D1 26B2
AUD_CLK	22A1 29C7
AUD_CLK_R	22B4
AUD_L_OUT	33C1 37C7
AUD_RDY_BSBY	26A2 35A3
AUD_RST_N	26B2 33B7
AUD_R_OUT	33B1 37C7
AUD_SPI_CLK	26A6 35A7
AUD_SPI_MISO	35A3 26A6
AUD_SPI_MOSI	26A4 35A7
AUD_SSB	26A1 35A7
AUD_VOUTL	33B4
AUD_VOUTL_R	33B3
AUD_VOUTR	33B4
AUD_VOUTR_R	33B3
AV_MODE0	37C3 27B8 37B3
AV_MODE0_R	27B6
AV_MODE1	37C3 27B8 37C3
AV_MODE1_R	27B6
AV_MODE2	37C3 27B8 37C3
AV_MODE2_R	27B6
BINDSW_N	38A8 27C1
BINDSW_N_R	38A6
BLEEDER_B	42B2
BLEEDER_C1	42B2
BLEEDER_C2	42B2
BLEEDER_V12P0_B1	42B7
BLEEDER_V12P0_B2	42C5
BLEEDER_V12P0_C1	42B6
BLEEDER_V12P0_C2	42B6
BLEEDER_V12P0_LOAD	42B5
BMA_PS_R	35C5
BND_GAP_CAP	23A5
BORONFPMPORT_DN	28C2 38B8
BORONFPMPORT_DP	28C2 38B8
BORONFPM_CLK	27A1 38A8
BORONFPM_DATA	27A1 38A8
BRD_TEMP_N	23C2 38A8 23A8
BRD_TEMP_N_R	38A6
BRD_TEMP_P	23A1 23C2 38A8
BRD_TEMP_P_R	38A6
CAL_TEMP_N	23A1 23A8
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CAPY	35C4
CAPZ	35C4
CORE_HF_BGR_PLL	2A1
CPU_CHECKSTOP_N	2D1 60A2
CPU_CHECKSTOP_N_LED	60B5
CPU_CHECKSTOP_N_LED_B	60A4
CPU_CHECKSTOP_N_LED_C	60B4
CPU_CHECKSTOP_N_R	60A5
CPU_CLK_DN	22D1 2C7
CPU_CLK_DN_R	22C4
CPU_CLK_DN_R2	2C7
CPU_CLK_DP	22D1 2C7
CPU_CLK_DP_R	22C4
CPU_CLK_DP_R2	2C7
CPU_CORE_HF_CLKOUT_DN	6D1
CPU_CORE_HF_CLKOUT_DP	6D1
CPU_DBG0_POST0	3A5
CPU_DBG1_POST1	3A5
CPU_DBG2_POST2	3A5
CPU_DBG3_POST3	3A5
CPU_DBG4_POST4	3A5
CPU_DBG5_POST5	3A5
CPU_DBG6_POST6	3A5
CPU_DBG7_POST7	3A5
CPU_DBG8_RST0	3A5
CPU_DBG9_RST1	3A5
CPU_DBG10_RST2	3A5
CPU_DBG11_GPU_HB_TP	3A5
CPU_DBG12_CPUCLK0_TP	3A5
CPU_DBG13_CPUCLK1_TP	3A5
CPU_DBG14_GPUCLK0_TP	3A5
CPU_DBG15_GPUCLK1_TP	3A5
CPU_DBG_RST_EN	2B7
CPU_DBG_TBCLK0	3D7
CPU_DBG_TBCLK1	3D7
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CPU_DLL_SNIF_OUT_TP	3D5
CPU_EXT_CLK_EN	2B7
CPU_LIMIT_BYPASS	2B1
CPU_PLL_BYPASS	2B1
CPU_PSRO0_OUT	2B7
CPU_PWRGD	27A1 2D7
CPU_RST_N	27B1 2D7
CPU_RST_N_2_R	60A6
CPU_RST_V1P1_N	2D1 60A7
CPU_SRVID	2B1 51B8
CPU_TCLK	5C8 60A2 60D8
CPU_TDI	5C8 60A7 60D8
CPU_TDO	5C8 60A7 60D8
CPU_TEMP_N	4B8 61C3 23A8
CPU_TEMP_P	23A1 4B8 61C6
CPU_TINIT	2A6
CPU_TMS	5C8 60A7 60D6
CPU_TRST_N	5C8 60A7
CPU_TRST_N_R	5C8 60D8
CPU_VDDS0_DN	6D8
CPU_VDDS0_DP	6D8
CPU_VDDS1_DN	6D8
CPU_VDDS1_DP	6D8
CPU_VGATE	2B7
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CPU_VREG_APS2	2C1 43D7
CPU_VREG_APS3	2C1 43D7
CPU_VREG_APS4	2C1 43D7
CPU_VREG_APS5	2C1 43D7
CPU_VREG_APS6	2C1 43D7
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DB_TM_CT2	58B1
DB_TM_CT3	58B1
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EDRAM_TEMP_N	4B8 61B3 23A8
EDRAM_TEMP_P	23A1 4B8 61B6
EJECTSW_N	38A8 27C1 35A3
EJECTSW_N_R	38A6
ENET_1.8VEXT	32C5
ENET_ACT_N	32A3
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ENET_CLK_R	22C4
ENET_LINK_N	32A3
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ENET_REXT	32B5
ENET_RSTN_R	32A5
ENET_RST_N	26B2 32A8 32B8
ENET_RX_DN	32A8 38B8
ENET_RX_DP	32A8 38C8
ENET_RX_TERM	38C7
ENET_TX_DN	32A1 38C8
ENET_TX_DP	32A1 38C8
ENET_TX_TERM	38C7
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EXPPORT_PORT1_DP	28B7 39C4
EXPPORT_PORT2_DN	28B7 39B4
EXPPORT_PORT2_DP	28B7 39B4
EXPPORT_PORT3_DN	28A7 39A4
EXPPORT_PORT3_DP	28B7 39A4
EXPPORT_RJ45_DN	28B7 38C5
EXPPORT_RJ45_DP	28B7 38C5
EXT_PWR_ON_DBG	59C3
EXT_PWR_ON_N	37D3 59C1 60A2 27C8 37C3 61B2
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FAN1_FDBK_R	36B6
FAN1_OUT	23A2 36C6
FAN1_Q1_C	36C5
FAN1_Q1_E	36C5
FAN_OP1_DP	23A7
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FLSH_ALE	28C2 34B5
FLSH_CE_N	28C2 34B5
FLSH_CLE	28C2 34B5
FLSH_DATA<7..0>	28C7 34C8
FLSH_NC38	34C2
FLSH_READY	34C1 28B7
FLSH_RE_N	28C2 34B5
FLSH_WE_N	28C2 34B5
FLSH_WP_N	28C7 34B5
GAMEPORT1_DN	28B2 39D8
GAMEPORT1_DP	28B2 39D8
GAMEPORT2_DN	28B2 39C8
GAMEPORT2_DP	28B2 39C8
GND_DECOUPLE	32A5
GPU_CLK_DN	22D1 4D8
GPU_CLK_DN_C	4C8
GPU_CLK_DN_R	22C4
GPU_CLK_DN_R2	4D6
GPU_CLK_DP	22D1 4D8
GPU_CLK_DP_C	4D8
GPU_CLK_DP_R	22C4
GPU_CLK_DP_R2	4D6
GPU_DBG_RST_EN	2B7
GPU_HSYNC_OUT	4B1 23C8
GPU_PIX_CLK_1X	4C2 23D8
GPU_RST_DONE	4D2 27C1
GPU_RST_DONE_R	27C4
GPU_RST_N	27A1 4C8
GPU_SROM_CLK_R	60C8 5B1
GPU_SROM_CS	5C4
GPU_SROM_CS_N_R	60C8 5B1
GPU_SROM_EN	5C4
GPU_SROM_SCLK	5C4
GPU_SROM_SI	5B1 60C6
GPU_SROM_SO	5C4
GPU_SROM_SO_R	60C8 5B1
GPU_SROM_WP_N	60C6 5B1
GPU_TEMP_N	4B8 61B3 23A8
GPU_TEMP_P	23A1 4C8 61B6
GPU_TRST_ED_N	5B8 60D6
GPU_TRST_N	5B8 60D6
GPU_VSYNC_OUT	4B1 23C8
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HANA_CLK_DRV_RSET1	22C6
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HANA_DAC_RSET	23C6
HANA_OP2_DN	23A2 23B6
HANA_OP2_DP	23B6
HANA_OP2_OUT	23A4
HANA_PIX_CLK_2X_DN	22B1 4C8
HANA_PIX_CLK_2X_DN_R	22C4
HANA_PIX_CLK_2X_DP	22B1 4C8
HANA_PIX_CLK_2X_DP_R	22C4
HANA_POR_BYPASS	22D6
HANA_SPDIF_OUT	23A2 37D8 39A8

HANA_TCLK	60C8 22B8
HANA_TDI	60C8 22B8
HANA_TDO	22B8 60C8
HANA_TMS	60C6 22B8
HANA_TRST	22B8 60C6
HANA_V_12P0_DET	22D6
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HANA_XTAL_BYPASS	22C6
HANA_XTAL_IN	22C6
HANA_XTAL_OUT	22C6
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HBEDB_CLK_SEL	26D6
HDD_RX_DN	41C8 29B7
HDD_RX_DN_C	41C6
HDD_RX_DP	41C8 29B7
HDD_RX_DP_C	41C6
HDD_TX_DN	29A1 41D8
HDD_TX_DN_C	41D6
HDD_TX_DP	29A1 41D8
HDD_TX_DP_C	41D6
HDMI_CEC	40B3
HDMI_DDC_CLK	23A2 27B8 37D3 40A8 55D8
HDMI_DDC_DATA	23A2 27C8 37C3 40A8 55D8
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HDMI_HPD	40A1 23C8
HDMI_HPD_PIN	40A3
HDMI_TX0_DN	23A1 40C8
HDMI_TX0_DP	23B1 40C8
HDMI_TX0_DP_R	23B2
HDMI_TX1_DN	23B1 40C8
HDMI_TX1_DP	23B1 40D8
HDMI_TX1_DP_R	23B2
HDMI_TX2_DN	23B1 40D8
HDMI_TX2_DP	23B1 40D8
HDMI_TX2_DP_R	23B2
HDMI_TXC_DN	23B1 40B8
HDMI_TXC_DP	23C1 40B8
HDMI_TXC_DP_R	23C2
I2S_BCLK	29B1 23C8 33B7
I2S_BCLK_R	29B4
I2S_MCLK	29B1 33B7
I2S_MCLK_R	29B4
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I2S_SD1	23B6
I2S_SD2	23B6
I2S_SD3	23B6
I2S_SD_R	29B4
I2S_WS	29B1 23C8 33B7
I2S_WS_R	29B4
IR_DATA	35B5 27A8
KER_DBG_RXD	59C1 26C7
KER_DBG_TXD	26C1 59C5
KER_DBG_TXD_R	26C3
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MARGIN_GPUPCIE_CPUPLL_AD0	58C4
MARGIN_GPUPCIE_CPUPLL_AD1	58C4
MARGIN_V3P3_V5P0_AD0	56C6
MARGIN_V3P3_V5P0_AD1	56C6
MARGIN_VCS_AS	57B5
MARGIN_VCS_CONVST	57B4
MARGIN_VMEM_VEDRAM_AD0	55C4
MARGIN_VMEM_VEDRAM_AD1	55C4
MARGIN_VMEM_VREFS_BOT	57A6
MARGIN_VREFS_AD0	57A6
MARGIN_VREFS_AD1	57A6
MARGIN_VREFS_AS	57D4
MARGIN_VREFS_CONVST	57C4
MA_A<11..0>	12C5 14C8 15C8
MA_BA<2..0>	12C5 14C8 15C8
MA_CAS_N	12B5 14B8 15B8
MA_CKE	12B5 14B8 15B8
MA_CLK0_DN	12C5 14D8
MA_CLK0_DP	12C5 14D8
MA_CLK1_DN	12C5 15D8
MA_CLK1_DP	12C5 15D8
MA_CS0_N	12B5 14B8
MA_CS1_N	12B5 14B8 15B8
MA_DM0	12B8 14B4 15B5
MA_DM1	12C8 14B4 15B5
MA_DM2	12C8 14C4 15C5
MA_DM3	12D8 14C4 15C5
MA_DQ0	12B8 14B4 15B5
MA_DQ1	12B8 14B4 15B5
MA_DQ2	12B8 14B4 15B5
MA_DQ3	12B8 14B4 15B5
MA_DQ4	12B6 12B8 14B4 15B5
MA_DQ5	12B8 14B4 15C5
MA_DQ6	12B8 14B4 15C5
MA_DQ7	12B8 14B4 15C5
MA_DQ8	12C8 14B4 15B5
MA_DQ9	12C8 14B4 15B5
MA_DQ10	12C8 14B4 15B5
MA_DQ11	12C8 14B4 15B5
MA_DQ12	12B6 12C8 14B4 15B5
MA_DQ13	12C8 14B4 15B5
MA_DQ14	12C8 14C4 15B5
MA_DQ15	12C8 14C4 15B5
MA_DQ16	12C8 14C4 15C5
MA_DQ17	12C8 14C4 15C5
MA_DQ18	12C8 14C4 15C5
MA_DQ19	12C8 14C4 15C5
MA_DQ20	12C8 14C4 15D5
MA_DQ21	12C8 14C4 15D5
MA_DQ22	12C8 14C4 15D5
MA_DQ23	12C8 14C4 15D5
MA_DQ24	12D8 14C4 15C5
MA_DQ25	12D8 14C4 15C5
MA_DQ26	12D8 14C4 15C5
MA_DQ27	12D8 14C4 15C5
MA_DQ28	12D8 14C4 15C5
MA_DQ29	12D8 14D4 15C5

MA_DQ30	12D8 14D4 15C5
MA_DQ31	12D8 14D4 15C5
MA_RAS_N	12B5 14B8 15B8
MA_RDQS0	14B4 15B5 12B8
MA_RDQS1	14B4 15B5 12C8
MA_RDQS2	14C4 15C5 12C8
MA_RDQS3	14C4 15C5 12D8
MA_VREF0	12A7
MA_WDQS0	12A6 12B8 14B4 15B5
MA_WDQS1	12B6 12C8 14B4 15B5
MA_WDQS2	12C8 14C4 15C5
MA_WDQS3	12D8 14C4 15C5
MA_WE_N	12B5 14B8 15B8
MA_ZQ_BOT	15B5
MA_ZQ_TOP	14B5
MB_A<11..0>	12C1 16C8 17C8
MB_BA<2..0>	12C1 16B8 17B8
MB_CAS_N	12B1 16B8 17B8
MB_CKE	12B1 16B8 17B8
MB_CLK0_DN	12C1 16C8
MB_CLK0_DP	12C1 16D8
MB_CLK1_DN	12C1 17C8
MB_CLK1_DP	12C1 17D8
MB_CS0_N	12B1 16B8
MB_CS1_N	12B1 16B8 17B8
MB_DM0	12B4 16B5 17B5
MB_DM1	12C4 16B5 17B5
MB_DM2	12C4 16C5 17C5
MB_DM3	12D4 16C5 17C5
MB_DQ0	12B4 16B5 17B5
MB_DQ1	12B4 16B5 17B5
MB_DQ2	12B4 16B5 17B5
MB_DQ3	12B4 16B5 17B5
MB_DQ4	12B2 12B4 16B5 17B5
MB_DQ5	12B4 16B5 17B5
MB_DQ6	12B4 16B5 17B5
MB_DQ7	12B4 16B5 17B5
MB_DQ8	12C4 16B5 17B5
MB_DQ9	12C4 16B5 17B5
MB_DQ10	12C4 16B5 17B5
MB_DQ11	12C4 16B5 17B5
MB_DQ12	12B2 12C4 16B5 17B5
MB_DQ13	12C4 16B5 17B5
MB_DQ14	12C4 16B5 17B5
MB_DQ15	12C4 16B5 17B5
MB_DQ16	12C4 16C5 17C5
MB_DQ17	12C4 16C5 17C5
MB_DQ18	12C4 16C5 17C5
MB_DQ19	12C4 16C5 17C5
MB_DQ20	12C4 16C5 17C5
MB_DQ21	12C4 16C5 17C5
MB_DQ22	12C4 16C5 17C5
MB_DQ23	12C4 16C5 17D5
MB_DQ24	12D4 16C5 17C5
MB_DQ25	12D4 16C5 17C5
MB_DQ26	12D4 16C5 17C5
MB_DQ27	12D4 16C5 17C5

MB_DQ28	12D4 16C5 17C5
MB_DQ29	12D4 16C5 17C5
MB_DQ30	12D4 16C5 17C5
MB_DQ31	12D4 16D5 17C5
MB_RAS_N	12B1 16B8 17B8
MB_RDQS0	16B5 17B5 12B4
MB_RDQS1	16B5 17B5 12C4
MB_RDQS2	16C5 17C5 12C4
MB_RDQS3	16C5 17C5 12D4
MB_VREF0	12A3
MB_WDQS0	12A2 12B4 16B5 17B5
MB_WDQS1	12B2 12C4 16B5 17B5
MB_WDQS2	12C4 16C5 17C5
MB_WDQS3	12D4 16C5 17C5
MB_WE_N	12B1 16B8 17B8
MB_ZQ_BOT	17A5
MB_ZQ_TOP	16A5
MC_A<11..0>	13C5 18C8 19C8
MC_BA<2..0>	13C5 18B8 19B8
MC_CAS_N	13B5 18B8 19B8
MC_CKE	13C5 18B8 19B8
MC_CLK0_DN	13C5 18D8
MC_CLK0_DP	13C5 18D8
MC_CLK1_DN	13C5 19D8
MC_CLK1_DP	13D5 19D8
MC_CS0_N	13B5 18B8
MC_CS1_N	13B5 18B8 19B8
MC_DM0	13B8 18B4 19B4
MC_DM1	13C8 18B4 19B4
MC_DM2	13C8 18C4 19C4
MC_DM3	13D8 18C4 19C4
MC_DQ0	13B8 18B4 19B4
MC_DQ1	13B8 18B4 19B4
MC_DQ2	13B8 18B4 19B4
MC_DQ3	13B8 18B4 19B4
MC_DQ4	13B6 13B8 18B4 19B4
MC_DQ5	13B8 18B4 19B4
MC_DQ6	13B8 18B4 19B4
MC_DQ7	13B8 18B4 19C4
MC_DQ8	13C8 18B4 19B4
MC_DQ9	13C8 18B4 19B4
MC_DQ10	13C8 18B4 19B4
MC_DQ11	13C8 18B4 19B4
MC_DQ12	13B6 13C8 18B4 19B4
MC_DQ13	13C8 18B4 19B4
MC_DQ14	13C8 18C4 19B4
MC_DQ15	13C8 18C4 19B4
MC_DQ16	13C8 18C4 19C4
MC_DQ17	13C8 18C4 19C4
MC_DQ18	13C8 18C4 19C4
MC_DQ19	13C8 18C4 19C4
MC_DQ20	13C8 18C4 19C4
MC_DQ21	13C8 18C4 19C4
MC_DQ22	13C8 18C4 19D4
MC_DQ23	13D8 18C4 19D4
MC_DQ24	13D8 18C4 19C4
MC_DQ25	13D8 18C4 19C4

MC_DQ26	13D8 18C4 19C4
MC_DQ27	13D8 18C4 19C4
MC_DQ28	13D8 18C4 19C4
MC_DQ29	13D8 18D4 19C4
MC_DQ30	13D8 18D4 19C4
MC_DQ31	13D8 18D4 19C4
MC_RAS_N	13B5 18B8 19B8
MC_RDQS0	18B4 19B4 13B8
MC_RDQS1	18B4 19B4 13C8
MC_RDQS2	18C4 19C4 13C8
MC_RDQS3	18C4 19C4 13D8
MC_VREF0	13A7
MC_WDQS0	13B5 13B8 18B4 19B4
MC_WDQS1	13B5 13C8 18B4 19B4
MC_WDQS2	13C8 18C4 19C4
MC_WDQS3	13D8 18C4 19C4
MC_WE_N	13B5 18B8 19B8
MC_ZQ_BOT	19B5
MC_ZQ_TOP	18B5
MD_A<11..0>	13C1 20C8 21C8
MD_BA<2..0>	13C1 20C8 21B8
MD_CAS_N	13B1 20B8 21B8
MD_CKE	13C1 20B8 21B8
MD_CLK0_DN	13C1 20D8
MD_CLK0_DP	13C1 20D8
MD_CLK1_DN	13C1 21D8
MD_CLK1_DP	13D1 21D8
MD_CS0_N	13B1 20B8
MD_CS1_N	13B1 20B8 21B8
MD_DM0	13B4 20B4 21B5
MD_DM1	13C4 20B4 21B5
MD_DM2	13C4 20C4 21C5
MD_DM3	13D4 20C4 21C5
MD_DQ0	13B4 20B4 21B5
MD_DQ1	13B4 20B4 21B5
MD_DQ2	13B4 20B4 21B5
MD_DQ3	13B4 20B4 21B5
MD_DQ4	13B4 20B4 21B5
MD_DQ5	13B4 20B4 21B5
MD_DQ6	13B4 20B4 21C5
MD_DQ7	13B4 20B4 21C5
MD_DQ8	13C4 20B4 21B5
MD_DQ9	13C4 20B4 21B5
MD_DQ10	13C4 20B4 21B5
MD_DQ11	13C4 20B4 21B5
MD_DQ12	13B2 13C4 20C4 21B5
MD_DQ13	13C4 20C4 21B5
MD_DQ14	13C4 20C4 21B5
MD_DQ15	13C4 20C4 21B5
MD_DQ16	13C4 20C4 21C5
MD_DQ17	13C4 20C4 21C5
MD_DQ18	13C4 20C4 21C5
MD_DQ19	13C4 20C4 21C5
MD_DQ20	13C4 20C4 21C5
MD_DQ21	13C4 20C4 21D5
MD_DQ22	13C4 20C4 21D5
MD_DQ23	13D4 20C4 21D5

MD_DQ24	13D4 20C4 21C5
MD_DQ25	13D4 20C4 21C5
MD_DQ26	13D4 20C4 21C5
MD_DQ27	13D4 20D4 21C5
MD_DQ28	13D4 20D4 21C5
MD_DQ29	13D4 20D4 21C5
MD_DQ30	13D4 20D4 21C5
MD_DQ31	13D4 20D4 21C5
MD_RAS_N	13B1 20B8 21B8
MD_RDQS0	20B4 21B5 13B4
MD_RDQS1	20B4 21B5 13C4
MD_RDQS2	20C4 21C5 13C4
MD_RDQS3	20C4 21C5 13D4
MD_VREF0	13A3
MD_WDQS0	13B4 20B4 21B5
MD_WDQS1	13B2 13C4 20B4 21B5
MD_WDQS2	13C4 20C4 21C5
MD_WDQS3	13D4 20C4 21C5
MD_WE_N	13B1 20B8 21B8
MD_ZQ_BOT	21B5
MD_ZQ_TOP	20B5
MEM_A_VREF0	15A6 14B8 15B8
MEM_A_VREF1	14A6 14B8 15B8
MEM_B_VREF0	17A6 16B8 17B8
MEM_B_VREF1	16A6 16B8 17B8
MEM_CALA	4A6
MEM_CALB	4A6
MEM_C_VREF0	19A6 18B8 19B8
MEM_C_VREF1	18A6 18B8 19B8
MEM_D_VREF0	21A6 20B8 21B8
MEM_D_VREF1	20A6 20B8 21B8
MEM_RST	4B1 14D8 15D8 16C8 17C8 18D8 19C8 20D8 21D8
MEM_SCAN_BOT_EN	4A1 15B8 17B8 19B8 21B8
MEM_SCAN_BOT_EN_N	4A4
MEM_SCAN_EN	4A1 14B8 15B8 16B8 17B8 18B8 19B8 20B8 21B8
MEM_SCAN_TOP_EN	4A1 14B8 16B8 18B8 20B8
MEM_VREFS	57A6 57D4
MEM_VREFS_R	57A6
MII_COL	32C1 29C7
MII_CRS	32C1 29C7
MII_MDC_CLK_OUT	29D1 32B8
MII_MDC_CLK_OUT_R	29D4
MII_MDIO	29C8 32B8
MII_RXD0	32A1 29C7
MII_RXD1	32A1 29C7
MII_RXD2	32A1 29C7
MII_RXD3	32B1 29C7
MII_RXDV	32C1 29C7
MII_RXER	32B1 29C7
MII_RX_CLK	32B1 29D7
MII_RX_CLK_R	29D6
MII_TXD0	29C1 32A8
MII_TXD1	29C1 32A8

MII_TXD2	29C1 32A8
MII_TXD3	29C1 32B8
MII_TXEN	29C1 32B8
MII_TX_CLK	32B1 29D7
MII_TX_CLK_R	29D6
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MUPORT_DP	28C2 41B3
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NET_259_I6_VIN1	57D3
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ODD_RX_DN_C	41A7
ODD_RX_DP	41A8 29B7
ODD_RX_DP_C	41A7
ODD_TX_DN	29A1 41A8
ODD_TX_DN_C	41A7
ODD_TX_DP	29A1 41B8
ODD_TX_DP_C	41B7
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PCIEX_CLK_DN_R	22C4
PCIEX_CLK_DP	22C1 26C7
PCIEX_CLK_DP_R	22C4
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PEX_GPU_SB_L0_DN_C	4C4
PEX_GPU_SB_L0_DP	4C2 26C7
PEX_GPU_SB_L0_DP_C	4C4
PEX_GPU_SB_L1_DN	4C2 26C7
PEX_GPU_SB_L1_DN_C	4C4
PEX_GPU_SB_L1_DP	4D2 26C7
PEX_GPU_SB_L1_DP_C	4D4
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PEX_RBIAS1	26C6
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PEX_SB_GPU_L0_DN_C	26C3
PEX_SB_GPU_L0_DP	26D1 4C8
PEX_SB_GPU_L0_DP_C	26D3
PEX_SB_GPU_L1_DN	26D1 4C8
PEX_SB_GPU_L1_DN_C	26D3
PEX_SB_GPU_L1_DP	26D1 4C8
PEX_SB_GPU_L1_DP_C	26D3
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PMBUS_DATA	35C8 44C8 55A2 55D1 55D6 56B1 56D3 57A2 57C2 57D1 58A5 58B4 58C8 58D1 61B2
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PSU_V12P0_EN_R	38A2
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PWRSW_N_R	38A8 35B3
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SATA_CLK_DN_R	22C4
SATA_CLK_DP	22C1 26D7
SATA_CLK_DP_R	22C4
SATA_CLK_REF	22B1 26D7
SATA_CLK_REF_R	22C4
SATA_CLK_SEL	26D6
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SB_GPIO<11>	26A4
SB_GPIO<14>	26A2
SB_GPIO<15>	26A8
SB_GPIO_RESERVED6	26B2 26A8
SB_GPIO_RESERVED16	26B3
SB_GPIO_RESERVED17	26B3
SB_GPIO_RESERVED18	26B3
SB_GPIO_RESERVED19	26B3
SB_GPIO_RESERVED20	26B3
SB_GPIO_RESERVED21	26B3
SB_GPIO_RESERVED22	26B3
SB_GPIO_RESERVED23	26B3
SB_GPIO_RESERVED24	26B3
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SB_GPIO_RESERVED26	26C3
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SB_MAIN_PWRGD_R	27B4
SB_RST_N	27A1 27D8
SB_SPDIF_OUT	29B1 23C8
SB_TCLK	60B8 26A6
SB_TDI	60B8 26A6
SB_TDO	26A6 60B8
SB_TMS	60B6 26A6
SB_TRST	26A6 60B6
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SCART_RGB_R	37B7
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SMB_CLK_MU_R	41B2
SMB_CLK_R	59C4
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SMB_DATA_MU_R	41B2
SMB_DATA_R	59C3
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SMC_CPU_CHKSTOP_DETECT_B	60A4
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SMC_DBG_TXD	27D1 59C5
SMC_DBG_TXD_R	27D4
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SMC_PWM1	27A1 36A6
SMC_PWM1_R	36A3
SMC_RST_N	22D3 27D8 42B3 59C1
SMC_RST_N_R	22D4
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TEMP_RT_D1_P	58B2
TEMP_RT_D2_P	58B2
TEMP_RT_D3_P	58B2
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VID_DACB_DP	23D1 37A8
VID_DACB_OUT	37A6 37D7
VID_DACC_DN	23D4
VID_DACC_DP	23D1 37A6
VID_DACC_OUT	37A3 37D7
VID_DACD_DN	23D4
VID_DACD_DP	23D1 37A6
VID_DACD_OUT	37A3 37C7
VID_HSYNC_OUT	37A1 37C7
VID_HSYNC_OUT_R	23C1 37A3
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VID_VSYNC_OUT_R	23C1 37A3
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VREG_1P8STBY_FB	53C4
VREG_1P8STBY_SW	53C4
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VREG_3P3STBY_FB	53B4
VREG_3P3STBY_SW	53B4
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VREG_CPUPLL_PCIE_CONVST_N	58A7
VREG_CPUPLL_R	52A6
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VREG_CPU_BST1_R	45A5
VREG_CPU_BST2	45D5
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VREG_CPU_COMP	44C4
VREG_CPU_COMP_R	44A6
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VREG_CPU_CSCOMP_R	44B6
VREG_CPU_CSREF	44C8 61B2
VREG_CPU_CSSUM	44C8 61B2
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VREG_CPU_DRVH2	45C5
VREG_CPU_DRVL1	45A5
VREG_CPU_DRVL2	45C5
VREG_CPU_DRV_EN	44C1 45C8
VREG_CPU_EN	27C1 44D8
VREG_CPU_FAULT_N	44C2
VREG_CPU_FB	44A6 44C4
VREG_CPU_FBRTN	44B3 44C4
VREG_CPU_ILIMITFS	44B4
VREG_CPU_IMON	44C2
VREG_CPU_IREF	44C4
VREG_CPU_OD1_N	44C2
VREG_CPU_PHASE1	45A1 44C8
VREG_CPU_PHASE1_R	44C4
VREG_CPU_PHASE2	45C1 44C8
VREG_CPU_PHASE2_R	44C4
VREG_CPU_PWM1	44C1 45A8
VREG_CPU_PWM2	44C1 45C8
VREG_CPU_RAMPADJ	44D4
VREG_CPU_RAMPADJ_R	44D5
VREG_CPU_RT	44C2
VREG_CPU_SW1_R	45A2
VREG_CPU_SW2_R	45C3
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VREG_CPU_SW4	44C4
VREG_CPU_TRDET	44C4
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VREG_GPUPCIE_FB	52C1 58A8 58D5
VREG_GPUPCIE_FB_MID	58D5 52C1
VREG_PCIEX_ADJUST	52C3
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VREG_V3P3_COMP	48A8
VREG_V3P3_COMP_C	48A7
VREG_V3P3_DH	48C5
VREG_V3P3_DL	48B5
VREG_V3P3_EN	27D1 48C8
VREG_V3P3_FB	48B1 56D1
VREG_V3P3_FB_A3	56D4
VREG_V3P3_FB_MID	48A1 56C1
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VREG_V3P3_ILIM	48B5
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VREG_V3P3_ISENSE_N	48C1 56A7
VREG_V3P3_ISENSE_P	48C1 56A7
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VREG_V3P3_RAMP	48D5
VREG_V3P3_RSENSE	48C3
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VREG_V3P3_V5P0_VCCO	47D1 48D8
VREG_V3P3_V5P0_VDL	47D7
VREG_V5P0_BST	47C5
VREG_V5P0_CF2	56A6
VREG_V5P0_COMP	47A8
VREG_V5P0_COMP_C	47A8
VREG_V5P0_DH	47C5
VREG_V5P0_DL	47B5
VREG_V5P0_EN	27C1 47B8
VREG_V5P0_EN_R	47B7
VREG_V5P0_FB	47A1 56D8
VREG_V5P0_FB_A1	56D6
VREG_V5P0_FB_MID	47A1 56C8
VREG_V5P0_FB_MID_R	56C6
VREG_V5P0_FB_R	56A4
VREG_V5P0_ILIM	47B5
VREG_V5P0_IOUT	56B5
VREG_V5P0_ISENSE_N	47C1 56B7
VREG_V5P0_ISENSE_P	47C1 56B7
VREG_V5P0_PGND	47B5
VREG_V5P0_PWRGD	47D1 27B8
VREG_V5P0_RAMP	47C5
VREG_V5P0_RSENSE	47C3
VREG_V5P0_SEL	27C1 46C7
VREG_V5P0_SEL_B1	46C6
VREG_V5P0_SEL_B2	46C5
VREG_V5P0_SEL_C	46C6
VREG_V5P0_SEL_NGATE	46C5
VREG_V5P0_SEL_PGATE	46C5
VREG_V5P0_SS	47A7
VREG_V5P0_SW	47B5
VREG_V5P0_SW_S	47C4
VREG_V5P0_TRK	47C7
VREG_V12P0_A0	58C6
VREG_V12P0_A1	58C6
VREG_V12P0_ISENSE_N	38B1 58C8
VREG_V12P0_ISENSE_N_R	58C6
VREG_V12P0_ISENSE_P	38B1 58D8
VREG_V12P0_ISENSE_P_R	58D6
VREG_VCS_CF1	57C7
VREG_VCS_CF2	57C7
VREG_VCS_COMP	51B6
VREG_VCS_COMP_R	51A6
VREG_VCS_FB	51A1 57A2 57C8
VREG_VCS_FB_MID	51A1 57A2
VREG_VCS_FB_MID_R	57A4
VREG_VCS_HDRV	51C5
VREG_VCS_HDRV_R	51C4
VREG_VCS_IN	57B7
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VREG_VCS_LDRV	51B5
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VREG_VCS_NC	51C6
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VREG_VEDRAM_COMP_C	49A7
VREG_VEDRAM_DH	49C5
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VREG_VEDRAM_EN	27D1 49B8
VREG_VEDRAM_FB	49B1 55A7 55D1
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VREG_VEDRAM_FB_MID_R	55C3
VREG_VEDRAM_FREQ	49B7
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VREG_VEDRAM_ISENSE_P	49C1 55A7
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VREG_VMEM_CF2	55A6
VREG_VMEM_COMP	50A8
VREG_VMEM_COMP_C	50A7
VREG_VMEM_DH	50C5
VREG_VMEM_DL	50B5
VREG_VMEM_EN	27C1 50C8
VREG_VMEM_FB	50A1 55A7 55D6
VREG_VMEM_FB_MID	50A1 55C6
VREG_VMEM_FB_MID_R	55C4
VREG_VMEM_ILIM	50B5
VREG_VMEM_IOUT	55A5
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VREG_VMEM_ISENSE_P	50C1 55A7
VREG_VMEM_PGND	50B5
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VREG_VMEM_PWRGD_R	50D5
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VREG_VMEM_RSENSE	50C3
VREG_VMEM_SS	50A7
VREG_VMEM_SW	50B5
VREG_VMEM_SW_S	50C4
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VREG_VMEM_VEDRAM_SYNC	49C7
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V_3P3_VREF_VMEM_VEDRAM	55B3
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V_AUD_FLYN_N	33B4
V_AUD_FLYN_P	33B4
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V_AUD_FLYP_P	33C4
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V_AVDD_PEX	31D6
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V_AVSS0_SATA	31B6
V_AVSS1_SATA	31C6
V_AVSS_PEX	31D6
V_AVSS_USB	30D6
V_BMA	35D6
V_CMPAVDD18_USB	30C6
V_CMPAVDD33_USB	30A6
V_CMPAVDD_SATA	31B6
V_CMPAVSS18_USB	30C6
V_CMPAVSS33_USB	30A6

V_CMPAVSS_SATA	31B6
V_CPU_CORE_HF_GNDA_PLL	6A4
V_CPU_CORE_HF_VDDA_PLL	6B4
V_CPU_GNDA_RNG	6B4
V_CPU_PVDDA_ED	6B4
V_CPU_PVDDA_HS	6C4
V_CPU_PVDDA_MEM	6D4
V_CPU_PVDDA_PEX	6C4
V_CPU_PVSSA_ED	6B4
V_CPU_PVSSA_HS	6C4
V_CPU_PVSSA_MEM	6C4
V_CPU_PVSSA_PEX	6C4
V_CPU_VDDA_RNG	6B4
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V_GPU_GNDA_PLL	6A4
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WSS_CNTL_E	37C7
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C1A1	CAPN_805	[39B6]
C1A2	CAPN_805	[39B2]
C1A3	CAP_P_RDL	[39B3]
C1A6	CAPN_402	[39B2]
C1A7	CAPN_402	[39B6]
C1A8	CAPN_402	[39D2]
C1A9	CAPN_402	[39C2]
C1A10	CAPN_402	[54D2]
C1B1	CAPN_402	[41A7]
C1B2	CAPN_402	[41A7]
C1B3	CAPN_402	[41A7]
C1B4	CAPN_402	[41B7]
C1B7	CAPN_402	[41C7]
C1B8	CAPN_402	[41C7]
C1B9	CAP_P_RDL	[39D3]
C1B10	CAPN_402	[41D7]
C1B11	CAPN_402	[41D7]
C1B12	CAPN_1206	[46C4]
C1C1	CAP_P_RDL	[52C6]
C1C2	CAPN_603	[52C6]
C1C3	CAPN_603	[52C7]
C1D1	CAPN_805	[41C3]
C1D2	CAPN_402	[41C2]
C1E1	CAPN_603	[47C8]
C1E2	CAPN_603	[47C8]
C1E3	CAPN_402	[48A7]
C1E4	CAPN_402	[48A8]
C1E5	CAPN_402	[48A7]
C1F1	CAPN_603	[48C5]
C1F2	CAPN_402	[56A6]
C1F3	CAPN_805	[48C1]
C1F6	CAPN_805	[48C2]
C1F9	CAPN_805	[48C2]
C1F10	CAPN_402	[56B4]
C1F11	CAPN_402	[56B2]
C1G2	CAPN_805	[48C1]
C1G7	CAPN_402	[58B3]
C1G8	CAPN_402	[58A3]
C1G9	CAPN_402	[58A3]
C1G10	CAPN_402	[58A3]
C1G11	CAPN_402	[58B3]
C1G12	CAPN_402	[58B4]
C1G13	CAPN_805	[58B3]
C1N1	CAPN_805	[39C2]
C1N3	CAPN_402	[46C5]
C1N4	CAPN_402	[46C4]
C1N5	CAPN_805	[39D2]
C1P1	CAPN_402	[54D2]
C1R1	CAPN_402	[54B5]
C1T2	CAPN_805	[34C5]
C1T3	CAPN_402	[34C5]
C1T4	CAPN_402	[54D2]
C1U1	CAPN_1206	[48C3]
C1U2	CAPN_402	[56B6]
C1U3	CAPN_402	[54D3]
C2A1	CAPN_402	[40A7]
C2A2	CAPN_402	[37D6]
C2A3	CAPN_402	[37D8]
C2A5	CAPN_805	[38D5]
C2A6	CAPN_402	[38C6]
C2A7	CAPN_402	[38C6]
C2A8	CAPN_805	[37D6]
C2A9	CAP_P_RDL	[39C3]
C2A10	CAP_P_RDL	[38D6]
C2A11	CAPN_402	[38D6]
C2A12	CAPN_805	[38D5]
C2A13	CAP_P_RDL	[38D6]
C2A14	CAPN_402	[38D6]
C2A15	CAPN_402	[54D1]
C2B2	CAP_P_RDL	[46C4]
C2B3	CAPN_402	[26B1]
C2C2	CAPN_402	[37B1]
C2C3	CAPN_402	[59C7]
C2C4	CAPN_402	[59D3]
C2C5	CAPN_402	[59D2]
C2C6	CAPN_603	[59D2]
C2C7	CAPN_402	[26B1]
C2C8	CAPN_805	[32C8]
C2C9	CAPN_805	[32C8]
C2C10	CAPN_805	[32C6]
C2D1	CAPN_603	[32C5]
C2D2	CAPN_402	[32C5]
C2D3	CAPN_402	[32C8]
C2D4	CAPN_603	[32A5]
C2D5	CAPN_603	[32C6]
C2E1	CAPN_402	[29A6]
C2E2	CAPN_603	[47C8]
C2E3	CAPN_402	[47A8]
C2E4	CAPN_402	[47A8]
C2E5	CAPN_402	[47A7]
C2E6	CAPN_402	[47B7]
C2E7	CAPN_402	[47B7]
C2E8	CAP_P_TH	[47D8]
C2F1	CAPN_603	[47C5]
C2F2	CAPN_402	[56B4]
C2F3	CAPN_1206	[47D4]
C2F4	CAPN_402	[56D6]
C2F6	CAPN_402	[56A6]
C2F10	CAPN_1206	[47D3]
C2G1	CAPN_805	[47B2]
C2G2	CAPN_805	[47B2]
C2G5	CAP_P_TH	[47B1]
C2M1	CAPN_402	[37B2]
C2M2	CAPN_402	[37B2]
C2M3	CAPN_402	[38B4]
C2M4	CAPN_402	[38B3]
C2M5	CAPN_805	[38B4]
C2M6	CAPN_805	[38B5]
C2N3	CAPN_402	[54B5]
C2N4	CAPN_402	[35D5]
C2N5	CAPN_402	[35D6]
C2P1	CAPN_402	[54B4]
C2P2	CAPN_805	[32C5]
C2P3	CAPN_805	[32C6]
C2P4	CAPN_402	[32C7]
C2P5	CAPN_402	[32C7]
C2R3	CAPN_603	[32A6]
C2R5	CAPN_402	[32B5]
C2R6	CAPN_805	[32C6]
C2R7	CAPN_805	[31A2]
C2R8	CAPN_402	[23D6]
C2R9	CAPN_402	[31B2]
C2R10	CAPN_805	[31B8]
C2R11	CAPN_402	[31B3]
C2R12	CAPN_402	[31B3]
C2R13	CAPN_402	[31B2]
C2R14	CAPN_402	[31D1]
C2R15	CAPN_603	[31B7]
C2R16	CAPN_402	[31B7]
C2R17	CAPN_603	[31C2]
C2R18	CAPN_402	[31B7]
C2R19	CAPN_603	[31B7]
C2R20	CAPN_402	[31D2]
C2R21	CAPN_402	[54B4]
C2R22	CAPN_402	[54B7]
C2T1	CAPN_805	[31A7]
C2T2	CAPN_402	[31A6]
C2T3	CAPN_402	[31A6]
C2T4	CAPN_402	[31D1]
C2T5	CAPN_402	[31A7]
C2T6	CAPN_402	[30C2]
C2T7	CAPN_805	[31B8]
C2T8	CAPN_603	[31A7]
C2T9	CAPN_603	[31C2]
C2T10	CAPN_402	[30C6]
C2T11	CAPN_402	[30C6]
C2T12	CAPN_805	[31C2]
C2T13	CAPN_402	[28A6]
C2T14	CAPN_402	[30C7]
C2T15	CAPN_805	[30C7]
C2T16	CAPN_805	[30C8]
C2T18	CAPN_402	[34C4]
C2T19	CAPN_402	[54B6]
C2U1	CAPN_402	[54B7]
C2V1	CAPN_805	[47B2]
C2V2	CAPN_402	[54C6]
C2V4	CAPN_805	[47B2]
C2V5	CAPN_805	[47B3]
C3A1	CAPN_402	[37B6]
C3A2	CAPN_402	[37B2]
C3A3	CAPN_402	[33B3]
C3A4	CAPN_402	[33B3]
C3A5	CAPN_402	[33D3]
C3A6	CAPN_603	[33D3]
C3A7	CAPN_402	[33D6]
C3A8	CAPN_402	[33C3]
C3A9	CAPN_603	[33B3]
C3A10	CAPN_402	[33A3]
C3B1	CAPN_402	[23B2]
C3B2	CAPN_402	[23B2]
C3B3	CAPN_402	[23B2]
C3B4	CAPN_402	[23C2]
C3B5	CAPN_402	[22D8]
C3B6	CAPN_402	[22D8]
C3B7	CAPN_402	[22A2]
C3B8	CAPN_402	[22A1]
C3B9	CAPN_402	[22B1]
C3B10	CAPN_402	[22A1]
C3B11	CAPN_603	[33D6]
C3B12	CAPN_402	[33D6]
C3C1	CAPN_805	[24A7]
C3C2	CAPN_805	[24A7]
C3C3	CAPN_402	[54C1]
C3D1	CAPN_603	[59D3]
C3D2	CAPN_402	[26D2]
C3E1	CAPN_402	[26D2]
C3E2	CAPN_402	[26C2]
C3E3	CAPN_402	[26D2]
C3E4	CAPN_402	[58D4]
C3E5	CAPN_402	[58B7]
C3E6	CAPN_402	[54C7]
C3E7	CAPN_402	[54C2]
C3F1	CAPN_1206	[49D3]
C3F2	CAPN_402	[49A7]
C3F3	CAPN_402	[49A8]
C3F4	CAPN_402	[49A7]
C3F5	CAPN_603	[49C5]
C3F6	CAPN_402	[55A6]
C3F7	CAPN_1206	[49D3]
C3F8	CAP_P_TH	[49D8]
C3G1	CAPN_603	[49C8]
C3G2	CAPN_402	[55B6]
C3G3	CAPN_603	[49C8]
C3G4	CAPN_402	[55A6]
C3G5	CAPN_402	[55D4]
C3G6	CAPN_402	[50A7]
C3G7	CAPN_402	[50A8]
C3G8	CAPN_402	[50A7]
C3G9	CAPN_603	[50C5]
C3G10	CAPN_402	[55B3]
C3G11	CAPN_402	[55B4]
C3G12	CAPN_402	[54C5]
C3G13	CAPN_1206	[35A7]
C3G14	CAPN_1206	[35A6]
C3M1	CAPN_402	[37B6]
C3M2	CAPN_805	[33A3]
C3M3	CAPN_805	[33A3]
C3M4	CAPN_603	[33C3]
C3M5	CAPN_402	[54D7]
C3M6	CAPN_603	[33C3]
C3N1	CAPN_805	[25C8]
C3N2	CAPN_805	[25B8]
C3N3	CAPN_805	[25C7]

C3N4	CAPN_805	[25B7]
C3N5	CAPN_805	[24A7]
C3N6	CAPN_402	[25C7]
C3N7	CAPN_402	[25C7]
C3N8	CAPN_402	[25C8]
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C3N14	CAPN_402	[24A4]
C3N15	CAPN_402	[24A6]
C3N16	CAPN_402	[24A6]
C3N17	CAPN_402	[24B6]
C3N18	CAPN_402	[25C1]
C3N19	CAPN_402	[25C2]
C3N20	CAPN_402	[24C6]
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C3N22	CAPN_805	[24A8]
C3N23	CAPN_805	[24C6]
C3N24	CAPN_402	[24A5]
C3N25	CAPN_402	[24A3]
C3N26	CAPN_402	[24A5]
C3N27	CAPN_402	[24C5]
C3N28	CAPN_402	[24A3]
C3N29	CAPN_402	[25C3]
C3N30	CAPN_402	[25C3]
C3N31	CAPN_402	[25C2]
C3N32	CAPN_402	[24A4]
C3N33	CAPN_402	[25C3]
C3N34	CAPN_805	[24A6]
C3N35	CAPN_402	[24A1]
C3N36	CAPN_805	[24C6]
C3N37	CAPN_805	[24C7]
C3N38	CAPN_402	[24C6]
C3N39	CAPN_402	[25C2]
C3N40	CAPN_402	[54D7]
C3N41	CAPN_603	[33C3]
C3P1	CAPN_402	[25D3]
C3P2	CAPN_402	[24A4]
C3P3	CAPN_805	[25D2]
C3P4	CAPN_805	[25D1]
C3P5	CAPN_402	[24A5]
C3P6	CAPN_402	[24A3]
C3P7	CAPN_402	[24A2]
C3P8	CAPN_402	[24A2]
C3P9	CAPN_402	[24A2]
C3P10	CAPN_402	[54B3]
C3R1	CAPN_402	[30A2]
C3R2	CAPN_603	[27D6]
C3R3	CAPN_603	[31A2]
C3R4	CAPN_402	[30A2]
C3R5	CAPN_805	[30A8]
C3R6	CAPN_402	[31B2]
C3R7	CAPN_402	[31D3]
C3R8	CAPN_402	[31D2]
C3R9	CAPN_402	[26C7]
C3R10	CAPN_402	[31D3]
C3R11	CAPN_402	[31D3]
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C3R14	CAPN_402	[26C8]
C3R15	CAPN_402	[31D7]
C3R16	CAPN_603	[31D7]
C3R17	CAPN_402	[31D1]
C3R18	CAPN_402	[31D2]
C3R19	CAPN_402	[54B1]
C3R20	CAPN_402	[54B4]
C3R21	CAPN_402	[54C2]
C3T1	CAPN_402	[31C6]
C3T2	CAPN_805	[31D8]
C3T3	CAPN_402	[31C7]
C3T4	CAPN_603	[30A7]
C3T5	CAPN_805	[31C7]
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C3T11	CAPN_402	[30D6]
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C3T13	CAPN_603	[30C7]
C3T14	CAPN_603	[30D7]
C3T15	CAPN_603	[30A7]
C3T16	CAPN_402	[23D8]
C3T17	CAPN_805	[30D8]
C3T18	CAPN_402	[23D8]
C3T19	CAPN_805	[30A8]
C3T20	CAPN_402	[54B6]
C3T21	CAPN_402	[54B6]
C3T23	CAPN_402	[54C6]
C3T24	CAPN_402	[54C3]
C3U1	CAPN_402	[54B7]
C3U2	CAPN_402	[58B6]
C3U3	CAPN_402	[58B7]
C3U4	CAPN_402	[54C6]
C3V1	CAPN_603	[49C8]
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C3V3	CAPN_402	[54C5]
C3V4	CAPN_402	[35A6]
C3V5	CAPN_402	[35A6]
C3V6	CAPN_402	[35A5]
C4A1	CAPN_402	[39A7]
C4A3	CAPN_402	[37A7]
C4A4	CAPN_402	[37A4]
C4A5	CAPN_402	[37A4]
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C4A8	CAPN_402	[37A4]
C4A9	CAPN_402	[37A7]
C4A10	CAPN_402	[37A7]
C4A11	CAPN_402	[41A2]
C4A12	CAPN_402	[59D4]
C4A14	CAPN_805	[41B4]
C4B1	CAPN_402	[57B7]
C4B2	CAPN_402	[22D6]
C4B3	CAPN_402	[23A6]
C4B4	CAPN_805	[51C5]
C4B5	CAPN_603	[51A6]
C4B6	CAPN_402	[51A7]
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C4B10	CAPN_805	[41D2]
C4B11	CAPN_805	[51C5]
C4B12	CAPN_805	[51C4]
C4B13	CAPN_402	[51A4]
C4B14	CAPN_1206	[51C5]
C4C1	CAPN_402	[23A2]
C4C2	CAPN_402	[4B6]
C4C3	CAPN_402	[60A6]
C4C4	CAPN_402	[60A5]
C4C5	CAPN_402	[51B6]
C4C6	CAPN_402	[4B6]
C4C7	CAPN_402	[4B6]
C4C8	CAPN_402	[5B7]
C4E1	CAPN_402	[4D6]
C4E2	CAPN_402	[4D6]
C4E3	CAP_P_RDL	[49C2]
C4E6	CAP_P_RDL	[49C2]
C4E9	CAPN_805	[52A6]
C4E10	CAPN_603	[52B8]
C4E11	CAPN_603	[52C4]
C4E12	CAPN_805	[52C2]
C4E13	CAPN_402	[52C3]
C4F7	CAP_P_RDL	[49C1]
C4F8	CAPN_402	[52A7]
C4G1	CAPN_402	[54B2]
C4M1	CAPN_402	[54B7]
C4N1	CAPN_402	[57B5]
C4N2	CAPN_402	[54B2]
C4N3	CAPN_402	[54B5]
C4N4	CAPN_402	[57D4]
C4N5	CAPN_402	[54B5]
C4N6	CAPN_402	[54C7]
C4N7	CAPN_603	[51C6]
C4N8	CAPN_402	[54B4]
C4N9	CAPN_603	[51C6]
C4N10	CAPN_805	[51C4]
C4P1	CAPN_402	[36C6]
C4P2	CAPN_402	[23A6]
C4P3	CAPN_402	[54C7]
C4R1	CAPN_603	[52A2]
C4R2	CAPN_603	[52A4]
C4R3	CAPN_402	[52A2]
C4R4	CAPN_402	[5C1]
C4T1	CAPN_603	[2D5]
C4T3	CAPN_805	[9A3]
C4T4	CAPN_805	[9A3]
C4T7	CAPN_1206	[49B1]
C4U4	CAP_P_SM	[50B2]
C4V1	CAPN_402	[54B2]
C5A1	CAPN_402	[53B4]
C5A2	CAPN_805	[53B3]
C5A3	CAPN_603	[53B3]
C5A6	CAPN_805	[41B5]
C5A7	CAPN_402	[41B4]
C5A8	CAPN_603	[41B5]
C5A9	CAPN_805	[53C8]
C5A11	CAPN_805	[41B5]
C5A12	CAPN_603	[36C3]
C5A14	CAPN_402	[41B4]
C5A15	CAPN_603	[36C3]
C5B1	CAPN_402	[53C4]
C5B2	CAPN_805	[53C3]
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C5B17	CAPN_402	[41D2]
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C5C2	CAP_P_RDL	[51B1]
C5C3	CAP_P_RDL	[43A5]
C5C6	CAPN_805	[51B1]
C5D1	CAPN_805	[9D1]
C5D2	CAPN_805	[9B7]
C5D3	CAPN_805	[9C7]
C5D4	CAPN_805	[9C1]
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C5D12	CAPN_805	[9B8]
C5D13	CAPN_805	[9D7]
C5D14	CAPN_805	[9C7]
C5E1	CAPN_402	[4C3]
C5E2	CAPN_402	[4D3]
C5E3	CAPN_402	[4C3]
C5E4	CAPN_402	[4C3]
C5E5	CAPN_805	[9C3]
C5E6	CAPN_805	[9D3]
C5E7	CAPN_805	[9C3]
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C5E11	CAPN_1206	[49B2]
C5F1	CAPN_402	[19A7]
C5F2	CAPN_402	[20A2]
C5F3	CAPN_402	[20A2]
C5F4	CAPN_402	[20A3]

C5F5	CAPN_402	[20A1]
C5F6	CAPN_402	[20A1]
C5F7	CAPN_402	[20A3]
C5F8	CAPN_402	[20A1]
C5F9	CAPN_402	[20A3]
C5F10	CAPN_805	[18A4]
C5G1	CAP_P_RDL	[38B6]
C5G2	CAPN_402	[38B5]
C5G3	CAPN_402	[38A5]
C5G4	CAPN_402	[38A6]
C5G5	CAPN_402	[38A6]
C5G6	CAPN_805	[35B6]
C5G7	CAPN_402	[35B6]
C5G8	CAPN_402	[54C4]
C5M5	CAPN_603	[53A6]
C5N5	CAPN_805	[45B5]
C5N6	CAPN_603	[45A5]
C5N7	CAPN_402	[57D5]
C5N8	CAPN_402	[57D7]
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C5N10	CAPN_805	[51C4]
C5N11	CAPN_805	[51C4]
C5P1	CAPN_805	[51B2]
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C5R2	CAPN_805	[9A6]
C5R3	CAPN_805	[9B6]
C5R4	CAPN_805	[9C1]
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C5R7	CAPN_805	[9C6]
C5R8	CAPN_805	[9D6]
C5R9	CAPN_805	[9D5]
C5R10	CAPN_805	[9C8]
C5R11	CAPN_603	[2D5]
C5R12	CAPN_805	[9B8]
C5R13	CAPN_805	[9A7]
C5R14	CAPN_805	[6D5]
C5R15	CAPN_805	[9C8]
C5R16	CAPN_805	[9B7]
C5R17	CAPN_805	[6C5]
C5R18	CAPN_805	[9B5]
C5R19	CAPN_402	[11A6]
C5R20	CAPN_402	[11B6]
C5R21	CAPN_402	[11C3]
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C5R23	CAPN_402	[11A6]
C5R24	CAPN_402	[11B5]
C5R25	CAPN_402	[11D6]
C5R26	CAPN_402	[10D5]
C5R27	CAPN_402	[10C3]
C5R28	CAPN_402	[10C3]
C5R29	CAPN_402	[11A5]
C5R30	CAPN_402	[11D4]
C5R31	CAPN_805	[6A6]
C5R32	CAPN_402	[10B5]
C5R33	CAPN_402	[10C6]
C5R34	CAPN_402	[11B3]
C5R35	CAPN_402	[9D2]
C5R36	CAPN_402	[10A5]
C5R37	CAPN_402	[10C4]
C5R38	CAPN_402	[10B6]
C5R39	CAPN_402	[10C6]
C5R40	CAPN_402	[10C6]
C5R41	CAPN_402	[11B4]
C5R42	CAPN_805	[6B6]
C5R43	CAPN_402	[9C2]
C5R44	CAPN_402	[11B5]
C5R45	CAPN_402	[10A4]
C5R46	CAPN_402	[10B4]
C5R47	CAPN_402	[11B5]
C5R48	CAPN_402	[11B5]
C5R49	CAPN_402	[10C4]
C5R50	CAPN_402	[9B2]
C5R51	CAPN_402	[10B3]
C5R52	CAPN_402	[11C4]
C5R53	CAPN_402	[11C5]
C5R54	CAPN_805	[6B6]
C5R55	CAPN_402	[10B3]
C5R56	CAPN_402	[11A5]
C5R57	CAPN_402	[10B4]
C5R58	CAPN_402	[9C2]
C5R59	CAPN_402	[10C3]
C5R60	CAPN_402	[10C5]
C5R61	CAPN_402	[10C5]
C5R62	CAPN_402	[10B3]
C5R63	CAPN_402	[10C3]
C5R64	CAPN_402	[10B4]
C5T1	CAPN_402	[9B2]
C5T2	CAPN_402	[11B3]
C5T3	CAPN_402	[11C3]
C5T4	CAPN_805	[6A5]
C5T5	CAPN_402	[11B3]
C5T6	CAPN_402	[6A4]
C5T7	CAPN_402	[9C2]
C5T8	CAPN_402	[10C4]
C5T9	CAPN_805	[6C5]
C5T10	CAPN_402	[10D4]
C5T11	CAPN_402	[10A5]
C5T12	CAPN_402	[10D6]
C5T13	CAPN_805	[6B5]
C5T14	CAPN_402	[11D3]
C5T15	CAPN_402	[11C4]
C5T16	CAPN_402	[11C3]
C5T17	CAPN_402	[10D4]
C5T18	CAPN_402	[11A4]
C5T19	CAPN_402	[11C6]
C5T20	CAPN_402	[9B4]
C5T21	CAPN_402	[9A4]
C5T22	CAPN_402	[9B4]
C5T23	CAPN_402	[9B4]
C5T24	CAPN_402	[9C4]
C5T25	CAPN_402	[9A4]
C5T26	CAPN_402	[9D4]
C5T27	CAPN_402	[9B4]
C5T28	CAPN_402	[11C4]
C5T29	CAPN_402	[11B5]
C5T30	CAPN_402	[11B5]
C5T31	CAPN_402	[9C4]
C5T32	CAPN_402	[9C4]
C5T33	CAPN_805	[9A5]
C5T34	CAPN_805	[9B3]
C5T35	CAPN_805	[9C3]
C5T36	CAPN_402	[4A5]
C5T37	CAPN_402	[13A6]
C5T38	CAPN_402	[13A1]
C5T39	CAPN_402	[13A2]
C5T41	CAPN_402	[13A5]
C5T42	CAPN_402	[13A2]
C5T43	CAPN_805	[9B3]
C5T44	CAPN_402	[13A1]
C5T45	CAPN_402	[13A2]
C5T46	CAPN_402	[13A5]
C5T47	CAPN_402	[13A5]
C5T48	CAPN_402	[13A2]
C5T49	CAPN_402	[13A5]
C5T50	CAPN_402	[13A6]
C5T52	CAPN_1206	[49B2]
C5U1	CAPN_402	[18A5]
C5U2	CAPN_805	[13A6]
C5U3	CAPN_402	[21A2]
C5U4	CAPN_402	[21A3]
C5U5	CAPN_402	[21A3]
C5U6	CAPN_402	[21A2]
C5U7	CAPN_402	[21A2]
C5U8	CAPN_402	[21A3]
C5U9	CAPN_402	[18A7]
C5U10	CAPN_402	[21A1]
C5U11	CAPN_402	[21A1]
C5U12	CAPN_402	[21A6]
C6A1	CAPN_402	[38A3]
C6A2	CAPN_402	[38A2]
C6A3	CAPN_402	[38A2]
C6A4	CAP_P_RDL	[38A3]
C6A5	CAP_P_RDL	[38A3]
C6A6	CAPN_603	[58C6]
C6A7	CAP_P_RDL	[36C3]
C6B1	CAP_P_TH	[43B5]
C6B2	CAPN_1206	[45A3]
C6B3	CAPN_1206	[43B4]
C6B4	CAPN_603	[45D7]
C6B5	CAPN_1206	[43B4]
C6C1	CAP_P_RDL	[43A6]
C6C2	CAP_P_RDL	[43A5]
C6C3	CAP_P_RDL	[43A6]
C6D1	CAPN_805	[9A8]
C6D2	CAPN_805	[9A7]
C6D3	CAPN_805	[9C6]
C6D4	CAPN_805	[9C6]
C6D5	CAPN_805	[9B8]
C6D6	CAPN_805	[9A6]
C6F1	CAPN_402	[18A2]
C6F2	CAPN_402	[18A2]
C6F3	CAPN_402	[21A7]
C6F4	CAPN_402	[18A3]
C6F5	CAPN_402	[18A2]
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C6F8	CAPN_402	[18A3]
C6F9	CAPN_402	[18A1]
C6F10	CAPN_402	[18A3]
C6F11	CAPN_805	[20A4]
C6G1	CAP_P_RDL	[39D7]
C6G2	CAPN_402	[39D7]
C6G3	CAPN_805	[39D7]
C6M5	CAPN_402	[58D6]
C6N1	CAPN_805	[45D5]
C6N2	CAPN_603	[45D5]
C6N3	CAPN_1206	[45B3]
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C6R3	CAPN_805	[9C8]
C6R4	CAPN_805	[9D8]
C6R5	CAPN_805	[9A8]
C6R6	CAPN_805	[9C6]
C6R7	CAPN_805	[9B6]
C6R8	CAPN_402	[11D5]
C6R9	CAPN_402	[11B6]
C6R10	CAPN_402	[11B6]
C6R11	CAPN_402	[12A2]
C6R12	CAPN_402	[11B3]
C6R13	CAPN_402	[11C3]
C6R14	CAPN_402	[11B3]
C6R15	CAPN_402	[10B4]
C6R16	CAPN_402	[12A2]
C6R17	CAPN_402	[10A3]
C6R18	CAPN_402	[10A3]
C6R19	CAPN_402	[11C5]
C6R20	CAPN_402	[10A4]
C6R21	CAPN_402	[10B4]
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C6R27	CAPN_402	[12A3]
C6R28	CAPN_402	[10B5]
C6R29	CAPN_402	[11A5]
C6R30	CAPN_402	[11A4]
C6R31	CAPN_402	[10B6]
C6R32	CAPN_402	[11A5]
C6R33	CAPN_402	[10C4]
C6R34	CAPN_402	[11C5]
C6R35	CAPN_402	[11C5]
C6R36	CAPN_402	[10D3]
C6R37	CAPN_402	[10C4]
C6R38	CAPN_402	[10A6]
C6R39	CAPN_402	[11D5]

C6R40	CAPN_402	[11A3]
C6R41	CAPN_402	[11A3]
C6R42	CAPN_402	[10C4]
C6R43	CAPN_402	[10A6]
C6R44	CAPN_402	[10A4]
C6R45	CAPN_402	[10C4]
C6R46	CAPN_402	[12A1]
C6T2	CAPN_402	[11B4]
C6T3	CAPN_402	[11C5]
C6T4	CAPN_402	[11A5]
C6T5	CAPN_402	[11D3]
C6T6	CAPN_402	[10B5]
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C6T8	CAPN_402	[10B4]
C6T9	CAPN_402	[11C3]
C6T10	CAPN_402	[12A6]
C6T11	CAPN_402	[10C4]
C6T12	CAPN_402	[10B6]
C6T13	CAPN_402	[11A3]
C6T14	CAPN_402	[10A4]
C6T15	CAPN_402	[11C6]
C6T16	CAPN_402	[11A4]
C6T17	CAPN_402	[11A3]
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C6T25	CAPN_402	[11B3]
C6T26	CAPN_402	[13A2]
C6T27	CAPN_402	[12A6]
C6T28	CAPN_402	[13A5]
C6T29	CAPN_402	[12A5]
C6T30	CAPN_805	[12A2]
C6T31	CAPN_402	[13A1]
C6T32	CAPN_402	[12A5]
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C6U2	CAPN_402	[19A2]
C6U3	CAPN_402	[19A3]
C6U4	CAPN_402	[19A2]
C6U5	CAPN_402	[19A1]
C6U6	CAPN_402	[19A3]
C6U7	CAPN_402	[20A7]
C6U8	CAPN_402	[19A1]
C6U9	CAPN_402	[19A3]
C6U10	CAPN_402	[21A6]
C7A1	CAPN_603	[38A3]
C7A2	CAPN_603	[38A3]
C7A3	CAPN_603	[38A3]
C7A4	CAPN_603	[38A2]
C7B1	CAPN_1206	[43B6]
C7B2	CAP_P_TH	[38A3]
C7B3	CAP_P_TH	[43B5]
C7B4	CAPN_402	[54D6]
C7B5	CAPN_1206	[45D3]
C7B7	CAPN_402	[44A6]
C7B8	CAP_P_TH	[49D8]
C7C1	CAPN_402	[44B5]
C7C2	CAPN_402	[44A7]
C7C3	CAPN_402	[44B5]
C7C4	CAPN_402	[44A5]
C7C5	CAPN_402	[44A7]
C7C6	CAPN_402	[44A2]
C7C7	CAPN_402	[44B2]
C7C8	CAPN_805	[45C3]
C7C9	CAPN_402	[44D3]
C7C10	CAPN_1206	[44D5]
C7C11	CAPN_603	[44D4]
C7C12	CAP_P_RDL	[43A4]
C7C13	CAP_P_RDL	[43A4]
C7D7	CAPN_402	[16A1]
C7D8	CAPN_402	[16A1]
C7D9	CAPN_402	[16A3]
C7D10	CAPN_402	[16A2]
C7D11	CAPN_805	[16A4]
C7D12	CAPN_402	[17A7]
C7D13	CAPN_402	[16A3]
C7D14	CAPN_402	[16A2]
C7D15	CAPN_402	[21A4]
C7E1	CAPN_402	[21A4]
C7E2	CAPN_402	[16A2]
C7E3	CAPN_402	[16A3]
C7E4	CAPN_402	[14A1]
C7E5	CAPN_402	[14A2]
C7E6	CAPN_402	[14A3]
C7E7	CAPN_402	[14A1]
C7E8	CAPN_805	[14A4]
C7E9	CAPN_402	[15A7]
C7E10	CAPN_402	[14A2]
C7E11	CAPN_402	[14A3]
C7E12	CAPN_402	[21A5]
C7E13	CAPN_402	[14A2]
C7E14	CAPN_402	[14A3]
C7F1	CAPN_805	[50C2]
C7F2	CAP_P_RDL	[50C2]
C7F3	CAPN_1206	[50D3]
C7G1	CAP_P_RDL	[39C7]
C7G2	CAPN_402	[39C7]
C7N1	CAPN_1206	[45D3]
C7P1	CAPN_402	[44A5]
C7P2	CAPN_603	[44D6]
C7R1	CAP_P_SM	[50B2]
C7R2	CAPN_402	[17A1]
C7R3	CAPN_402	[17A1]
C7R4	CAPN_402	[17A3]
C7R5	CAPN_402	[17A2]
C7R6	CAPN_402	[16A7]
C7R7	CAPN_402	[17A3]
C7R8	CAPN_402	[17A2]
C7R9	CAPN_402	[21A4]
C7T1	CAPN_402	[17A2]
C7T2	CAPN_402	[17A3]
C7T3	CAPN_402	[15A1]
C7T4	CAPN_402	[15A2]
C7T5	CAPN_402	[15A3]
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C7T7	CAPN_402	[14A7]
C7T8	CAPN_402	[15A2]
C7T9	CAPN_402	[15A3]
C7T10	CAPN_402	[21A5]
C7T11	CAPN_402	[15A2]
C7T12	CAPN_402	[15A3]
C7U1	CAPN_1206	[50D3]
C7V1	CAPN_805	[39C7]
D4A1	DIODE_SOT23	[36C5]
D4D1	LED_SM	[60B5]
D5B1	DIODE_SOT23	[45B6]
D6B1	DIODE_SOT23	[45D6]
DB1E1	DBPAD_TP	[42C1]
DB1F1	DBPAD_TP	[58A2]
DB1F2	DBPAD_TP	[48B1]
DB1V1	DBPAD_TP	[58B1]
DB1V2	DBPAD_TP	[58B1]
DB1V3	DBPAD_TP	[58B1]
DB2E1	DBPAD_TP	[52C5]
DB2G1	DBPAD_TP	[48C1]
DB2G2	DBPAD_TP	[47C1]
DB2G3	DBPAD_TP	[27A8]
DB2G4	DBPAD_TP	[47B1]
DB2N1	DBPAD_TP	[35C4]
DB2N2	DBPAD_TP	[35C4]
DB2N3	DBPAD_TP	[35C4]
DB2R1	DBPAD_TP	[32B5]
DB2R2	DBPAD_TP	[26B3]
DB2R3	DBPAD_TP	[26B3]
DB2R4	DBPAD_TP	[26B3]
DB2R5	DBPAD_TP	[26B3]
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DB2R7	DBPAD_TP	[26B3]
DB2R8	DBPAD_TP	[26D6]
DB2R9	DBPAD_TP	[26B3]
DB2R10	DBPAD_TP	[26B3]
DB2R11	DBPAD_TP	[26C3]
DB2R12	DBPAD_TP	[26C3]
DB2R13	DBPAD_TP	[26C3]
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DB4E1	DBPAD_TP	[52C1]
DB4E2	DBPAD_TP	[52B5]
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DB4N3	DBPAD_TP	[51B6]
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DB4N7	DBPAD_TP	[23A2]
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DB4P7	DBPAD_TP	[51C6]
DB4P8	DBPAD_TP	[51C8]
DB4R1	DBPAD_TP	[5C4]
DB5A1	DBPAD_TP	[53A3]
DB5B1	DBPAD_TP	[53B1]
DB5B2	DBPAD_TP	[51A3]
DB5B3	DBPAD_TP	[51A3]
DB5B4	DBPAD_TP	[53C1]
DB5B5	DBPAD_TP	[53C3]
DB5C1	DBPAD_TP	[51B1]
DB5R5	DBPAD_TP	[6B5]
DB6M1	DBPAD_TP	[38A4]
DB6M2	DBPAD_TP	[38B4]
DB6M3	DBPAD_TP	[38B4]
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DB7C3	DBPAD_TP	[44C4]
DB7C4	DBPAD_TP	[45C1]
DB7C5	DBPAD_TP	[44A8]
DB7C6	DBPAD_TP	[44A8]
DB7F1	DBPAD_TP	[50C2]
DB7F2	DBPAD_TP	[50B2]
DB7P1	DBPAD_TP	[44C2]
DB7P2	DBPAD_TP	[44C2]
EG1A1	ESDGUARD_402	[39A7]
EG1A2	ESDGUARD_402	[39A7]
EG1A3	ESDGUARD_402	[39B2]
EG1A4	ESDGUARD_402	[39B3]
EG1A5	ESDGUARD_402	[39A2]
EG1A6	ESDGUARD_402	[39A3]
EG1A7	ESDGUARD_402	[39C2]
EG1A8	ESDGUARD_402	[39C3]
EG1B1	ESDGUARD_402	[41C7]
EG1B2	ESDGUARD_402	[41C6]
EG1B3	ESDGUARD_402	[41D7]
EG1B4	ESDGUARD_402	[41D6]
EG2A1	ESDGUARD_402	[37D7]
EG2A2	ESDGUARD_402	[38C4]
EG2A3	ESDGUARD_402	[38C5]
EG2A4	ESDGUARD_402	[38C6]
EG2A5	ESDGUARD_402	[38C6]

EG2A6	ESDGUARD_402	[38C6]
EG2A7	ESDGUARD_402	[38B6]
EG3A1	ESDGUARD_402	[40D6]
EG3A2	ESDGUARD_402	[40D7]
EG3A3	ESDGUARD_402	[40C6]
EG3A4	ESDGUARD_402	[40C7]
EG3A5	ESDGUARD_402	[40C6]
EG4A1	ESDGUARD_402	[39A7]
EG4A2	ESDGUARD_402	[40C7]
EG4A3	ESDGUARD_402	[40B6]
EG4A4	ESDGUARD_402	[40B7]
EG4A5	ESDGUARD_402	[37A5]
EG4A6	ESDGUARD_402	[37A5]
EG4A7	ESDGUARD_402	[37A8]
EG4A8	ESDGUARD_402	[37A8]
EG4A9	ESDGUARD_402	[37A2]
EG4A10	ESDGUARD_402	[37A2]
EG4M1	ESDGUARD_402	[40A6]
EG4M2	ESDGUARD_402	[40A7]
EG4M5	ESDGUARD_402	[40A2]
EG6G1	ESDGUARD_402	[39C7]
EG6G2	ESDGUARD_402	[39C7]
EG7G1	ESDGUARD_402	[39C7]
EG7G2	ESDGUARD_402	[39C7]
FB1A1	FERRITE_603	[39B7]
FB2C1	FERRITE_603	[32D8]
FB2M1	FERRITE_603	[38C4]
FB2R1	FERRITE_603	[32C5]
FB2R2	FERRITE_603	[31B7]
FB2R3	FERRITE_603	[31C7]
FB2T1	FERRITE_603	[31A7]
FB2T2	FERRITE_603	[31B7]
FB2T3	FERRITE_603	[30C7]
FB3A1	FERRITE_603	[33B2]
FB3A2	FERRITE_603	[33C2]
FB3N1	FERRITE_603	[25C8]
FB3N2	FERRITE_603	[25B8]
FB3N3	FERRITE_603	[24C6]
FB3N4	FERRITE_603	[24C6]
FB3P1	FERRITE_603	[25D2]
FB3R1	FERRITE_603	[30A7]
FB3R2	FERRITE_603	[31D7]
FB3T1	FERRITE_603	[30C8]
FB3T2	FERRITE_603	[30D7]
FB3T3	FERRITE_603	[30A7]
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FB5R2	FERRITE_603	[6C6]
FB5R3	FERRITE_603	[6A6]
FB5R4	FERRITE_603	[6B6]
FB5R5	FERRITE_603	[6B6]
FB5T1	FERRITE_603	[6A6]
FB5T2	FERRITE_603	[6C6]
FB5T3	FERRITE_603	[6B6]
FT1M3	FTPAD_TP	[41A7]
FT1M4	FTPAD_TP	[41A7]
FT1M5	FTPAD_TP	[41A6]
FT1N1	FTPAD_TP	[46C2]
FT1N2	FTPAD_TP	[41B7]
FT1N3	FTPAD_TP	[41A7]
FT1N4	FTPAD_TP	[41D5]
FT1N5	FTPAD_TP	[41D5]
FT1N6	FTPAD_TP	[41C5]
FT1N7	FTPAD_TP	[41C5]
FT1N8	FTPAD_TP	[41C5]
FT1N9	FTPAD_TP	[46C2]
FT1P1	FTPAD_TP	[46B7]
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FT1T2	FTPAD_TP	[34C8]
FT1T3	FTPAD_TP	[34C8]
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FT1T6	FTPAD_TP	[34C8]
FT1T7	FTPAD_TP	[34C8]
FT1T8	FTPAD_TP	[34C8]
FT1T9	FTPAD_TP	[48A1]
FT1T10	FTPAD_TP	[48C8]
FT1T11	FTPAD_TP	[34C4]
FT2M1	FTPAD_TP	[38D7]
FT2M2	FTPAD_TP	[38D7]
FT2P2	FTPAD_TP	[22B1]
FT2R1	FTPAD_TP	[22A1]
FT2R2	FTPAD_TP	[26A3]
FT2R3	FTPAD_TP	[22B1]
FT2R4	FTPAD_TP	[22C1]
FT2R5	FTPAD_TP	[22A1]
FT2R6	FTPAD_TP	[35A7]
FT2R7	FTPAD_TP	[35A3]
FT2T1	FTPAD_TP	[52C5]
FT2T2	FTPAD_TP	[47C8]
FT2T3	FTPAD_TP	[47A1]
FT2T4	FTPAD_TP	[35A7]
FT2T5	FTPAD_TP	[35A7]
FT2U2	FTPAD_TP	[41B3]
FT2U3	FTPAD_TP	[41B3]
FT2V1	FTPAD_TP	[27A8]
FT2V2	FTPAD_TP	[47C1]
FT2V3	FTPAD_TP	[48C1]
FT2V4	FTPAD_TP	[35A3]
FT3M1	FTPAD_TP	[40D7]
FT3M2	FTPAD_TP	[40D7]
FT3M3	FTPAD_TP	[40D7]
FT3M4	FTPAD_TP	[40C7]
FT3M5	FTPAD_TP	[40C7]
FT3M6	FTPAD_TP	[33B7]
FT3M7	FTPAD_TP	[40D7]
FT3M8	FTPAD_TP	[40D7]
FT3M9	FTPAD_TP	[40D7]
FT3M10	FTPAD_TP	[40C7]
FT3M11	FTPAD_TP	[40C7]
FT3N1	FTPAD_TP	[22B4]
FT3N2	FTPAD_TP	[22A1]
FT3N3	FTPAD_TP	[33D7]
FT3P1	FTPAD_TP	[22D7]
FT3P2	FTPAD_TP	[22D3]
FT3P3	FTPAD_TP	[22B1]
FT3P4	FTPAD_TP	[22B1]
FT3P5	FTPAD_TP	[22B8]
FT3P6	FTPAD_TP	[22B8]
FT3P7	FTPAD_TP	[22B8]
FT3P8	FTPAD_TP	[22B8]
FT3P9	FTPAD_TP	[22B8]
FT3R1	FTPAD_TP	[22D3]
FT3R3	FTPAD_TP	[22D3]
FT3R4	FTPAD_TP	[27C8]
FT3R5	FTPAD_TP	[27B8]
FT3R6	FTPAD_TP	[27B8]
FT3R9	FTPAD_TP	[27A6]
FT3R10	FTPAD_TP	[22C1]
FT3R11	FTPAD_TP	[22C1]
FT3R12	FTPAD_TP	[27B1]
FT3R13	FTPAD_TP	[22C8]
FT3R14	FTPAD_TP	[22D7]
FT3R15	FTPAD_TP	[27D8]
FT3R16	FTPAD_TP	[4D2]
FT3R17	FTPAD_TP	[4C7]
FT3T1	FTPAD_TP	[52B5]
FT3T2	FTPAD_TP	[44D1]
FT3T3	FTPAD_TP	[44D8]
FT3T4	FTPAD_TP	[26B5]
FT3T5	FTPAD_TP	[26B5]
FT3T6	FTPAD_TP	[26B5]
FT3T7	FTPAD_TP	[26B5]
FT3T8	FTPAD_TP	[26A5]
FT3U1	FTPAD_TP	[49A1]
FT3V1	FTPAD_TP	[49B8]
FT3V2	FTPAD_TP	[50A1]
FT3V3	FTPAD_TP	[50C8]
FT3V4	FTPAD_TP	[49D2]
FT3V5	FTPAD_TP	[50D2]
FT3V6	FTPAD_TP	[35A2]
FT3V7	FTPAD_TP	[35A2]
FT4M1	FTPAD_TP	[40A7]
FT4M2	FTPAD_TP	[40C7]
FT4M3	FTPAD_TP	[40B7]
FT4M4	FTPAD_TP	[40B7]
FT4M5	FTPAD_TP	[40A7]
FT4M6	FTPAD_TP	[40B2]
FT4M7	FTPAD_TP	[40C7]
FT4M8	FTPAD_TP	[40B7]
FT4M9	FTPAD_TP	[40B7]
FT4N1	FTPAD_TP	[23A6]
FT4N2	FTPAD_TP	[23A6]
FT4P1	FTPAD_TP	[5B7]
FT4P2	FTPAD_TP	[5B7]
FT4P4	FTPAD_TP	[5C7]
FT4P5	FTPAD_TP	[5C7]
FT4P6	FTPAD_TP	[5C7]
FT4P7	FTPAD_TP	[5C7]
FT4P8	FTPAD_TP	[5C7]
FT4R2	FTPAD_TP	[2D6]
FT4R3	FTPAD_TP	[52A1]
FT4R4	FTPAD_TP	[3B4]
FT4R5	FTPAD_TP	[52A4]
FT4R6	FTPAD_TP	[3B4]
FT4R7	FTPAD_TP	[3B4]
FT4R8	FTPAD_TP	[3B4]
FT4R9	FTPAD_TP	[3B4]
FT4R10	FTPAD_TP	[27B6]
FT4T1	FTPAD_TP	[52D1]
FT4T2	FTPAD_TP	[2B8]
FT4T3	FTPAD_TP	[52B5]
FT5M1	FTPAD_TP	[53B3]
FT5M2	FTPAD_TP	[53B6]
FT5M3	FTPAD_TP	[53C7]
FT5N1	FTPAD_TP	[53C6]
FT5N2	FTPAD_TP	[53C3]
FT5P1	FTPAD_TP	[3C6]
FT5P2	FTPAD_TP	[3C6]
FT5R1	FTPAD_TP	[3A4]
FT5R2	FTPAD_TP	[3A4]
FT5R3	FTPAD_TP	[3A4]
FT5R4	FTPAD_TP	[3A4]
FT5R5	FTPAD_TP	[3A4]
FT5R6	FTPAD_TP	[3A4]
FT5R7	FTPAD_TP	[3A4]
FT5R8	FTPAD_TP	[3A4]
FT5R9	FTPAD_TP	[3A4]
FT5R10	FTPAD_TP	[3A4]
FT5R11	FTPAD_TP	[3A4]
FT5R12	FTPAD_TP	[3A4]
FT5R13	FTPAD_TP	[3A4]
FT5R14	FTPAD_TP	[3A4]
FT5R15	FTPAD_TP	[3A4]
FT5R16	FTPAD_TP	[3A4]
FT5R17	FTPAD_TP	[51C1]
FT5R18	FTPAD_TP	[2D6]
FT5T2	FTPAD_TP	[3D6]
FT5T4	FTPAD_TP	[49C1]
FT6M1	FTPAD_TP	[38A4]
FT6R1	FTPAD_TP	[43A3]
FT6R2	FTPAD_TP	[43A3]
FT6U1	FTPAD_TP	[50C2]
FT7N1	FTPAD_TP	[38A4]
FT7P1	FTPAD_TP	[44C5]
FT7P2	FTPAD_TP	[44B5]
FT7P3	FTPAD_TP	[2C2]
FT7P4	FTPAD_TP	[2C2]
FT7P5	FTPAD_TP	[2C2]
FT7P6	FTPAD_TP	[2C2]
FT7P7	FTPAD_TP	[2C2]
FT7P8	FTPAD_TP	[2C2]
J1A1	WAVERECEPTACLE_TH	[39B5]
J1A2	USBTRIPLE_TH	[39C1]
J1B1	1X7SATA_TH	[41A6]
J1B2	1X7SATA_TH	[41C5]
J1D1	1X6HDR_SMT	[41B1]
J1F1	1X2HDR_TH	[35A1]
J1G3	2X4HDR_TH	[58A3]

J2A1	TRINITYRJ45AUX_TH	[38B3]
J2C1	2X5HDR10_TH	[59C7]
J2C3	2X7HDR14_TH	[59C3]
J3A1	HDMI_1X19HDR	[40B2]
J3C1	2X3HDR_TH	[60C7]
J3G1	2X3HDR_TH	[60B7]
J4A1	TOSLINK_TX_TH	[39A5]
J4A2	XENONAVIP_TH	[37C5]
J4A3	2X6HDR2_TH	[41A2]
J4C1	2X4HDR_TH	[60D7]
J4C2	2X5HDR_TH	[60A6]
J4D1	2X3HDR_TH	[60C7]
J5A4	1X4HDR_TH	[36C2]
J5B1	2X2HDR_TH	[55C6]
J5B2	1X5HDR2_TH	[41D1]
J5G2	XENONRF_BORON_TH	[38A5]
J6G1	USBDUALHORIZONTAL_TH	[39C5]
J7A1	TRINITYPWR_TH	[38A1]
L1F1	INDUCTOR_TH	[48C3]
L2B1	INDUCTOR_TH	[47D8]
L2F1	INDUCTOR_TH	[47C4]
L4A1	INDUCTOR_1210	[37A4]
L4A2	INDUCTOR_1210	[37A4]
L4A3	INDUCTOR_1210	[37A7]
L4A4	INDUCTOR_1210	[37A7]
L4B1	INDUCTOR_TH	[51C5]
L4F1	INDUCTOR_TH	[49C3]
L5A1	INDUCTOR_1210	[53B4]
L5B2	INDUCTOR_1210	[53C4]
L5C1	INDUCTOR_TH	[51B3]
L6A1	INDUCTOR_1210	[53C8]
L6B1	INDUCTOR_TH	[43B5]
L6C1	IND_2MODE_SM	[45C1]
L6C2	IND_2MODE_TH	[45B1]
L7B1	INDUCTOR_TH	[49D8]
L7F1	INDUCTOR_TH	[50C3]
LB2B1	LABEL_SM	[62D5]
MTG1B1	STD_MTG_HOLE_TH	[62C6]
MTG1G1	STD_MTG_HOLE_TH	[62C6]
MTG4D1	STD_MTG_HOLE_TH	[62A6]
MTG4F1	STD_MTG_HOLE_TH	[62B6]
MTG4G1	STD_MTG_HOLE_TH	[62C5]
MTG6D1	STD_MTG_HOLE_TH	[62A4]
MTG6F1	STD_MTG_HOLE_TH	[62B4]
MTG7G1	STD_MTG_HOLE_TH	[62C3]
Q1F1	SHUNT_3PIN_SOT23	[56D3]
Q1N1	MBT3904DUAL_SOT	[46C5]
Q1N2	FET_SOT23	[35C7]
Q1N3	FET_SOT23	[35C7]
Q1T1	NPN_SOT23	[42B2]
Q1T2	NPN_SOT23	[42B2]
Q2F1	FET_VREG_DPAK	[47C4]
Q2F2	FET_VREG_DPAK	[47B4]
Q2F3	SHUNT_3PIN_SOT23	[56D7]
Q2N1	NPN_SOT23	[35C4]
Q3A1	MBT3904DUAL_SOT	[37C7]
Q3F1	FET_VREG_DPAK	[49C4]
Q3M1	PNP_SOT23	[37B7]
Q4A1	NPN_SOT23	[36C5]
Q4B1	ADR510_SOT23	[57A5]
Q4D1	NPN_SOT23	[60A3]
Q4D2	NPN_SOT23	[60A4]
Q4F1	FET_VREG_DPAK	[49B4]
Q4G1	PNP_SOT23	[23C1]
Q5A2	PNP_DPAK	[36C5]
Q5B1	FET_VREG_DPAK	[51C3]
Q5C1	FET_VREG_DPAK	[45A3]
Q5C2	FET_VREG_DPAK	[51B3]
Q5C3	FET_VREG_DPAK	[45A4]
Q6A1	NPN_SOT23	[42B6]
Q6A2	FET_SOT23	[42B6]
Q6B1	FET_VREG_DPAK	[45A4]
Q6B2	FET_VREG_DPAK	[45D4]
Q6C1	FET_VREG_DPAK	[45C3]
Q6C2	FET_VREG_DPAK	[45C4]
Q6M1	PNP_2C_SOT223	[42C4]
Q7G1	FET_VREG_DPAK	[50C4]
Q7G2	FET_VREG_DPAK	[50B4]
R1A1	RESN_402	[39B7]
R1C1	RESN_805	[52C6]
R1D1	RESN_1210	[52D7]
R1D2	RESN_1210	[52D8]
R1D3	RESN_1210	[52D8]
R1D4	RESN_1210	[52D8]
R1D5	RESN_402	[41C2]
R1D6	RESN_402	[41B2]
R1E12	RESN_402	[47C7]
R1E14	RESN_402	[48D5]
R1E15	RESN_402	[48C7]
R1E16	RESN_402	[48C7]
R1E17	RESN_402	[47B7]
R1E19	RESN_402	[48A3]
R1E20	RESN_402	[48A3]
R1E21	RESN_402	[48A7]
R1E22	RESN_402	[48D4]
R1F1	RESN_402	[48B5]
R1F2	RESN_402	[48B4]
R1F3	RESN_402	[47B4]
R1F4	RESN_402	[56A5]
R1F5	RESN_402	[56A4]
R1F6	RESN_402	[56A5]
R1F9	RESN_2512	[48C2]
R1G1	RESN_402	[58B3]
R1N1	RESN_402	[46C5]
R1N2	RESN_402	[46C6]
R1N3	RESN_402	[46C5]
R1N4	RESN_402	[35D6]
R1N5	RESN_402	[35D7]
R1P1	RESN_402	[46C6]
R1P2	RESN_402	[46B5]
R1T1	RESN_402	[42B3]
R1T2	RESN_402	[47C7]
R1T3	RESN_1206	[42C1]
R1T4	RESN_805	[47D8]
R1T5	RESN_402	[34C5]
R1T6	RESN_1206	[42C2]
R1T7	RESN_402	[42C2]
R1T8	RESN_402	[34B7]
R1T9	RESN_402	[34C6]
R1T10	RESN_402	[34C6]
R1T11	RESN_402	[34B7]
R1T12	RESN_402	[34B6]
R1T13	RESN_402	[34B6]
R1T14	RESN_402	[34C2]
R1T15	RESN_402	[34B6]
R1T16	RESN_402	[34B6]
R1T17	RESN_402	[34B5]
R1T18	RESN_402	[34B5]
R1T19	RESN_402	[56C3]
R1U3	RESN_402	[56C7]
R1U4	RESN_402	[56C7]
R1U5	RESN_402	[56D2]
R2A2	RESN_402	[38C7]
R2A3	RESN_402	[38C7]
R2A4	RESN_402	[38C7]
R2A5	RESN_402	[38B7]
R2B1	RESN_402	[55D7]
R2B2	RESN_402	[55C7]
R2B3	RESN_402	[55D7]
R2B4	RESN_402	[55D7]
R2C1	RESN_402	[27D3]
R2C3	RESN_402	[37C1]
R2C4	RESN_402	[59C2]
R2C5	RESN_402	[27C6]
R2C6	RESN_402	[59C4]
R2C7	RESN_402	[59C2]
R2C8	RESN_402	[28D3]
R2C9	RESN_402	[26C2]
R2C10	RESN_402	[41B2]
R2C11	RESN_402	[41B2]
R2D1	RESN_402	[32B6]
R2D2	RESN_402	[32B7]
R2D3	RESN_402	[32A6]
R2D4	RESN_402	[32C2]
R2D5	RESN_402	[29B2]
R2D6	RESN_402	[32C6]
R2D7	RESN_402	[29D6]
R2D8	RESN_402	[29D6]
R2D9	RESN_402	[29B2]
R2D10	RESN_402	[29B3]
R2D11	RESN_402	[29B2]
R2D12	RESN_402	[29B3]
R2D13	RESN_402	[29D3]
R2D14	RESN_402	[26B7]
R2D15	RESN_402	[26B8]
R2D16	RESN_402	[26B8]
R2D17	RESN_402	[26B8]
R2D18	RESN_402	[26B7]
R2D19	RESN_402	[26A5]
R2E1	RESN_402	[29A6]
R2E2	RESN_402	[47B8]
R2E3	RESN_402	[47B7]
R2E4	RESN_402	[47A3]
R2E5	RESN_402	[47A8]
R2E6	RESN_402	[47C4]
R2E7	RESN_402	[47C7]
R2E8	RESN_402	[26A5]
R2E9	RESN_402	[26A7]
R2F1	RESN_402	[47B5]
R2F2	RESN_402	[56C6]
R2F3	RESN_402	[56C6]
R2F4	RESN_402	[56A5]
R2F5	RESN_402	[56A4]
R2F7	RESN_805	[47A3]
R2F8	RESN_402	[56A4]
R2F9	RESN_805	[48B3]
R2G1	RESN_2512	[47C3]
R2G2	RESN_1206	[47B1]
R2G3	RESN_402	[26A3]
R2G4	RESN_402	[26A3]
R2G5	RESN_402	[26A3]
R2G21	RESN_402	[26A1]
R2N1	RESN_402	[37C2]
R2N2	RESN_402	[35C7]
R2N3	RESN_402	[35C7]
R2N4	RESN_402	[35D5]
R2N5	RESN_402	[35D6]
R2N6	RESN_402	[35D6]
R2N7	RESN_402	[35D4]
R2N8	RESN_402	[35C3]
R2R1	RESN_402	[32B6]
R2R2	RESN_402	[32C6]
R2R3	RESN_402	[32C6]
R2R4	RESN_402	[32A6]
R2R5	RESN_402	[32B6]
R2R6	RESN_402	[32A7]
R2R7	RESN_402	[32C2]
R2R8	RESN_402	[32A7]
R2R9	RESN_402	[32C3]
R2R10	RESN_402	[32C3]
R2R11	RESN_402	[32A2]
R2R12	RESN_402	[32C1]
R2R13	RESN_402	[32A2]
R2R14	RESN_402	[29B4]
R2R15	RESN_402	[32C2]
R2R16	RESN_402	[29B3]
R2R17	RESN_402	[29B4]
R2R18	RESN_402	[29B3]
R2R19	RESN_402	[26D7]
R2R20	RESN_402	[26B7]
R2R21	RESN_402	[26B8]
R2R22	RESN_402	[26B8]
R2R23	RESN_402	[26C7]
R2R24	RESN_402	[26B8]
R2R25	RESN_402	[26B7]
R2R26	RESN_402	[26A7]
R2T1	RESN_402	[28B6]

R2T2	RESN_402	[28A6]
R2T3	RESN_402	[47D5]
R2T4	RESN_402	[47A3]
R2T5	RESN_402	[56C6]
R2U1	RESN_402	[56D7]
R3A1	RESN_402	[37C7]
R3A2	RESN_402	[37C6]
R3A3	RESN_402	[37C8]
R3A4	RESN_402	[37C8]
R3A5	RESN_402	[37C7]
R3A6	RESN_603	[37C7]
R3A8	RESN_402	[33B3]
R3A9	RESN_402	[33B3]
R3A10	RESN_402	[33B2]
R3A11	RESN_402	[33B2]
R3B2	RESN_402	[23C3]
R3B3	RESN_402	[22D6]
R3B4	RESN_402	[23B6]
R3B5	RESN_603	[23B1]
R3B6	RESN_603	[23B1]
R3B7	RESN_603	[23B1]
R3B8	RESN_603	[23C1]
R3B9	RESN_402	[22D8]
R3B10	RESN_402	[22C7]
R3B11	RESN_402	[22C7]
R3B12	RESN_402	[22A3]
R3B13	RESN_402	[22A2]
R3B14	RESN_402	[22B2]
R3B15	RESN_402	[22A3]
R3B16	RESN_402	[22B2]
R3B17	RESN_402	[22B2]
R3B18	RESN_402	[22C2]
R3B19	RESN_402	[22C2]
R3B20	RESN_402	[22C2]
R3B21	RESN_402	[22C2]
R3B22	RESN_805	[33D6]
R3B24	RESN_402	[37A2]
R3C1	RESN_402	[22C2]
R3C2	RESN_402	[22C2]
R3C3	RESN_402	[22C2]
R3C4	RESN_402	[22D2]
R3C5	RESN_402	[22D2]
R3C6	RESN_402	[22D2]
R3C7	RESN_402	[22C2]
R3C8	RESN_402	[22D2]
R3C9	RESN_402	[22D2]
R3C10	RESN_402	[22D2]
R3C11	RESN_402	[22B3]
R3C12	RESN_402	[22B3]
R3C13	RESN_402	[22B2]
R3C14	RESN_402	[22B2]
R3D1	RESN_402	[27A7]
R3D2	RESN_402	[27A7]
R3D3	RESN_402	[26B7]
R3D4	RESN_402	[26B6]
R3D5	RESN_402	[26B7]
R3D7	RESN_402	[26A8]
R3D8	RESN_402	[26A7]
R3D9	RESN_402	[26A1]
R3D10	RESN_402	[26A1]
R3E1	RESN_402	[58C4]
R3E2	RESN_402	[58C5]
R3E3	RESN_402	[58C5]
R3E4	RESN_402	[58A7]
R3E5	RESN_805	[52B6]
R3F2	RESN_402	[58C5]
R3F3	RESN_402	[58C5]
R3F4	RESN_402	[52B6]
R3F5	RESN_402	[58C2]
R3F6	RESN_402	[49A7]
R3F7	RESN_402	[49B4]
R3F8	RESN_402	[49A3]
R3F9	RESN_402	[49A3]
R3F10	RESN_402	[49C4]
R3F11	RESN_805	[49B3]
R3F12	RESN_402	[49C7]
R3F13	RESN_402	[49C7]
R3F14	RESN_402	[49C7]
R3F15	RESN_402	[49B7]
R3F16	RESN_402	[55C2]
R3G1	RESN_402	[55A4]
R3G2	RESN_805	[49D7]
R3G4	RESN_402	[49B7]
R3G5	RESN_402	[50C7]
R3G6	RESN_402	[55A4]
R3G7	RESN_402	[55C5]
R3G8	RESN_402	[55C5]
R3G9	RESN_402	[55C5]
R3G10	RESN_402	[50B5]
R3G11	RESN_402	[50A3]
R3G12	RESN_402	[50A3]
R3G13	RESN_402	[50C4]
R3G14	RESN_402	[50B8]
R3G15	RESN_402	[50D5]
R3G16	RESN_402	[49D5]
R3G17	RESN_805	[50A3]
R3G18	RESN_402	[26A7]
R3G19	RESN_402	[26A7]
R3G20	RESN_402	[26A5]
R3M1	RESN_402	[27B6]
R3M2	RESN_402	[37B7]
R3M3	RESN_402	[37B7]
R3M6	RESN_402	[33B5]
R3M7	RESN_402	[37B6]
R3N3	RESN_402	[23B6]
R3N4	RESN_402	[23B6]
R3N5	RESN_402	[22B4]
R3N6	RESN_402	[24B6]
R3N7	RESN_402	[22C8]
R3N8	RESN_402	[22C7]
R3P1	RESN_402	[22C7]
R3R1	RESN_402	[37C2]
R3R2	RESN_402	[37C2]
R3R3	RESN_402	[27B6]
R3R4	RESN_402	[27B6]
R3R5	RESN_402	[50D3]
R3R6	RESN_402	[27C6]
R3R7	RESN_402	[26B7]
R3R8	RESN_402	[26B6]
R3R9	RESN_402	[26B7]
R3R11	RESN_402	[35B6]
R3R13	RESN_402	[59C2]
R3R14	RESN_402	[26D8]
R3R15	RESN_402	[22D4]
R3R16	RESN_402	[22D4]
R3R17	RESN_402	[27B6]
R3R18	RESN_402	[27B6]
R3R19	RESN_402	[27C2]
R3R20	RESN_402	[27B2]
R3R21	RESN_402	[27B3]
R3R22	RESN_402	[26C7]
R3R23	RESN_402	[27B2]
R3R24	RESN_402	[26C8]
R3T1	RESN_805	[31D7]
R3T2	RESN_402	[27A3]
R3T3	RESN_402	[27A2]
R3T4	RESN_402	[26D8]
R3T5	RESN_402	[52C2]
R3U1	RESN_402	[55C5]
R3U2	RESN_402	[58A8]
R3U3	RESN_402	[55C5]
R3V1	RESN_402	[49B4]
R3V4	RESN_402	[50A7]
R3V5	RESN_402	[38A7]
R3V6	RESN_402	[38B6]
R4A1	RESN_402	[36C5]
R4A2	RESN_402	[37A5]
R4A3	RESN_402	[37A5]
R4A4	RESN_402	[37A7]
R4A5	RESN_402	[37A7]
R4A6	RESN_402	[41A3]
R4A7	RESN_402	[36C5]
R4B1	RESN_402	[57B7]
R4B2	RESN_402	[57C5]
R4B3	RESN_402	[57B5]
R4B4	RESN_805	[51C4]
R4B6	RESN_402	[22D5]
R4B7	RESN_402	[22D6]
R4B8	RESN_402	[23D2]
R4B9	RESN_402	[23D2]
R4B10	RESN_402	[23C6]
R4B11	RESN_402	[51B6]
R4B12	RESN_402	[23D3]
R4B13	RESN_402	[23D3]
R4B14	RESN_402	[23A3]
R4B15	RESN_402	[23A7]
R4B16	RESN_402	[22D7]
R4B17	RESN_402	[51B4]
R4B18	RESN_402	[57A3]
R4B19	RESN_402	[51A5]
R4B20	RESN_402	[37A2]
R4B21	RESN_402	[51C7]
R4B22	RESN_402	[51A5]
R4C1	RESN_402	[23A7]
R4C2	RESN_402	[23A5]
R4C3	RESN_402	[5C6]
R4C4	RESN_402	[60A4]
R4C5	RESN_402	[5B7]
R4C6	RESN_402	[60A5]
R4C7	RESN_402	[60A4]
R4C8	RESN_402	[5B7]
R4C9	RESN_402	[60A4]
R4C10	RESN_402	[60A6]
R4C11	RESN_402	[51B7]
R4C13	RESN_402	[51C7]
R4C14	RESN_402	[51B7]
R4C17	RESN_402	[51B6]
R4D1	RESN_402	[2C6]
R4D2	RESN_402	[2C6]
R4D3	RESN_402	[60B4]
R4D4	RESN_402	[2D4]
R4D5	RESN_402	[2D4]
R4E1	RESN_402	[4D7]
R4E2	RESN_402	[4D7]
R4E3	RESN_402	[60A3]
R4E4	RESN_805	[52B6]
R4E5	RESN_402	[52B6]
R4E6	RESN_402	[52B7]
R4E7	RESN_402	[52C2]
R4E8	RESN_402	[52C3]
R4E9	RESN_402	[52C3]
R4E10	RESN_402	[52C2]
R4E11	RESN_805	[52D2]
R4F1	RESN_2512	[49C2]
R4F2	RESN_402	[52A7]
R4G3	RESN_402	[50B4]
R4G4	RESN_402	[38B6]
R4G5	RESN_402	[38B7]
R4G6	RESN_402	[38A7]
R4G7	RESN_402	[38A7]
R4M1	RESN_402	[40A6]
R4M2	RESN_402	[40A7]
R4M5	RESN_402	[40A3]
R4M6	RESN_402	[40A2]
R4N1	RESN_402	[57B5]
R4N2	RESN_402	[57A7]
R4N3	RESN_402	[57A7]
R4N4	RESN_402	[57A6]
R4N5	RESN_402	[57A6]
R4N6	RESN_402	[57A6]
R4N7	RESN_402	[57A6]
R4N8	RESN_402	[57D4]
R4N10	RESN_402	[57C4]
R4N13	RESN_402	[57D4]
R4N14	RESN_402	[57C4]
R4N15	RESN_805	[51B4]
R4P1	RESN_402	[61C4]
R4P2	RESN_402	[61C5]

R4P3	RESN_402	[61B4]
R4P4	RESN_402	[61B4]
R4P5	RESN_402	[61B5]
R4P6	RESN_402	[61B5]
R4P9	RESN_402	[5C7]
R4R1	RESN_402	[52A3]
R4R2	RESN_402	[5C4]
R4R3	RESN_402	[3C3]
R4R4	RESN_805	[52A1]
R4R5	RESN_402	[3C3]
R4R6	RESN_402	[3C3]
R4R7	RESN_402	[5C4]
R4R8	RESN_402	[3C3]
R4R9	RESN_402	[5C4]
R4R10	RESN_402	[5B3]
R4R11	RESN_402	[5C4]
R4R12	RESN_402	[5C3]
R4R13	RESN_402	[3C2]
R4T5	RESN_402	[2B8]
R4T6	RESN_402	[2B8]
R4U4	RESN_402	[52B6]
R4V1	RESN_402	[38A7]
R4V2	RESN_402	[38A7]
R5A3	RESN_402	[36C2]
R5A5	RESN_402	[53B5]
R5A6	RESN_402	[53B4]
R5A7	RESN_402	[53B6]
R5A9	RESN_805	[36C3]
R5A10	RESN_402	[36A3]
R5A11	RESN_805	[53B3]
R5B2	RESN_402	[53C5]
R5B3	RESN_402	[53C6]
R5B4	RESN_805	[53C3]
R5B5	RESN_402	[53C6]
R5B6	RESN_402	[57B4]
R5B13	RESN_805	[51B3]
R5B17	RESN_402	[53C4]
R5C1	RESN_805	[45A2]
R5C2	RESN_2512	[51B2]
R5F1	RESN_402	[19A7]
R5F2	RESN_402	[19A7]
R5F3	RESN_402	[18D7]
R5F4	RESN_402	[18D7]
R5F5	RESN_402	[18A5]
R5G1	RESN_402	[35D2]
R5G2	RESN_402	[35D2]
R5M1	RESN_805	[42B5]
R5M2	RESN_805	[42B5]
R5M3	RESN_402	[36B5]
R5M4	RESN_402	[36B5]
R5M5	RESN_402	[36B5]
R5M6	RESN_402	[53B6]
R5N2	RESN_402	[57C5]
R5N7	RESN_805	[45B7]
R5N8	RESN_805	[45A5]
R5R1	RESN_402	[2A6]
R5T1	RESN_402	[4C6]
R5T2	RESN_402	[13A7]
R5T3	RESN_402	[13A7]
R5T4	RESN_402	[13A3]
R5T5	RESN_402	[13A3]
R5T6	RESN_402	[13B5]
R5T7	RESN_402	[13B5]
R5U1	RESN_402	[19A5]
R5U2	RESN_402	[19D7]
R5U3	RESN_402	[19D7]
R5U4	RESN_402	[18A7]
R5U5	RESN_402	[18A7]
R5U6	RESN_402	[4A4]
R6A3	RESN_402	[42B7]
R6A4	RESN_402	[42B7]
R6A5	RESN_402	[38A3]
R6A6	RESN_402	[38A2]
R6A7	RESN_402	[42C6]
R6A8	RESN_402	[42C6]
R6A9	RESN_402	[42C5]
R6A10	RESN_402	[58D7]
R6A11	RESN_402	[58C7]
R6C1	RESN_805	[45C3]
R6C2	THERMISTOR_603	[44C6]
R6F1	RESN_402	[21A8]
R6F2	RESN_402	[21A8]
R6F3	RESN_402	[20D7]
R6F4	RESN_402	[20D7]
R6F5	RESN_402	[20A5]
R6F6	RESN_402	[4A3]
R6G1	RESN_402	[35C6]
R6M1	RESN_805	[42B4]
R6M2	RESN_805	[42B5]
R6M3	RESN_402	[58C6]
R6M4	RESN_402	[58C7]
R6N1	RESN_805	[45D7]
R6N2	RESN_805	[45D5]
R6R1	RESN_402	[12B1]
R6R2	RESN_402	[12B1]
R6T1	RESN_402	[12A3]
R6T2	RESN_402	[12A3]
R6T3	RESN_402	[4A6]
R6T4	RESN_402	[12A7]
R6T5	RESN_402	[12A7]
R6T6	RESN_402	[4A6]
R6T7	RESN_402	[12B5]
R6T8	RESN_402	[12B5]
R6T9	RESN_402	[13B1]
R6U1	RESN_402	[21A5]
R6U2	RESN_402	[21D7]
R6U3	RESN_402	[21D7]
R6U4	RESN_402	[20A8]
R6U5	RESN_402	[20A8]
R7A1	RESN_2512	[38B2]
R7A2	RESN_2512	[38A2]
R7B1	RESN_402	[44B6]
R7B2	RESN_402	[44B6]
R7B3	RESN_402	[44B7]
R7B4	RESN_402	[44B7]
R7B5	RESN_402	[44D6]
R7C1	RESN_402	[44B4]
R7C2	RESN_402	[44A7]
R7C3	RESN_402	[44A5]
R7C4	RESN_402	[44D5]
R7C5	RESN_402	[44B2]
R7C6	RESN_402	[44B4]
R7C7	RESN_402	[44C6]
R7C8	RESN_402	[44B1]
R7C9	RESN_402	[44C6]
R7C10	RESN_402	[44D6]
R7C11	RESN_603	[44D6]
R7C12	RESN_603	[44D6]
R7C13	RESN_402	[44D2]
R7C14	RESN_805	[44A7]
R7C15	RESN_402	[43C5]
R7C16	RESN_402	[43C5]
R7C17	RESN_402	[43C4]
R7C18	RESN_402	[43C4]
R7C19	RESN_402	[43C4]
R7C20	RESN_402	[43C3]
R7D2	RESN_402	[16D7]
R7D3	RESN_402	[16D7]
R7D4	RESN_402	[17A7]
R7D5	RESN_402	[17A7]
R7E1	RESN_402	[16A5]
R7E2	RESN_402	[4A2]
R7E4	RESN_402	[14D7]
R7E5	RESN_402	[14D7]
R7E6	RESN_402	[15A8]
R7E7	RESN_402	[15A8]
R7E8	RESN_402	[14A5]
R7F1	RESN_2512	[50C2]
R7P1	RESN_402	[44A7]
R7P2	RESN_402	[44A6]
R7P3	RESN_402	[43D6]
R7P4	RESN_402	[43D6]
R7P5	RESN_402	[43D6]
R7P6	RESN_402	[43D6]
R7P7	RESN_402	[43D6]
R7P8	RESN_402	[43C6]
R7R1	RESN_402	[17D7]
R7R2	RESN_402	[16A8]
R7R3	RESN_402	[17D7]
R7R4	RESN_402	[16A8]
R7R6	RESN_402	[4A3]
R7T1	RESN_402	[17A5]
R7T2	RESN_402	[15D7]
R7T3	RESN_402	[15D7]
R7T4	RESN_402	[14A7]
R7T5	RESN_402	[14A7]
R7T6	RESN_402	[15A5]
R7T7	RESN_402	[4A3]
RT1B1	THERMISTOR_1206	[38D6]
RT1M1	THERMISTOR_1206	[39B3]
RT1M2	THERMISTOR_1206	[39C3]
RT2M1	THERMISTOR_1206	[39D3]
RT3A1	THERMISTOR_1206	[37D7]
RT3A2	THERMISTOR_1206	[38D6]
RT5A1	THERMISTOR_1206	[41D3]
RT6G1	THERMISTOR_1206	[39D8]
RT7V1	THERMISTOR_1206	[39C8]
ST1F1	SHORT_SM	[48C2]
ST1F2	SHORT_SM	[48B2]
ST1F3	SHORT_SM	[48C2]
ST1U1	SHORT_SM	[48B4]
ST1U2	SHORT_SM	[48C4]
ST2G1	SHORT_SM	[47B3]
ST2G2	SHORT_SM	[47C2]
ST2G3	SHORT_SM	[47C2]
ST2R1	SHORT_SM	[31B7]
ST2R2	SHORT_SM	[31B7]
ST2T1	SHORT_SM	[31A7]
ST2T2	SHORT_SM	[30C8]
ST2U1	SHORT_SM	[47C4]
ST2U2	SHORT_SM	[47B4]
ST3C1	SHORT_SM	[23A6]
ST3C2	SHORT_SM	[23A6]
ST3C3	SHORT_SM	[23A6]
ST3C4	SHORT_SM	[23A6]
ST3C5	SHORT_SM	[23A6]
ST3F1	SHORT_SM	[49C4]
ST3R1	SHORT_SM	[31D7]
ST3T1	SHORT_SM	[30D7]
ST3T2	SHORT_SM	[30A7]
ST4F1	SHORT_TRACE	[49B2]
ST4F2	SHORT_SM	[49C2]
ST4F4	SHORT_SM	[49C2]
ST4U1	SHORT_TRACE	[49B4]
ST5C1	SHORT_SM	[51C2]
ST5C2	SHORT_TRACE	[51B3]
ST5C3	SHORT_SM	[51C2]
ST5R1	SHORT_SM	[6C6]
ST5R2	SHORT_SM	[6C6]
ST5R3	SHORT_SM	[6A6]
ST5R4	SHORT_SM	[6A6]
ST5R5	SHORT_SM	[6B6]
ST5T1	SHORT_SM	[6C6]
ST5T2	SHORT_SM	[6B6]
ST6C1	SHORT_SM	[44B8]
ST6D1	SHORT_SM	[44A8]
ST6D2	SHORT_SM	[44A5]
ST6V1	SHORT_TRACE	[50B4]
ST6V2	SHORT_TRACE	[50C4]
ST7A1	SHORT_SM	[38B2]
ST7A2	SHORT_SM	[38B2]
ST7F1	SHORT_SM	[50B2]
ST7F2	SHORT_SM	[50C2]
ST7F3	SHORT_SM	[50C2]
STP3C1	STP_TP	[61B1]
STP4C1	STP_TP	[61C4]
STP4C2	STP_TP	[61B4]
STP4C3	STP_TP	[61C5]

STP4C4	STP_TP	[61B4]
STP4C5	STP_TP	[61B5]
STP4C6	STP_TP	[61B5]
STP4E1	STP_TP	[61B7]
STP4E2	STP_TP	[61B7]
STP4E3	STP_TP	[61A8]
STP5B1	STP_TP	[61B1]
STP5B2	STP_TP	[61B1]
STP5D1	STP_TP	[61C7]
STP5D2	STP_TP	[61C7]
STP6C1	STP_TP	[61B7]
STP6C2	STP_TP	[61A7]
STP7B1	STP_TP	[61B1]
STP7C1	STP_TP	[61B1]
STP7C2	STP_TP	[61C1]
STP7C3	STP_TP	[61C1]
STP7C4	STP_TP	[61C1]
STP7C5	STP_TP	[61C1]
STP7C6	STP_TP	[61C1]
STP7C7	STP_TP	[61C1]
STP7E1	STP_TP	[61C7]
STP7E2	STP_TP	[61C7]
STP7N1	STP_TP	[61B1]
U1B1	SI4501DY_SO8	[46C3]
U1C1	NCP1117_DPAK	[52C7]
U1E1	ADP1877_LCC32	[47A6]
U1E1	ADP1877_LCC32	[48A7]
U1E2	NAND_TSOP	[34B3]
U1F1	FET_VREG_DUAL_1_SO-8	[48C4]
U1F2	AD7991_SOT23	[56B3]
U1F3	REF3333_SC70	[56B3]
U1F5	TRSET_9920_TH	[35B1]
U1G2	LM95234_LLP-14	[58B2]
U1G3	TRSET_9920_SMT	[35B1]
U1U1	AD5252_TSSOP	[56C5]
U2D1	ETHERNETPHY_KSZ8041NL_AR8032_QFN	[32A5]
U2N1	BMAX20_LGA12	[35C5]
U2U1	AD8213_MSOP10	[56B5]
U3A5	AUDIODAC_CSS4354_WM1824_QFN25	[33A5]
U3B2	HANA_BGA225	[22C5]
U3B2	HANA_BGA225	[23C4]
U3B2	HANA_BGA225	[24C4]
U3B2	HANA_BGA225	[25B4]
U3D1	SB_BGA	[26C4]
U3D1	SB_BGA	[27C5]
U3D1	SB_BGA	[28C5]
U3D1	SB_BGA	[29C5]
U3D1	SB_BGA	[30C4]
U3D1	SB_BGA	[31B5]
U3E1	AD7992_MSOP10	[58A6]
U3E2	AD5252_TSSOP	[58C4]
U3G1	ADP1877_LCC32	[49A6]
U3G1	ADP1877_LCC32	[50A7]
U3G2	AD7991_SOT23	[55A3]
U3G3	REF3333_SC70	[55B4]
U3G4	ISD2130_QFN21	[35A4]
U3T1	REF3333_SC70	[58B7]
U3V1	AD5252_TSSOP	[55C4]
U3V2	AD8213_MSOP10	[55A5]
U4B1	AD5252_TSSOP	[57A5]
U4B2	AD7992_MSOP10	[57D3]
U4B3	IR3638_SSOP	[51B5]
U4E1	NCP1117_DPAK	[52B7]
U4E2	NCP1117_SOT223	[52D3]
U4R1	LD39015_SOT23-5	[52A3]
U4R2	AT25020A_SOI8	[5C2]
U5A1	SIMPLESWR_SOT23	[53B5]
U5B1	SIMPLESWR_SOT23	[53C5]
U5B2	AD8213_MSOP10	[57C6]
U5B5	MOSDRIVER_SOI8	[45A6]
U5B6	REF3333_SC70	[57D6]
U5E1	VALHALLA_1_BGA_2	[2C4]
U5E1	VALHALLA_1_BGA_2	[3C5]
U5E1	VALHALLA_1_BGA_2	[4A5]
U5E1	VALHALLA_1_BGA_2	[5C5]
U5E1	VALHALLA_1_BGA_2	[6C3]
U5E1	VALHALLA_1_BGA_2	[7B6 7A8 7C8 7B4 7B1]
U5E1	VALHALLA_1_BGA_2	[8B2 8B4 8B7]
U5E1	VALHALLA_1_BGA_2	[12C3 12C7]
U5E1	VALHALLA_1_BGA_2	[13C6 13C3]
U5F1	GDDR136_1GBIT_BGA136	[18C2 18C6]
U5N1	AD7992_MSOP10	[57C4]
U5U1	GDDR136_1GBIT_BGA136	[19C6 19C2]
U5U2	74LVC1G06_SC70	[4A3]
U6A1	INA219_SOT23-8	[58C6]
U6B1	MOSDRIVER_SOI8	[45C6]
U6F1	GDDR136_1GBIT_BGA136	[20C6 20C2]
U6G1	IR_WHOLDER_TH	[35B7]
U6U1	GDDR136_1GBIT_BGA136	[21C6 21C2]
U7C1	NCP4201_LCC40	[44C3]
U7D1	GDDR136_1GBIT_BGA136	[16C2 16B6]
U7E1	GDDR136_1GBIT_BGA136	[14C2 14C6]
U7R1	GDDR136_1GBIT_BGA136	[17B6 17C2]
U7T1	GDDR136_1GBIT_BGA136	[15C6 15C2]
Y3B1	CRYSTAL_SM	[22D8]