

CACTUS

REV 0.991

FAB G RETAIL

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- RULES: (APPLIED WHEN POSSIBLE)
1. MSB TO LSB IS TOP TO BOTTOM
 2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
 3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
 4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
 5. LANED SIGNALS ARE GROUPED ON SYMBOLS
 6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
 7. SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
 8. SUFFIX DP AND DN ARE USED FOR DIFFERENTIAL PAIRS
 9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
 10. SUFFIX N FOR ACTIVE LOW OR N JUNCTION
 12. SUFFIX P FOR P JUNCTION
 13. SUFFIX EN FOR ENABLE
 14. 'CLK' FOR CLOCKS, 'RST' FOR RESETS
 15. PWRGD FOR POWER GOOD
 16. REV AND FAB ARE SET USING CUSTOM VARIABLES
- TOOLS>OPTIONS>VARIABLES

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DRAWING
Thu Apr 20 16:18:47 2017

D

C

B

A

D

C

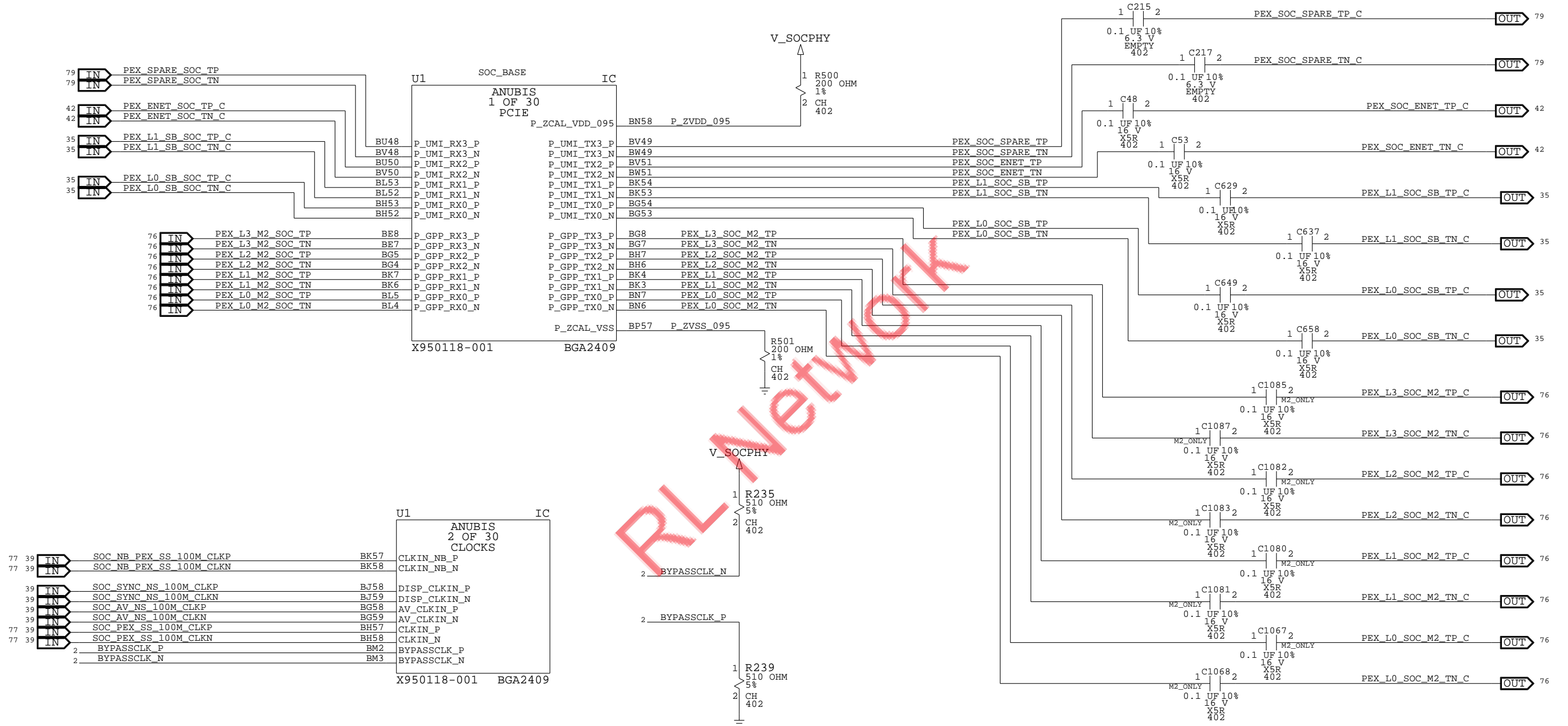
B

A

SOC:PCIEX, CLOCKS

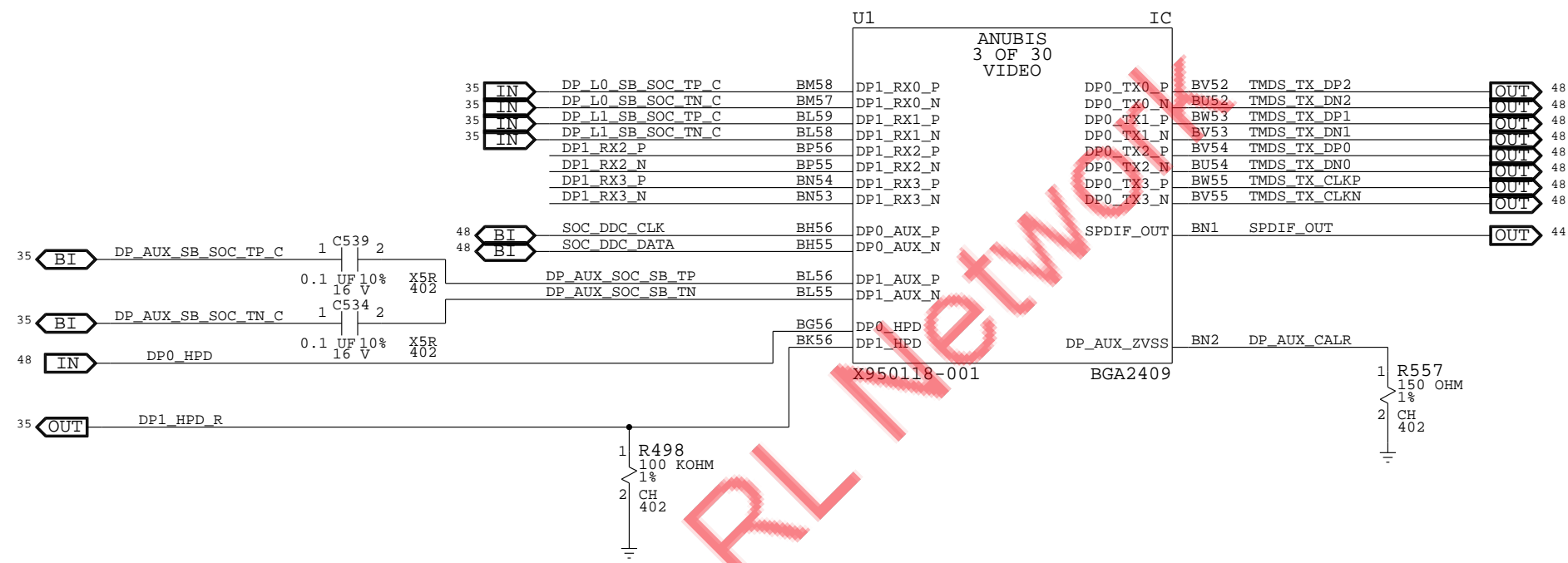
NOTES:

- 1.TO SUPPORT PCIE SPARE LANE INTERFACE (J28) , POPULATE C215 AND C217
- 2.SEE PAGES 77 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION



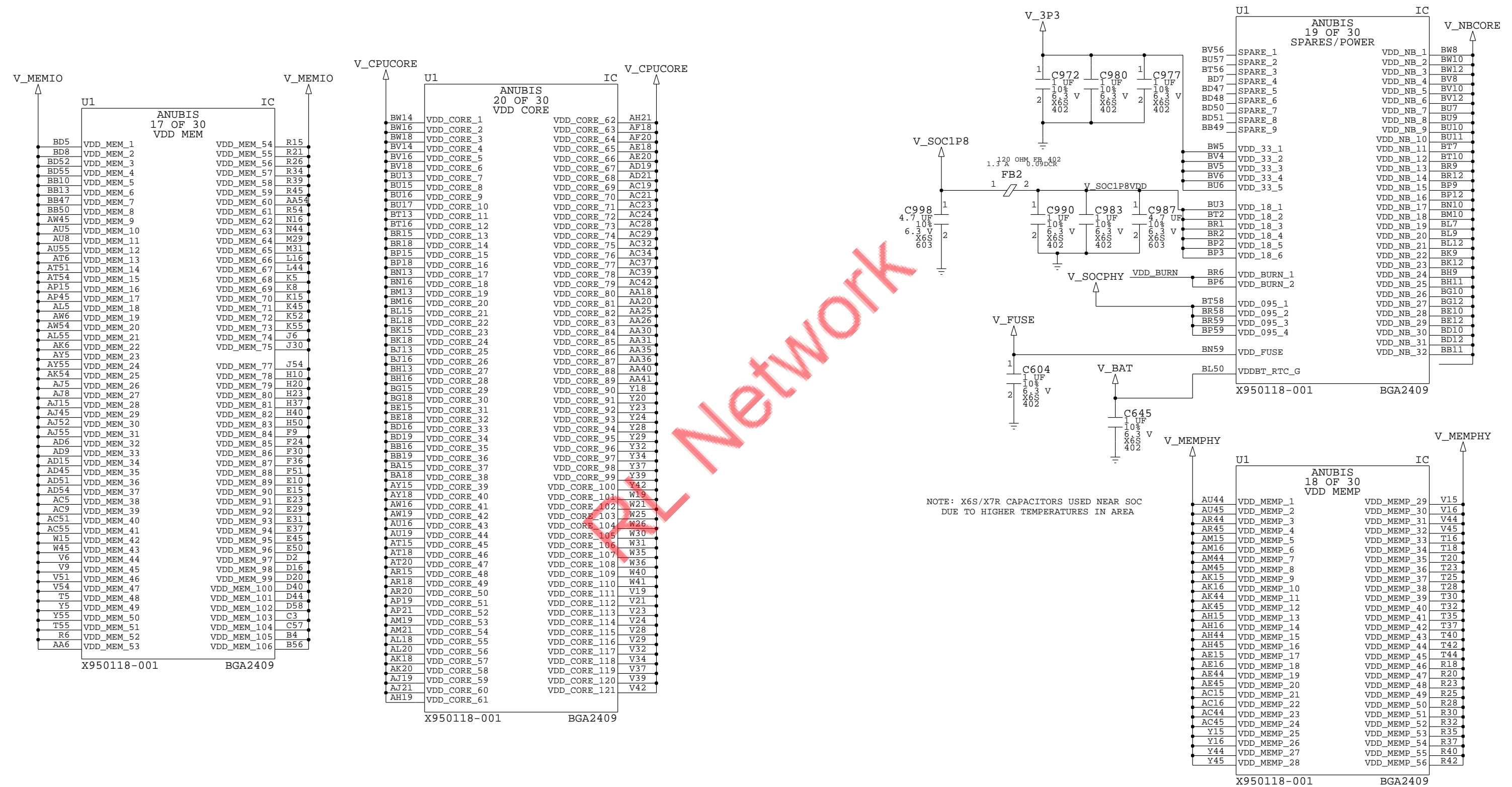
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X950118-001	IC	U1	PROCSR-CPU-GPU_SM,1.0GHZ,BGA2049,ANUBIS	SOC_INCLUDE
X950118-001	EMPTY	U1	PROCSR-CPU-GPU_SM,1.0GHZ,BGA2049,ANUBIS	SOC_EMPTY

SOC: VIDEO

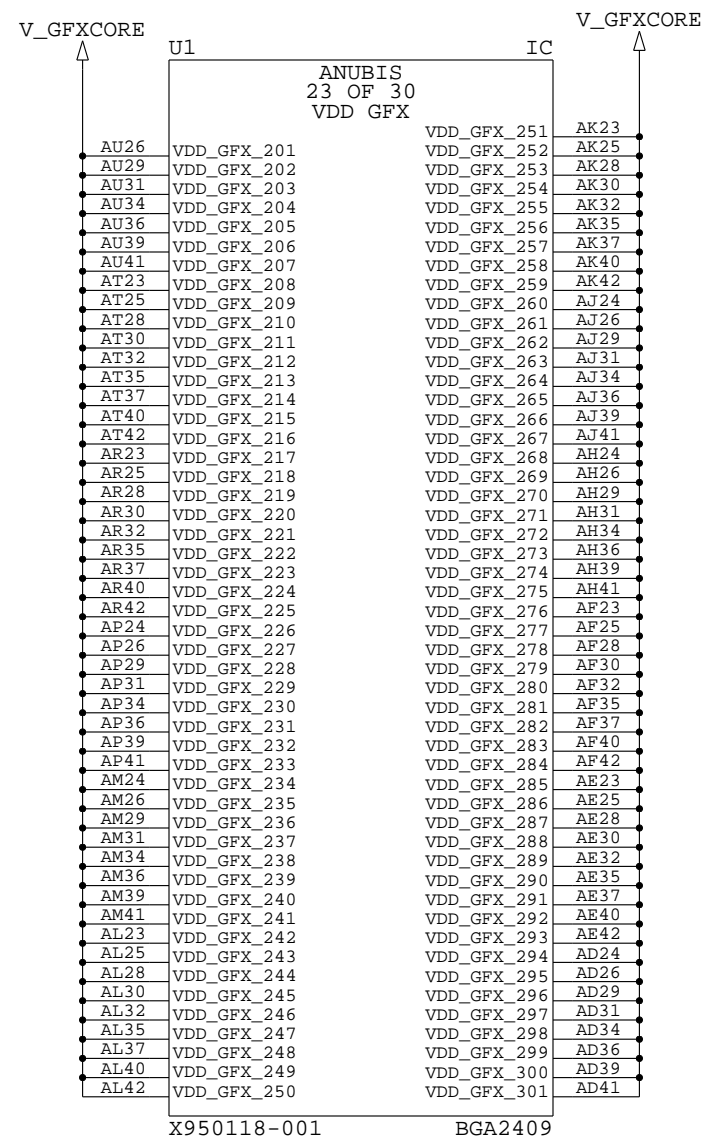
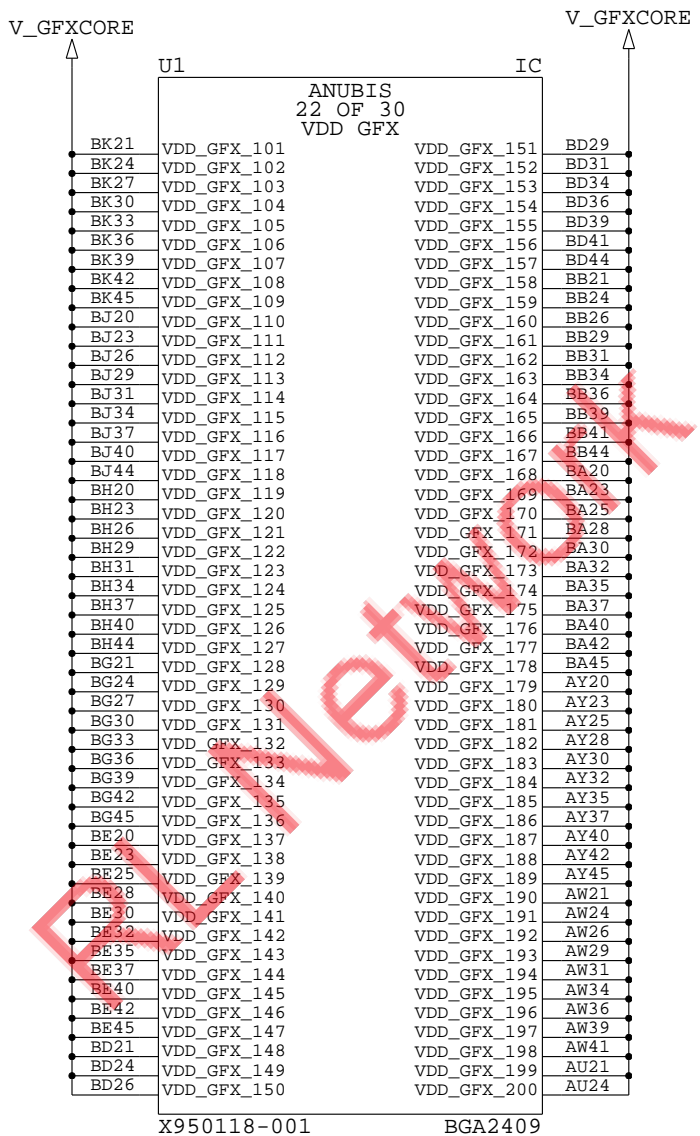
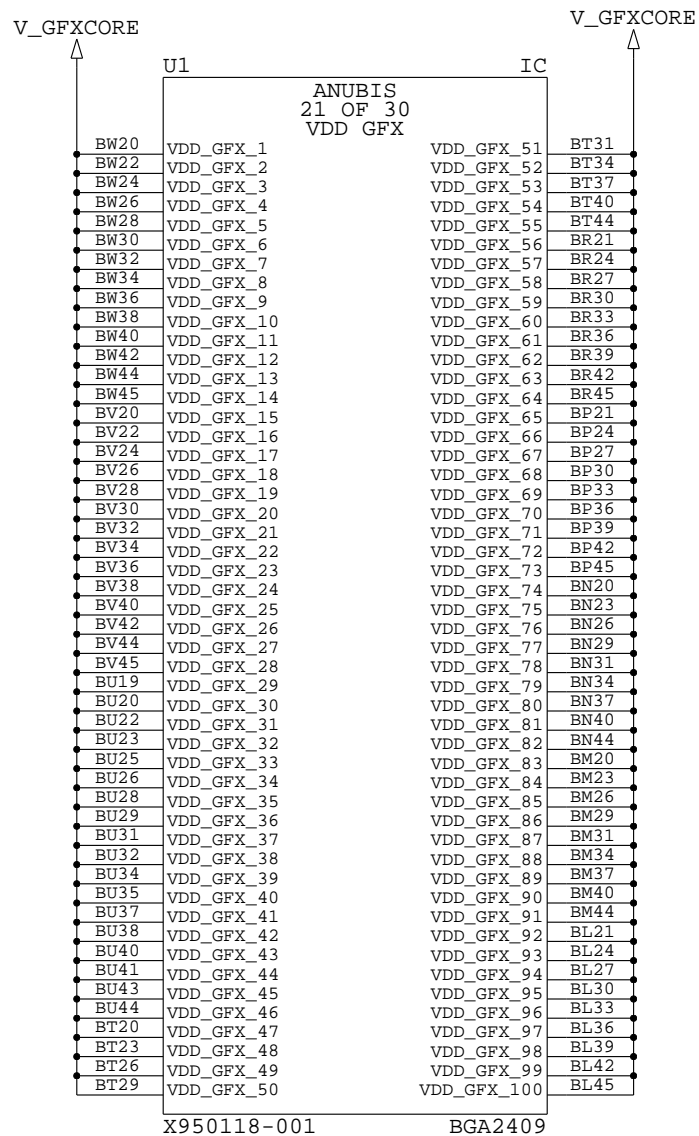


DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

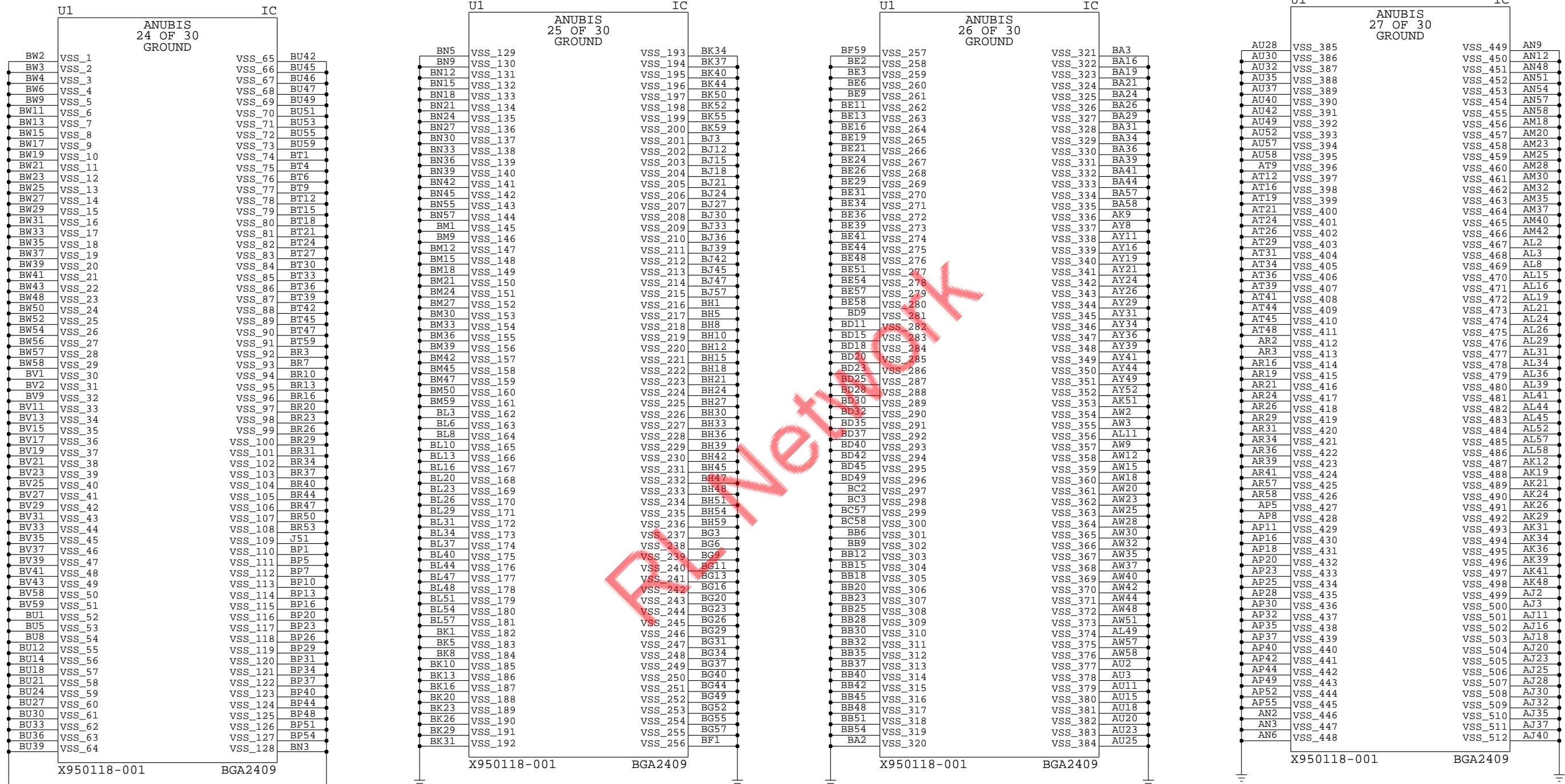
SOC : POWER : MEMIO , MEMPHY , CPUCORE , NBCORE , MISC



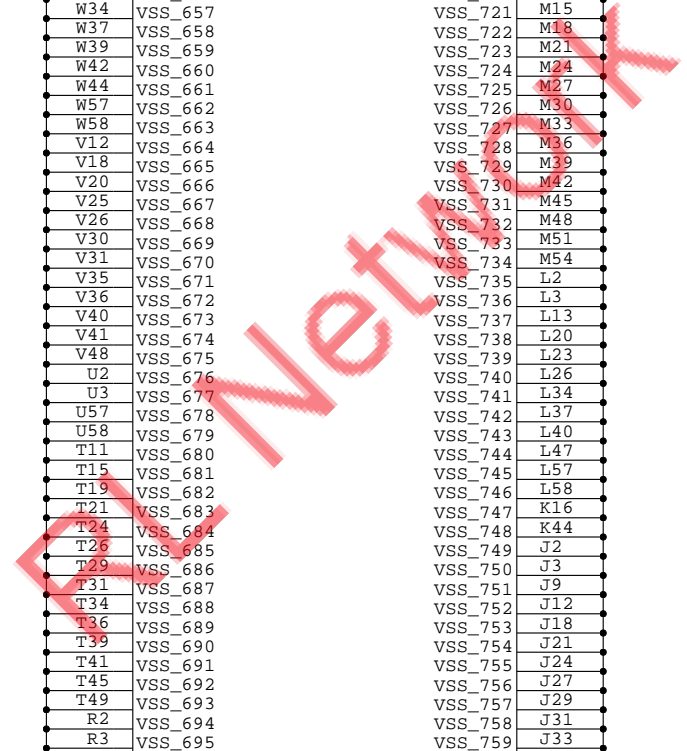
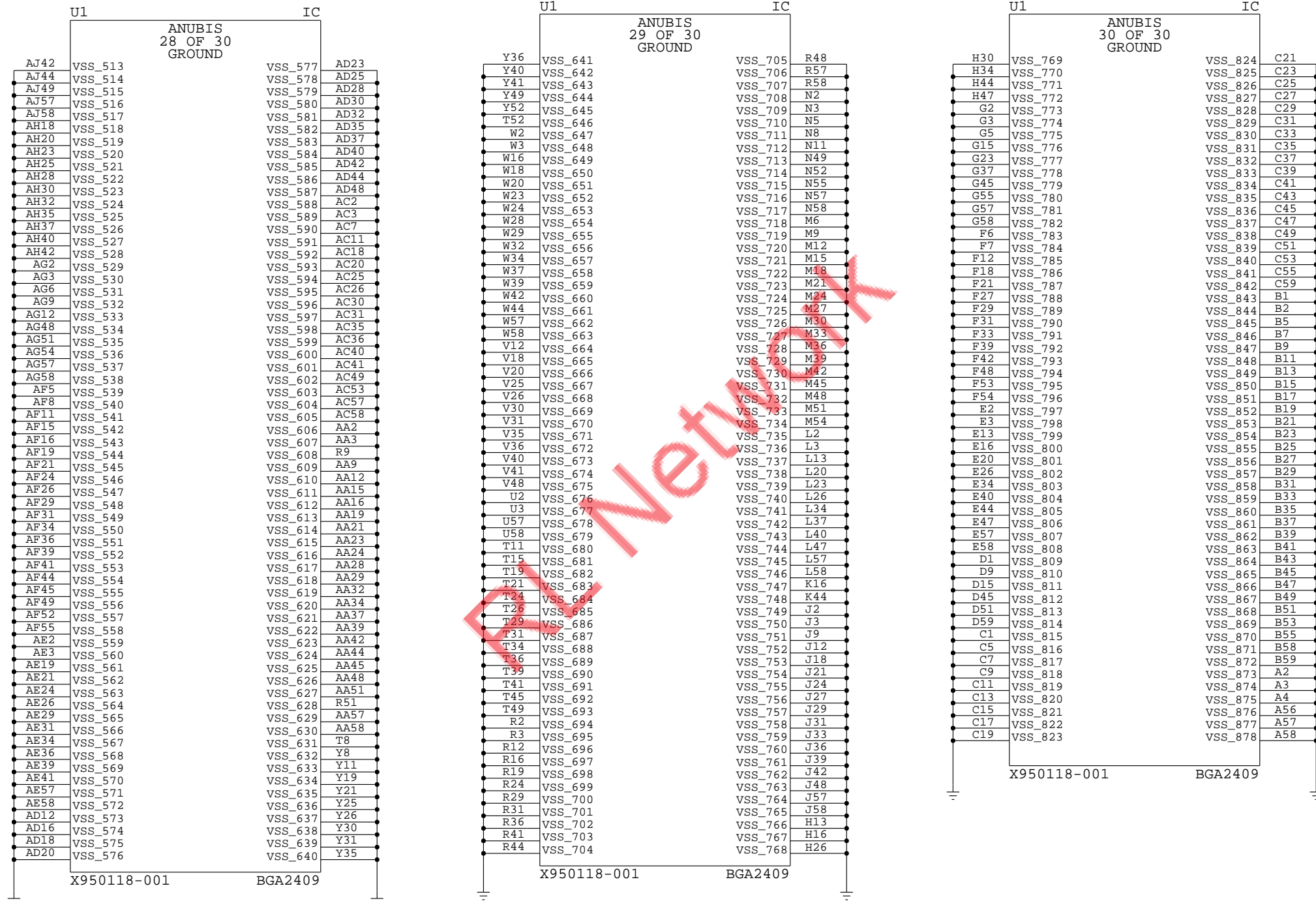
SOC: POWER: GFXCORE



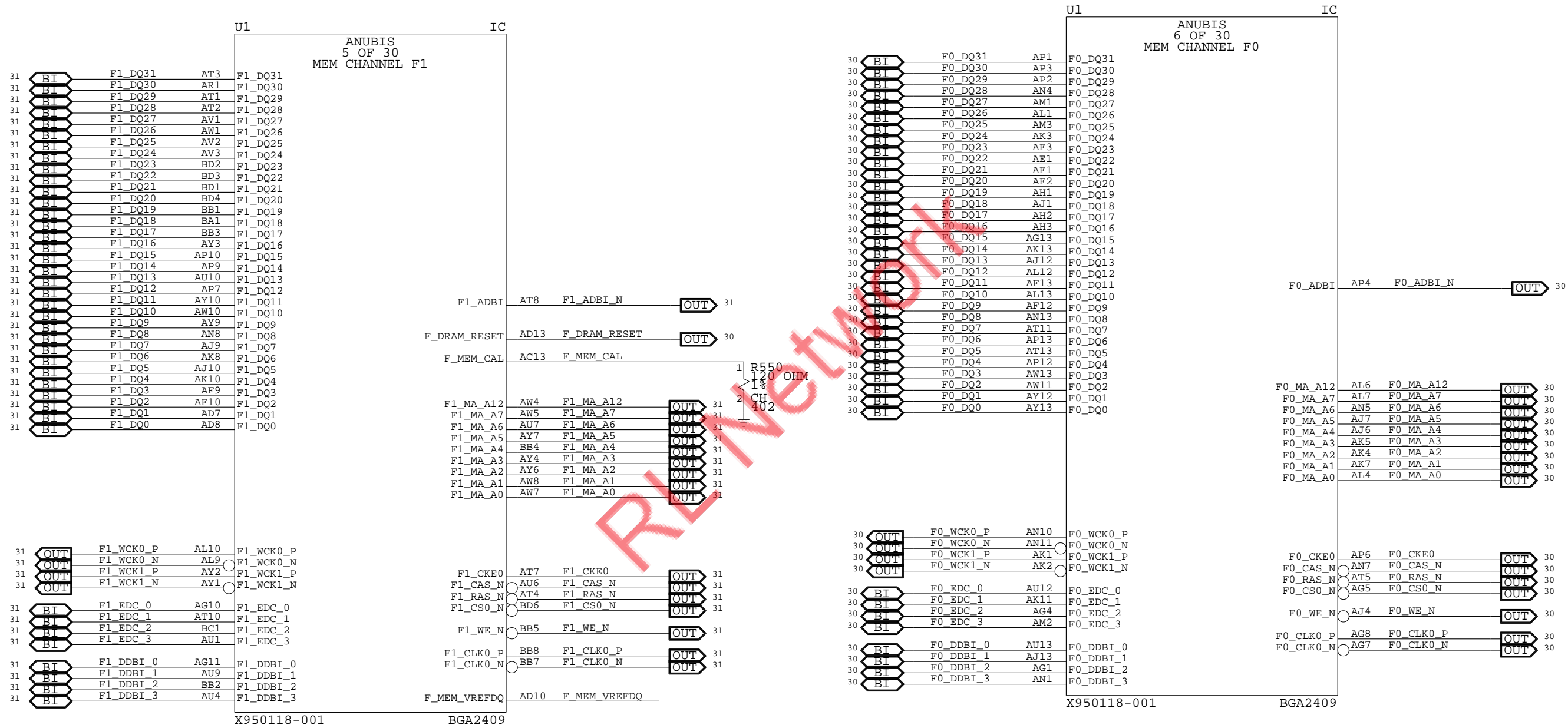
SOC: POWER: VSS



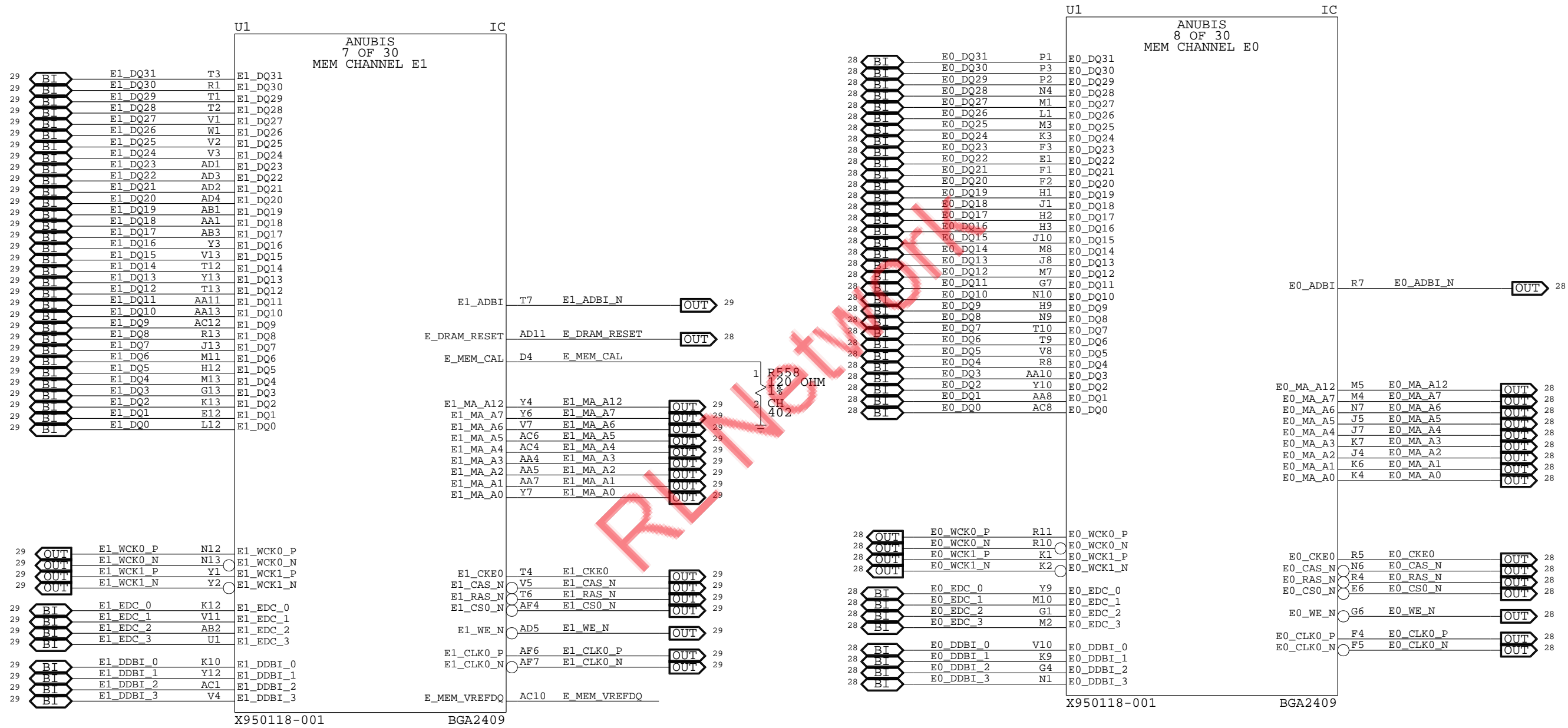
SOC : POWER : VSS



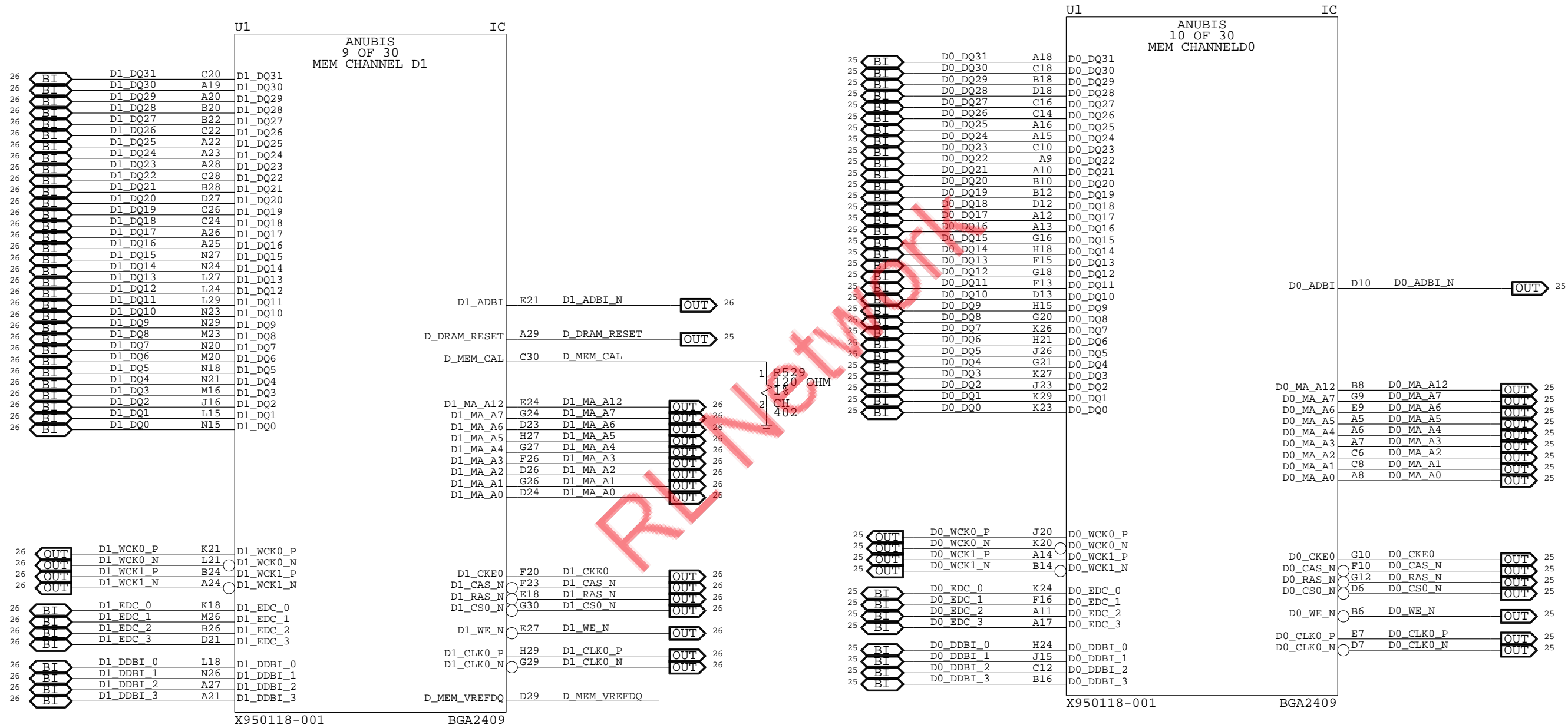
MEMORY: PARTITION F1/F0



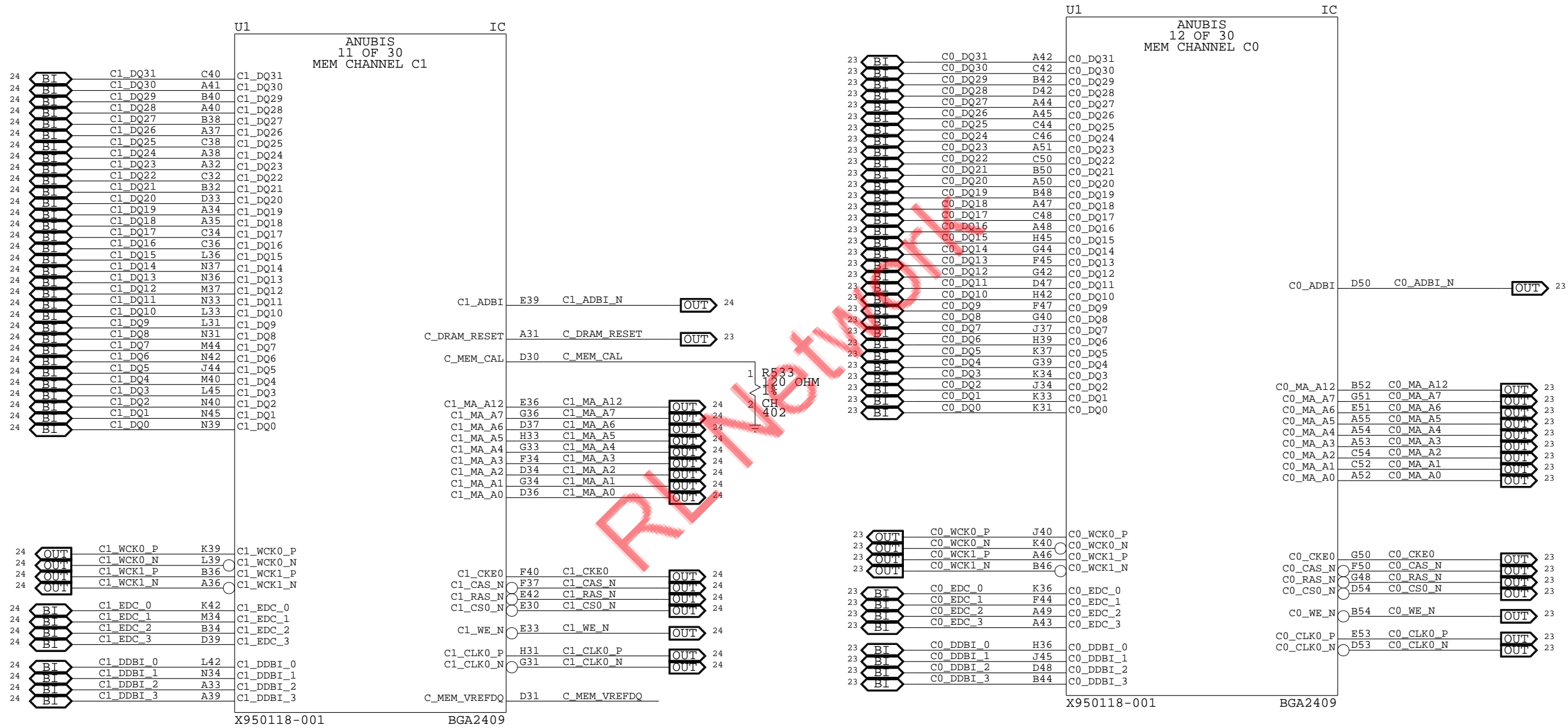
MEMORY: PARTITION E1/E0



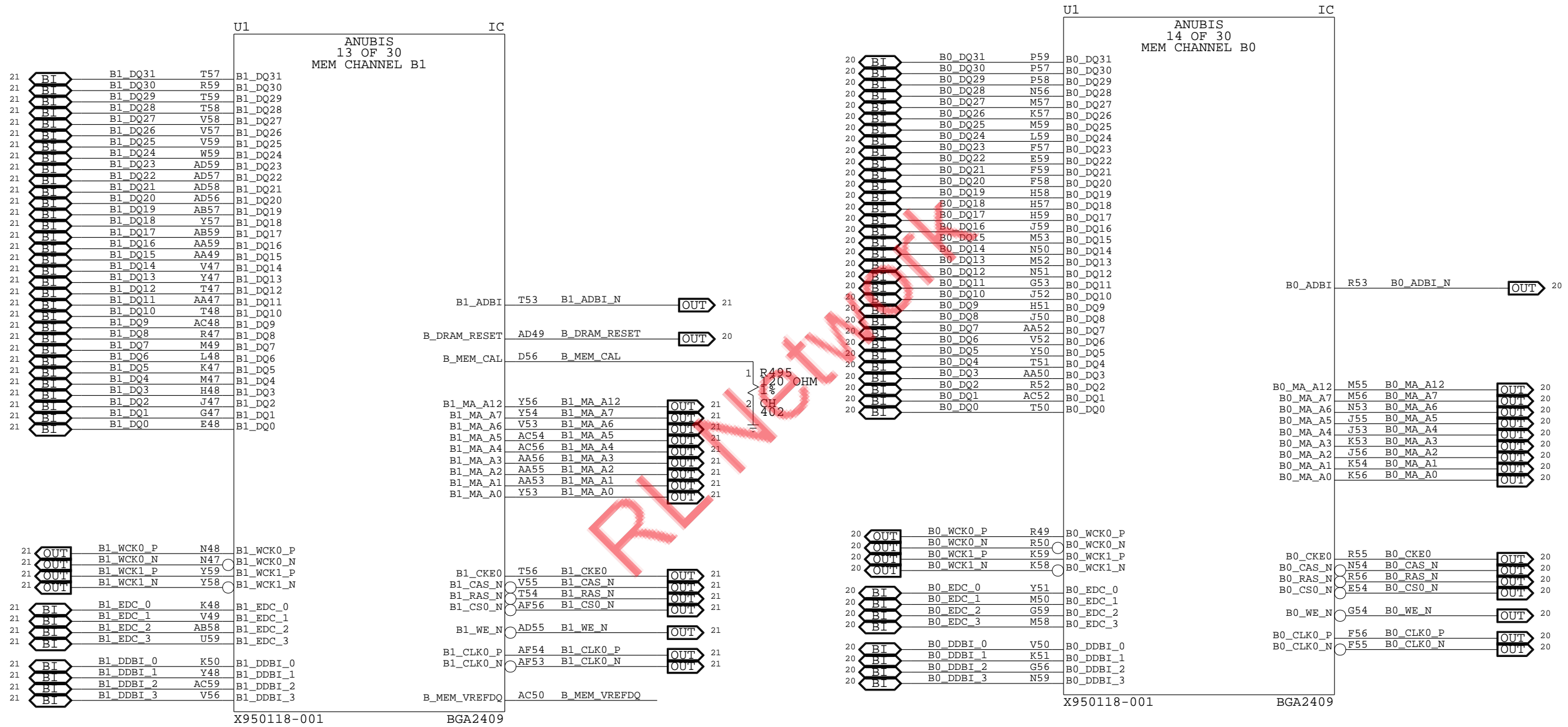
MEMORY: PARTITION D1/D0



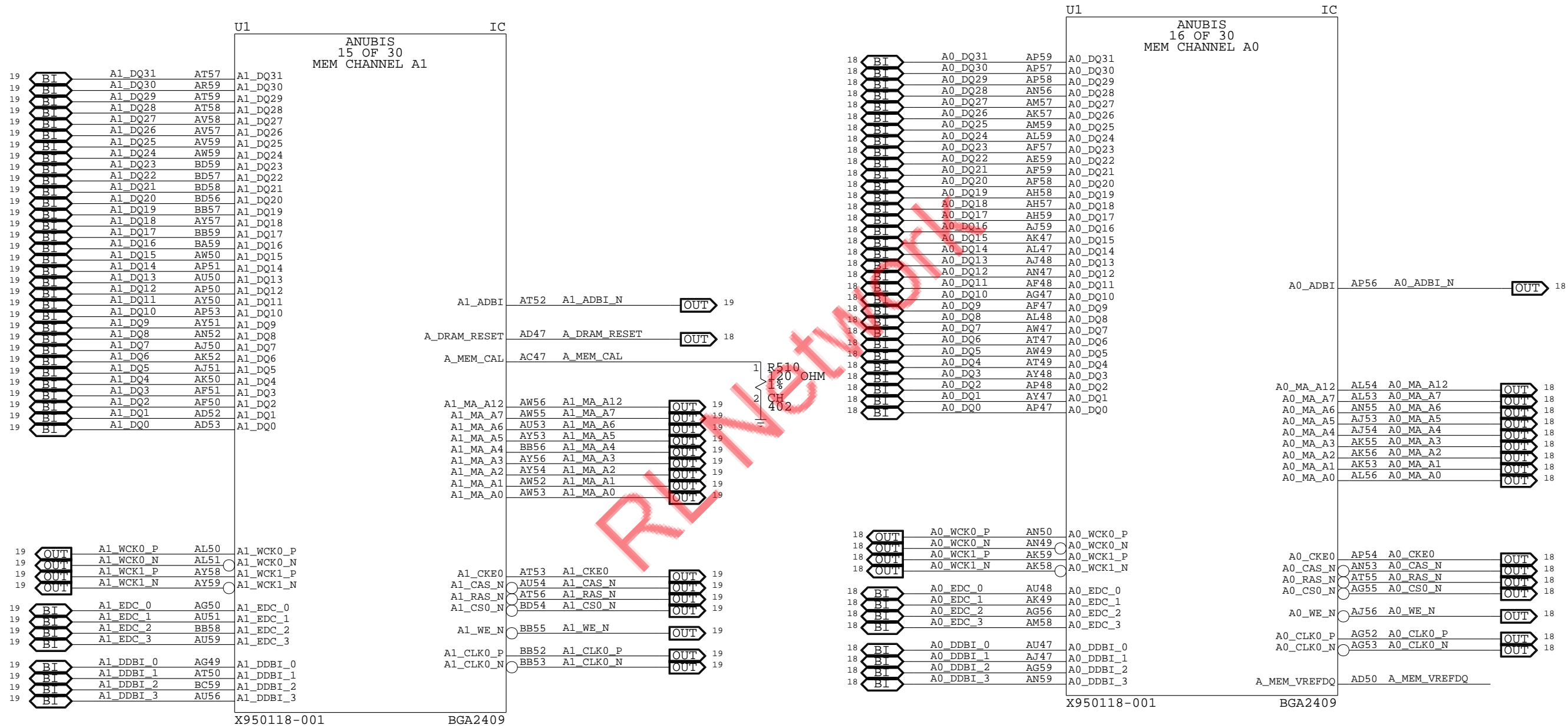
MEMORY: PARTITION C1/C0



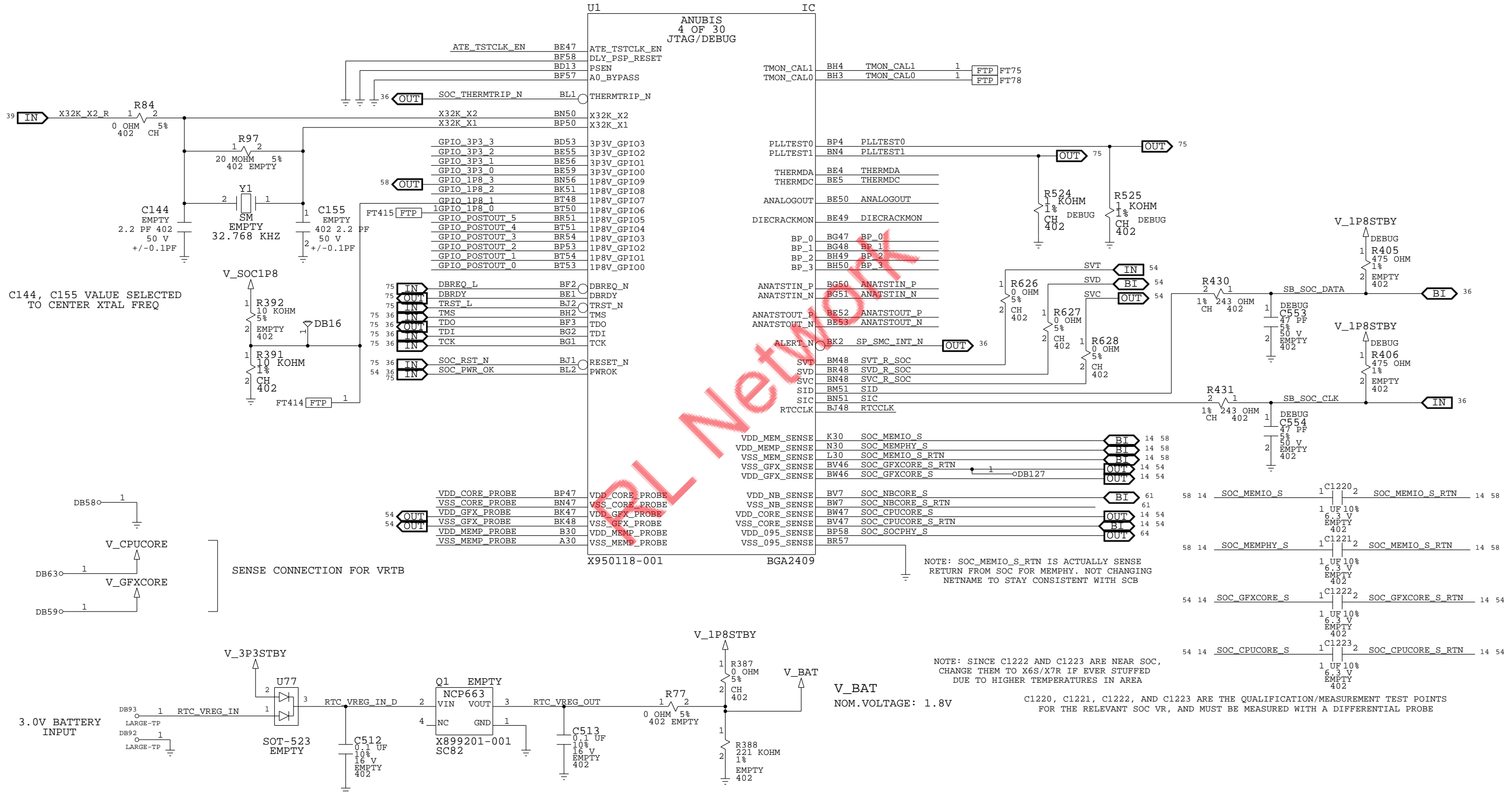
MEMORY: PARTITION B1/B0



MEMORY: PARTITION A1/A0



SOC: DEBUG, SB SIGNALS, V_BAT



C144, C155 VALUE SELECTED TO CENTER XTAL FREQ

SENSE CONNECTION FOR VRTB

NOTE: SOC_MEMIO_S_RTN IS ACTUALLY SENSE RETURN FROM SOC FOR MEMPHY. NOT CHANGING NETNAME TO STAY CONSISTENT WITH SCB

NOTE: SINCE C1222 AND C1223 ARE NEAR SOC, CHANGE THEM TO X6S/X7R IF EVER STUFFED DUE TO HIGHER TEMPERATURES IN AREA

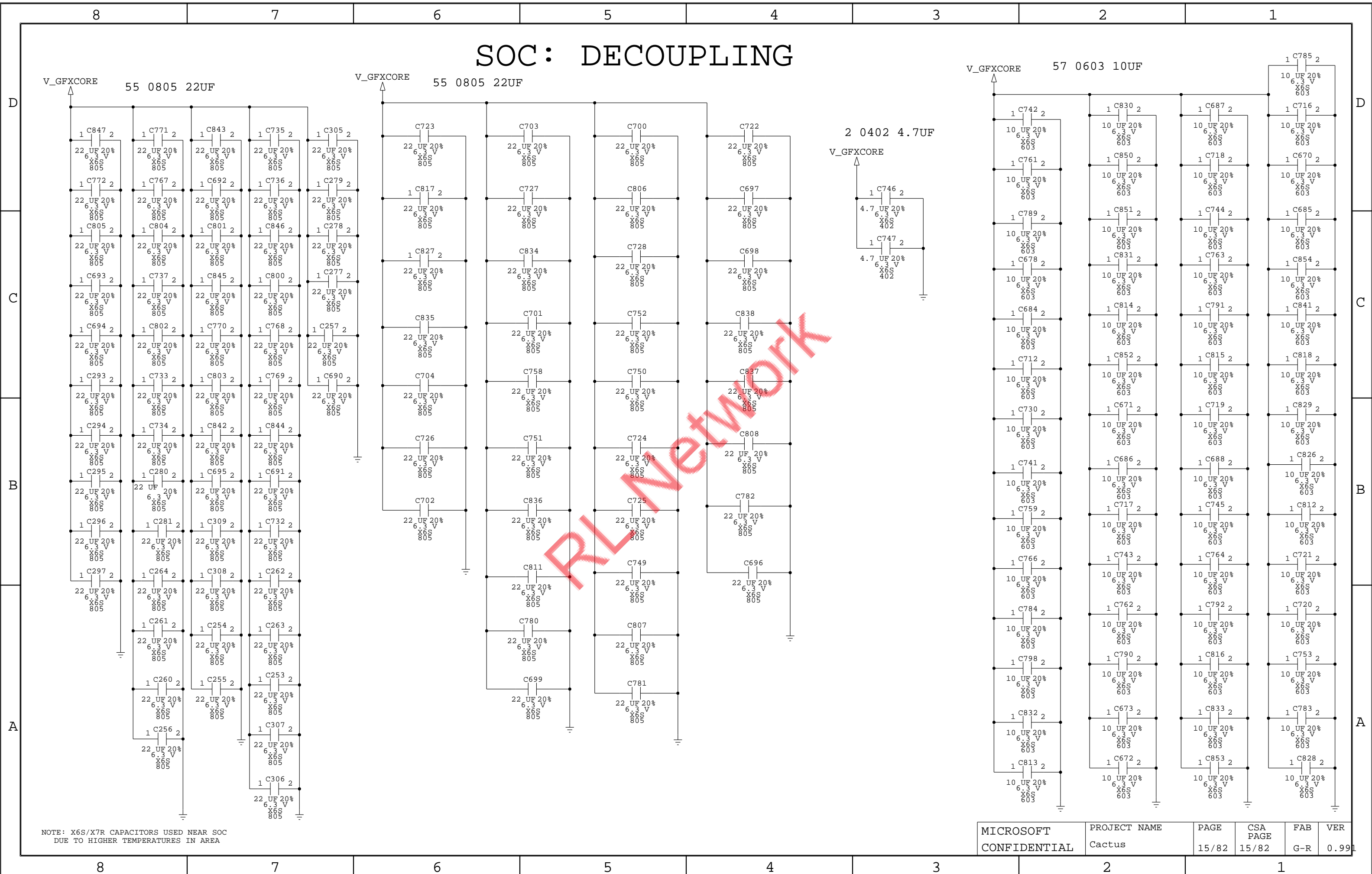
C1220, C1221, C1222, AND C1223 ARE THE QUALIFICATION/MEASUREMENT TEST POINTS FOR THE RELEVANT SOC VR, AND MUST BE MEASURED WITH A DIFFERENTIAL PROBE

V_BAT
NOM. VOLTAGE: 1.8V

STUFF R388 IF SOC IS NOT STUFFED

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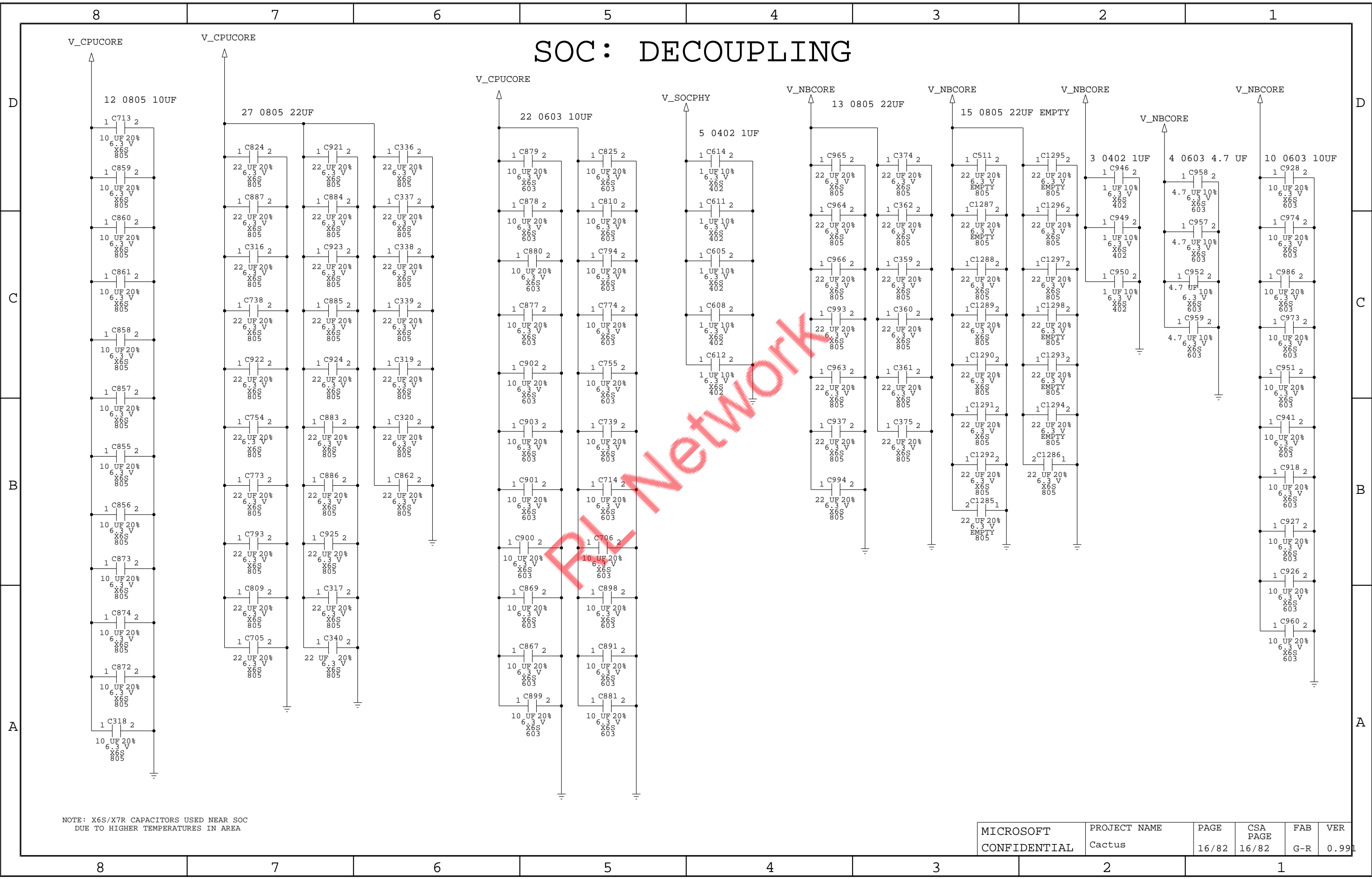
SOC: DECOUPLING



NOTE: X6S/X7R CAPACITORS USED NEAR SOC DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
CONFIDENTIAL	Cactus	15/82	15/82	G-R	0.99L

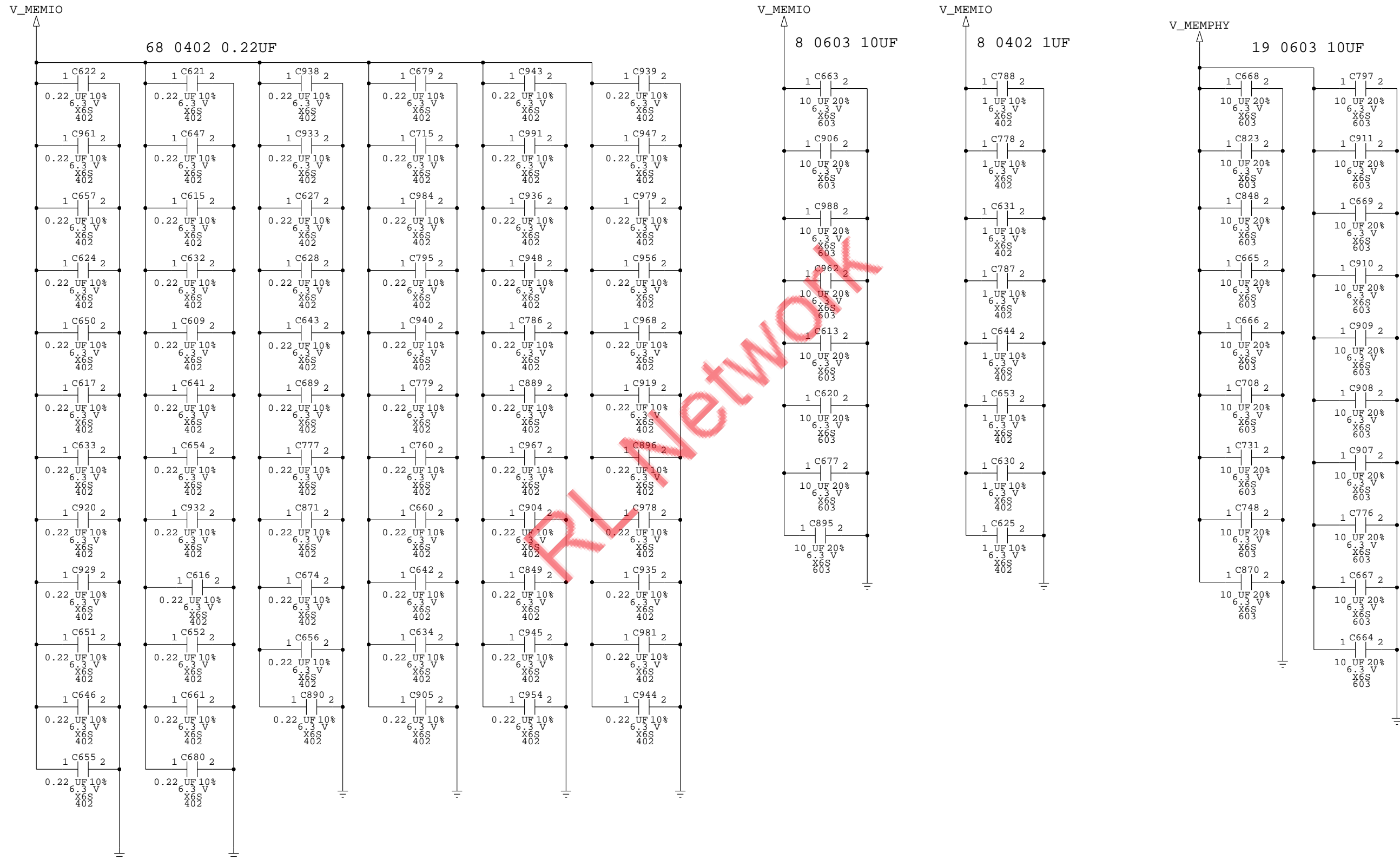
SOC: DECOUPLING



NOTE: X6S/X7R CAPACITORS USED NEAR SOC DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 16/82	CSA PAGE 16/82	FAB G-R	VER 0.99L
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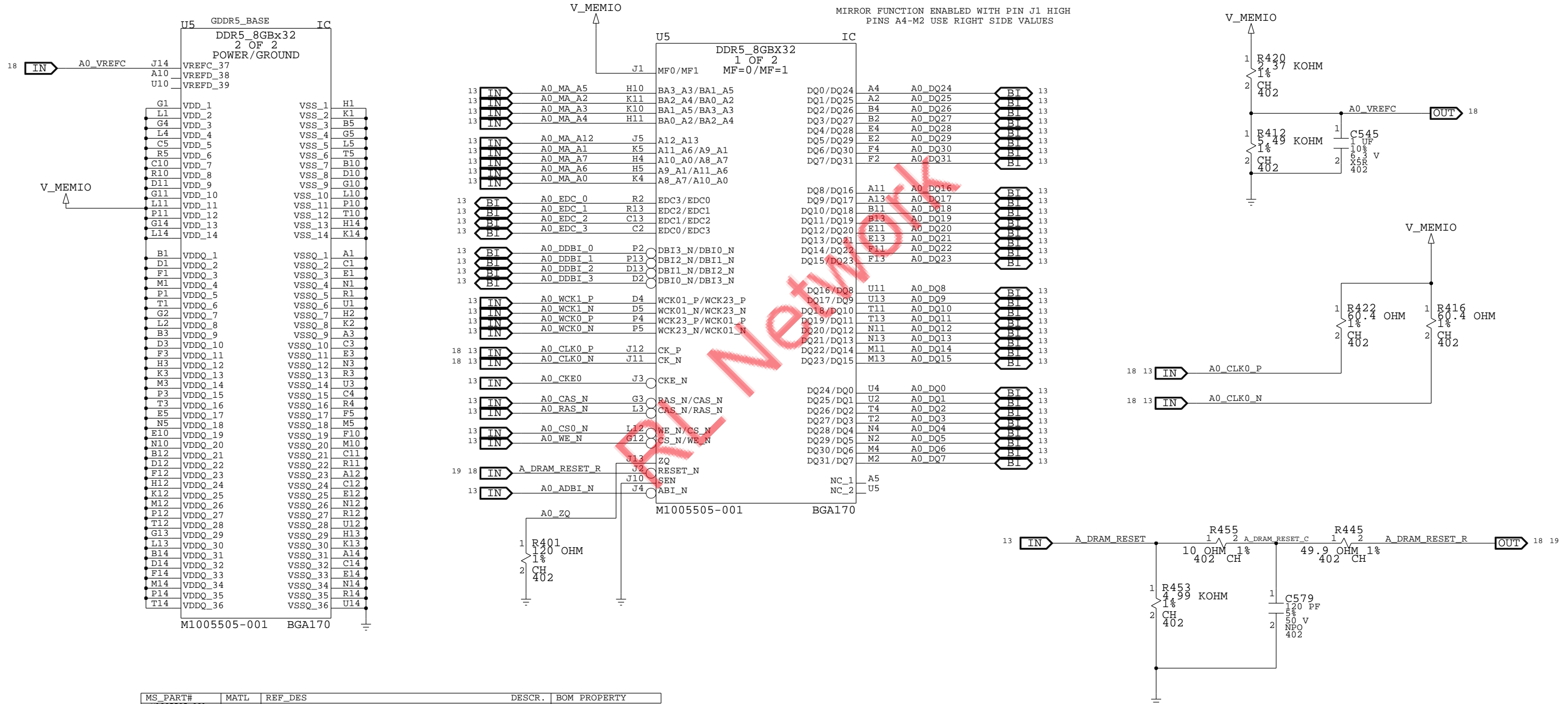
SOC: DECOUPLING



NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

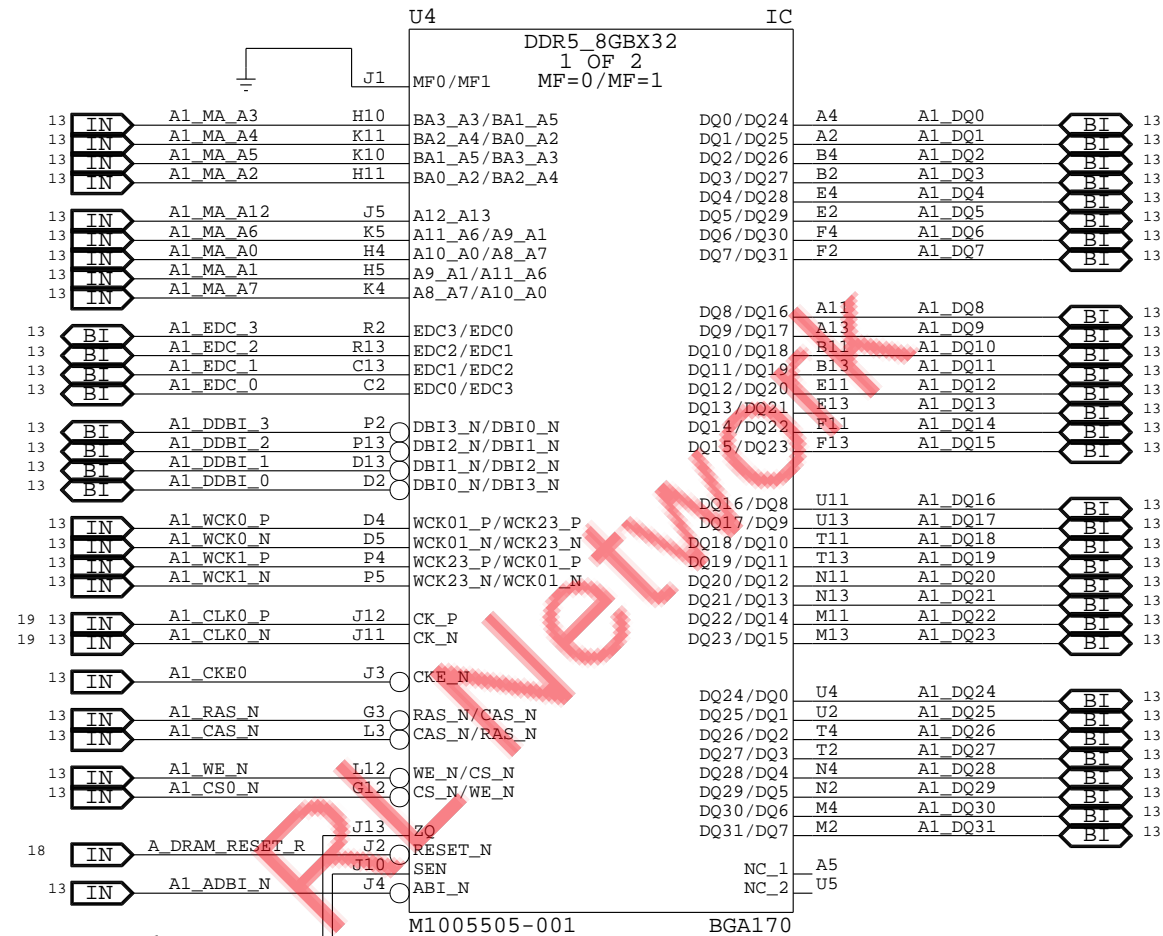
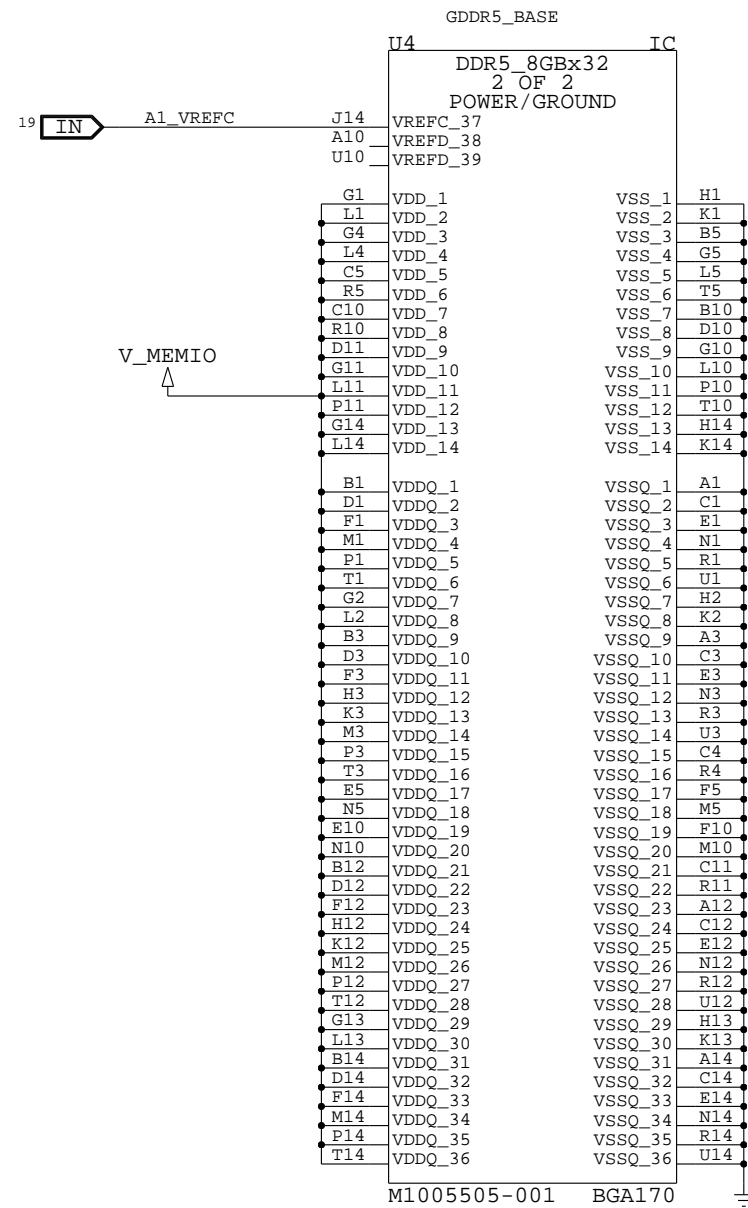
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MEMORY: CHANNEL A0

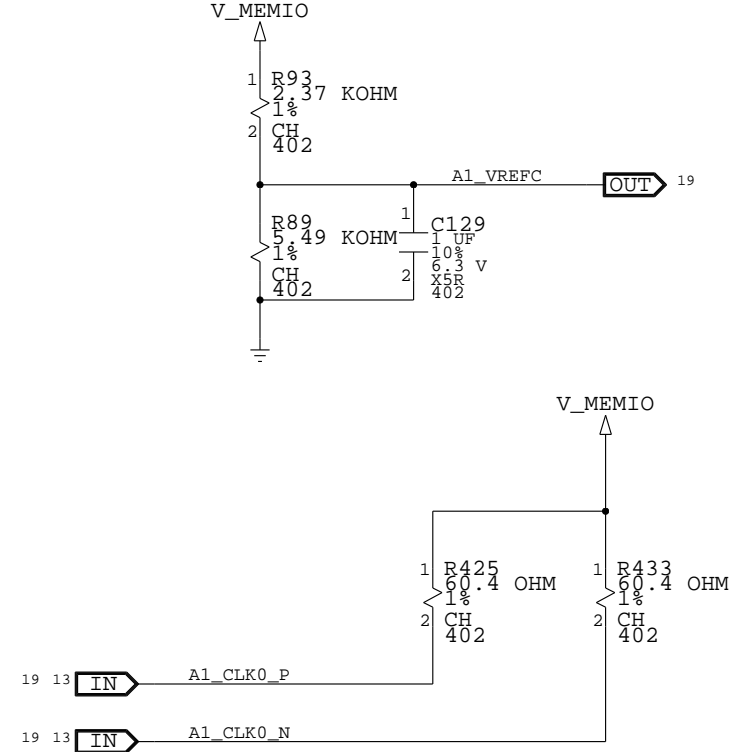


MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
M1005505-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FPRGM	GDDR5_SAMSUNG
M1005717-001	IC	U4,U5,U6,U7,U8,U9,U10,U11,U12,U13,U14,U15	MEM,SM,8GB,16MX32,GDDR5,170FPRGM	GDDR5_HYNIX

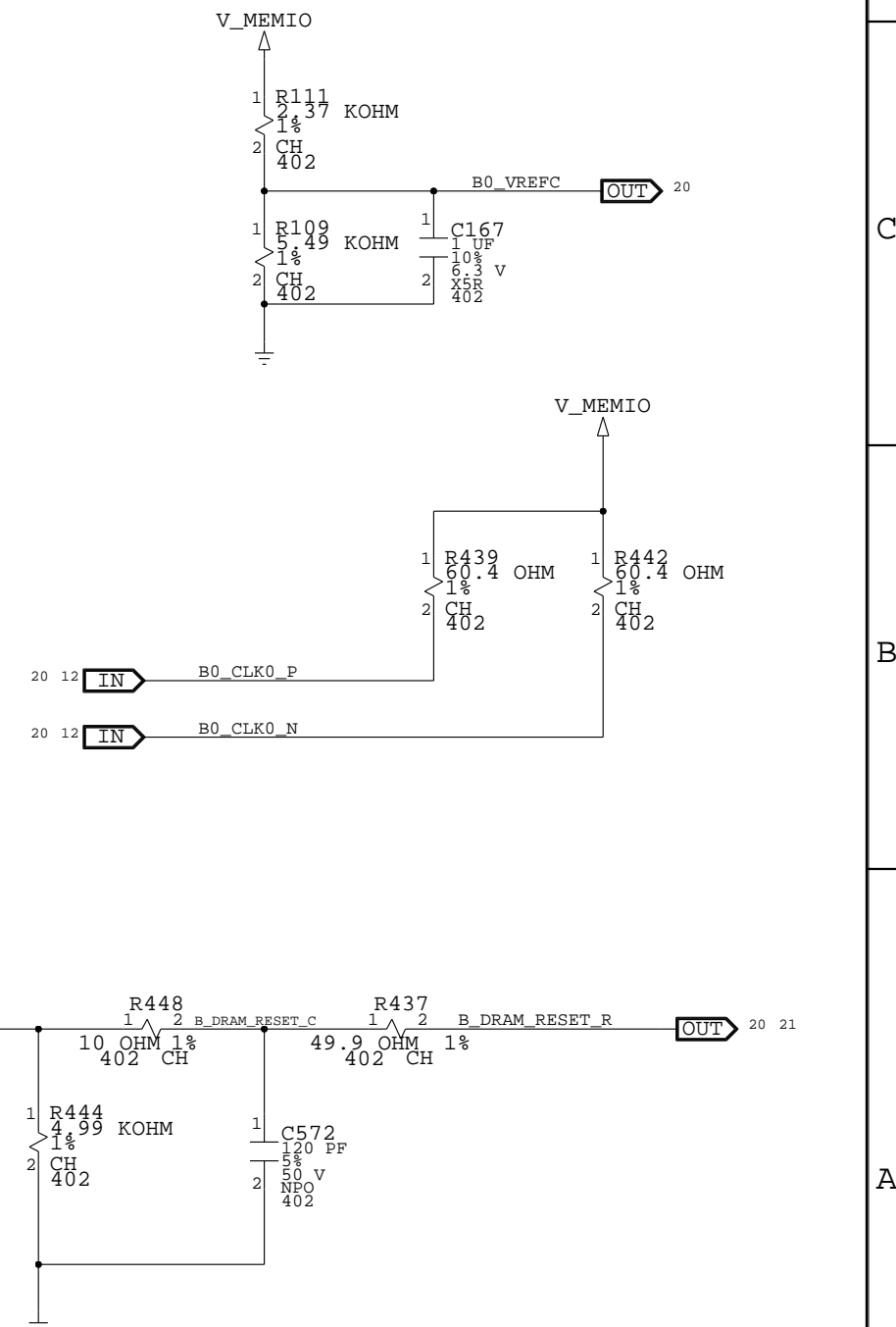
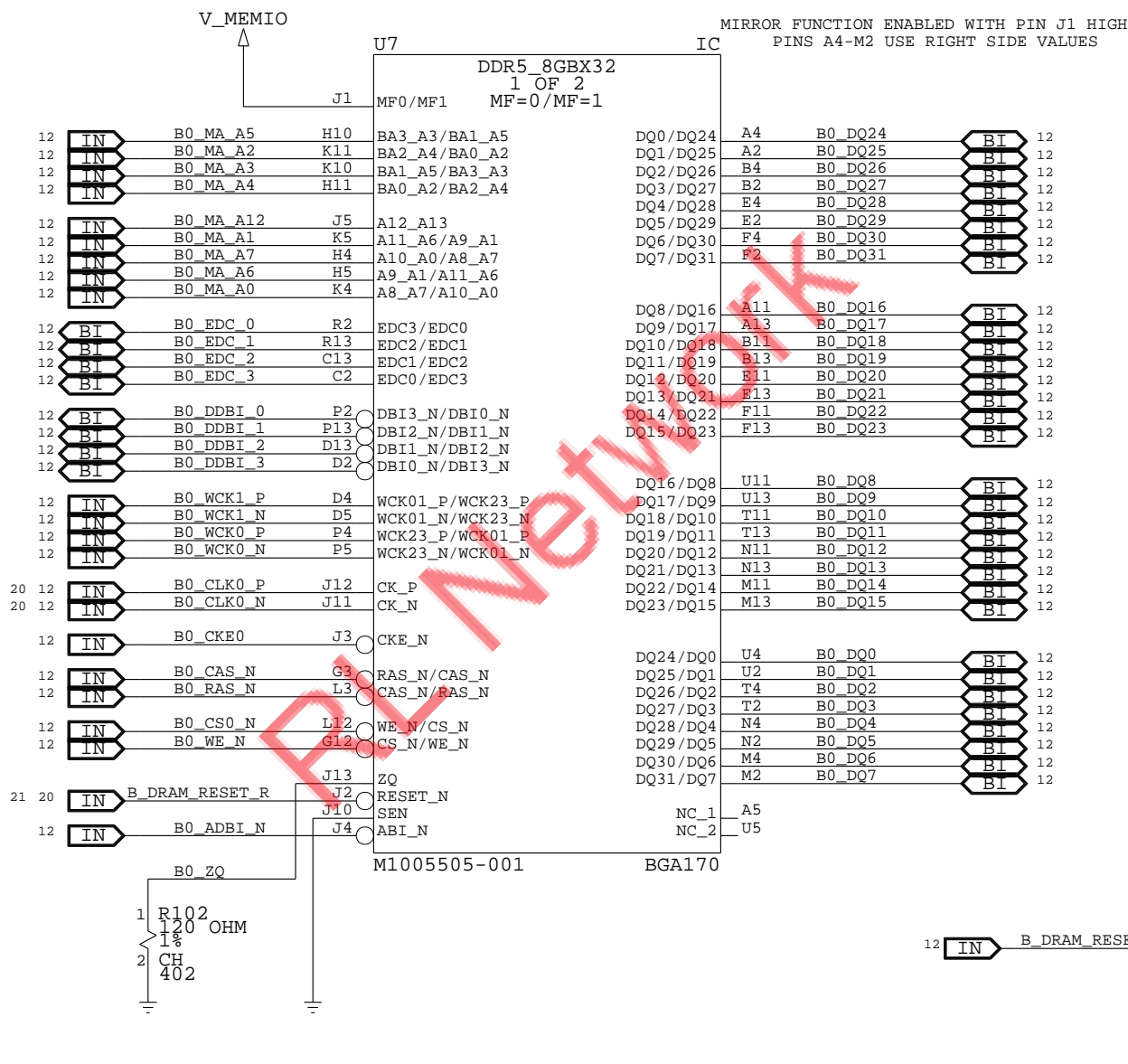
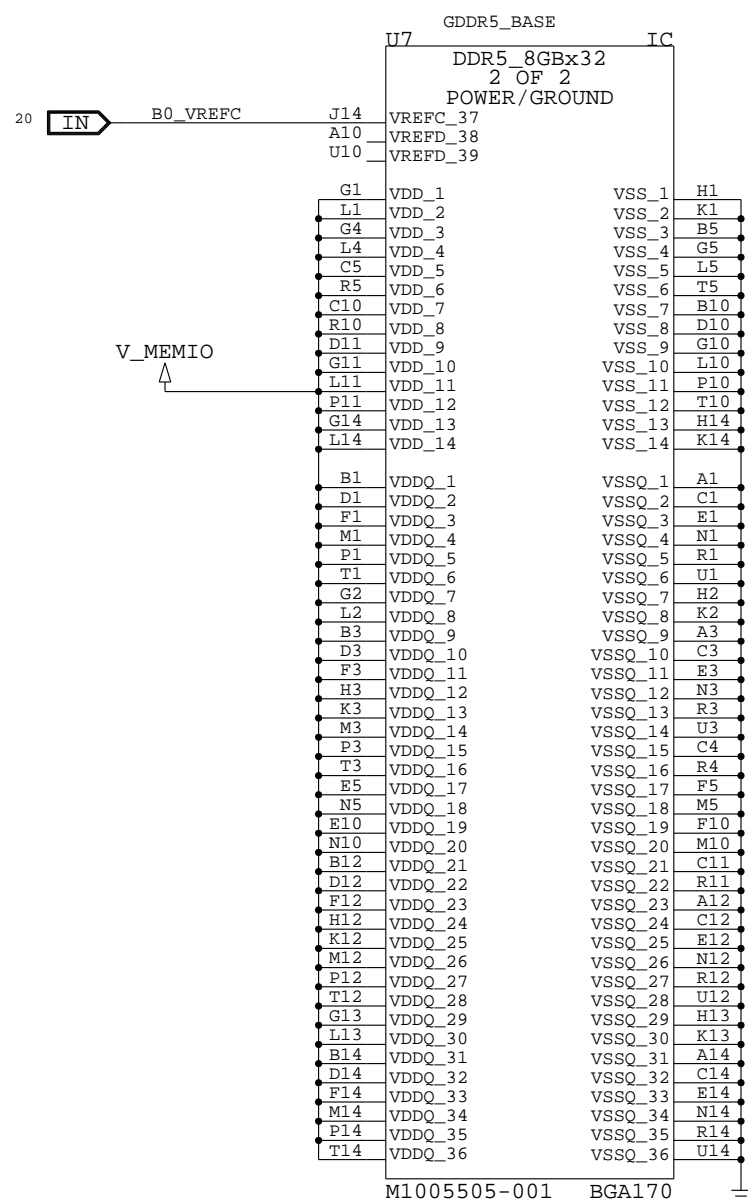
MEMORY: CHANNEL A1



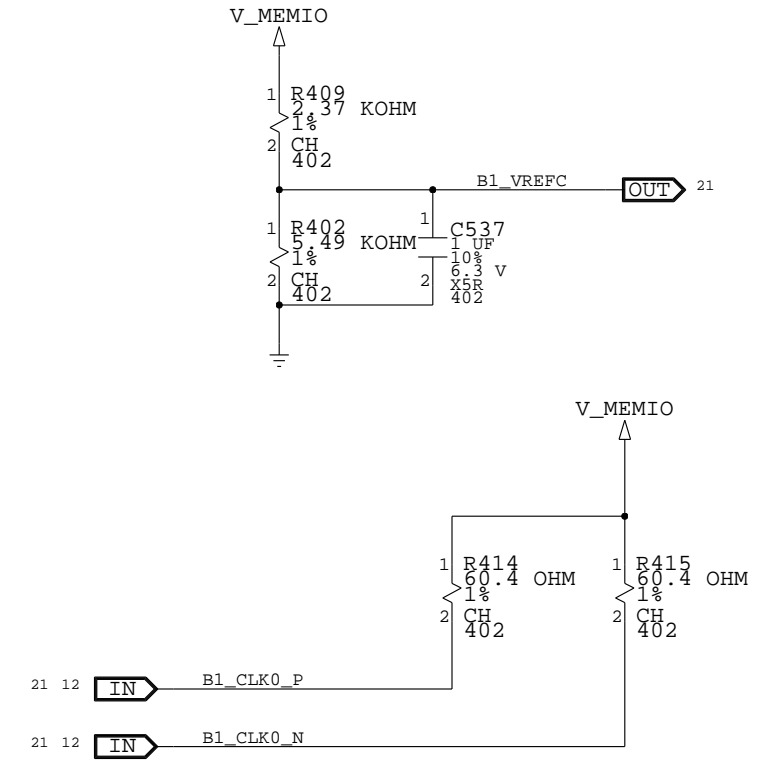
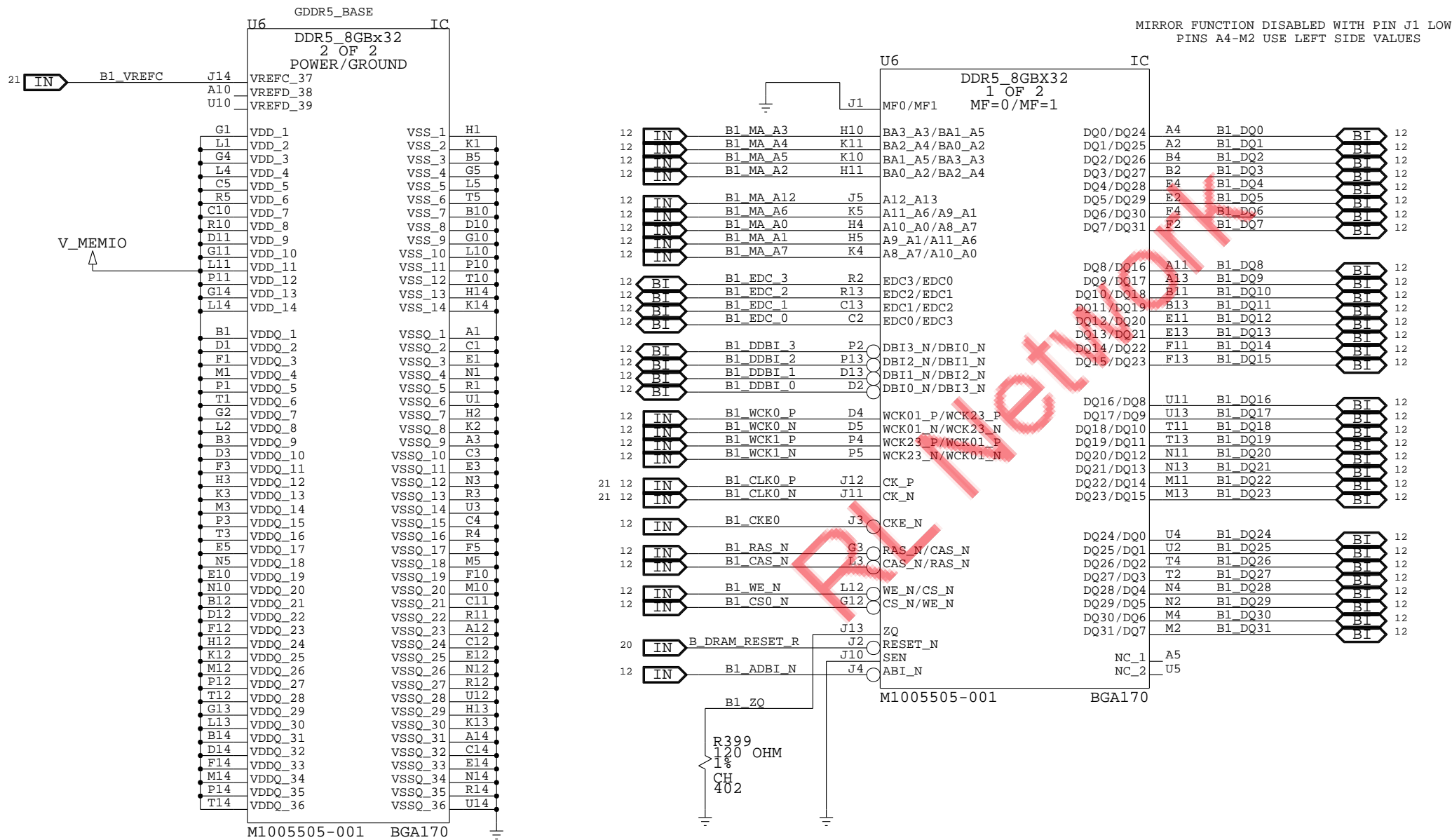
MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES



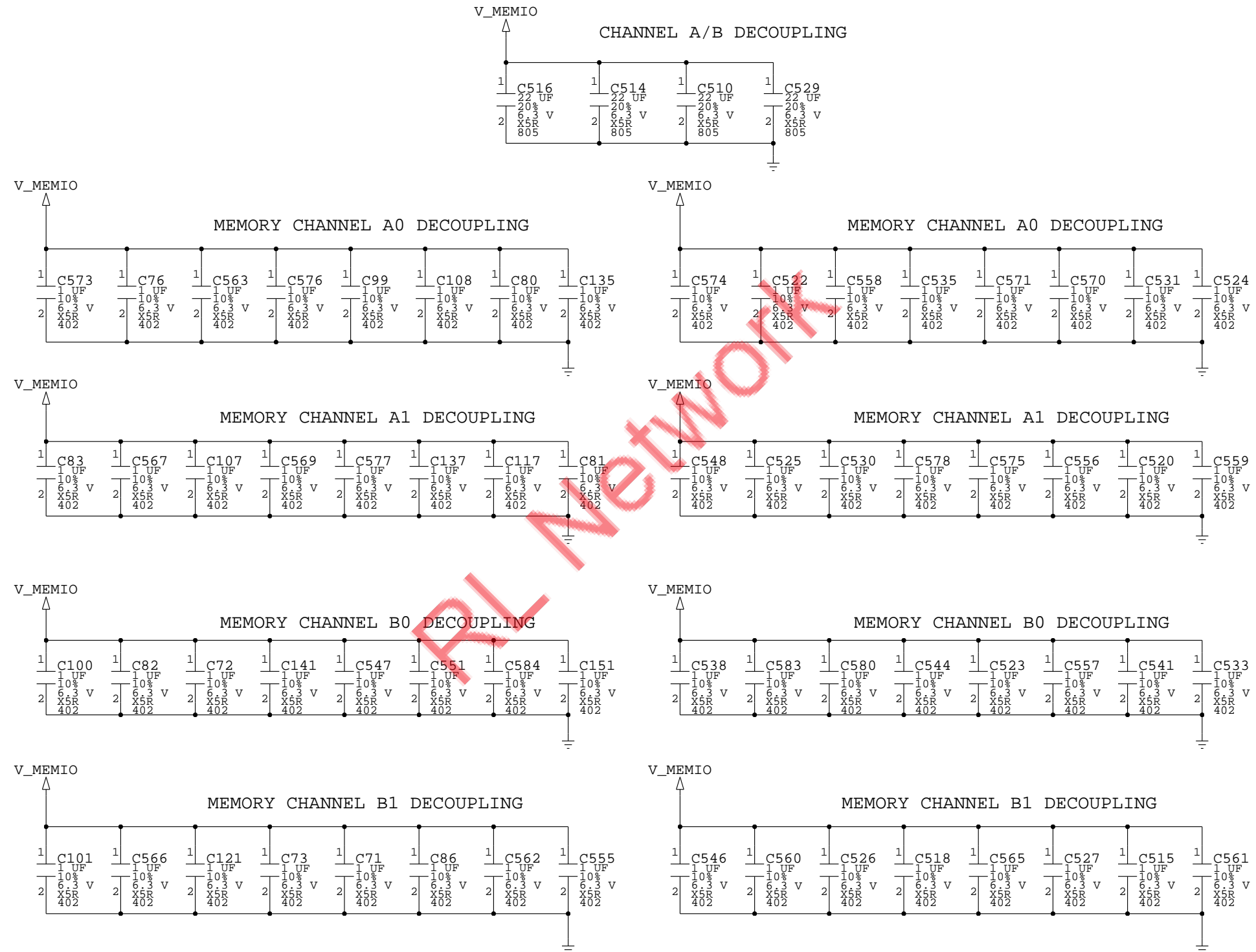
MEMORY: CHANNEL B0



MEMORY: CHANNEL B1



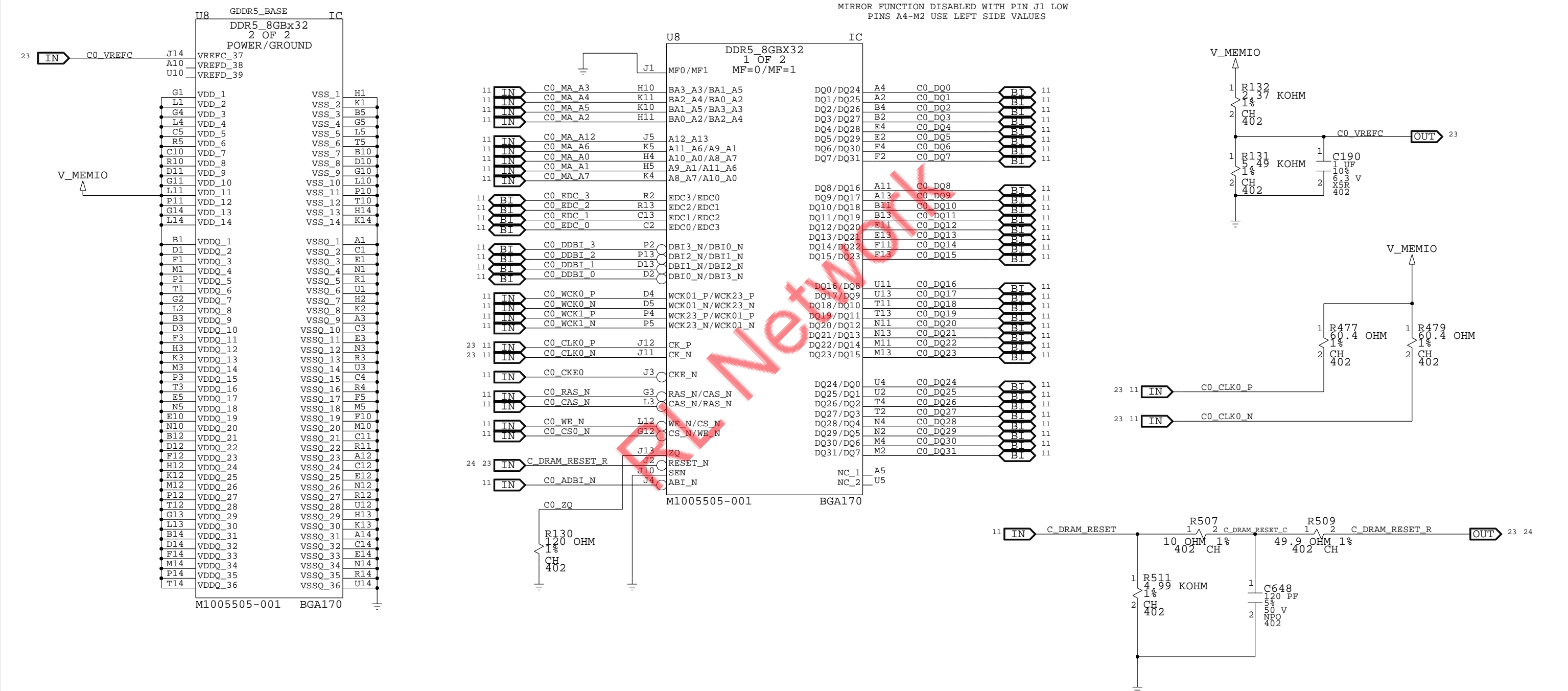
MEMORY: CHANNEL A/B DECOUPLING



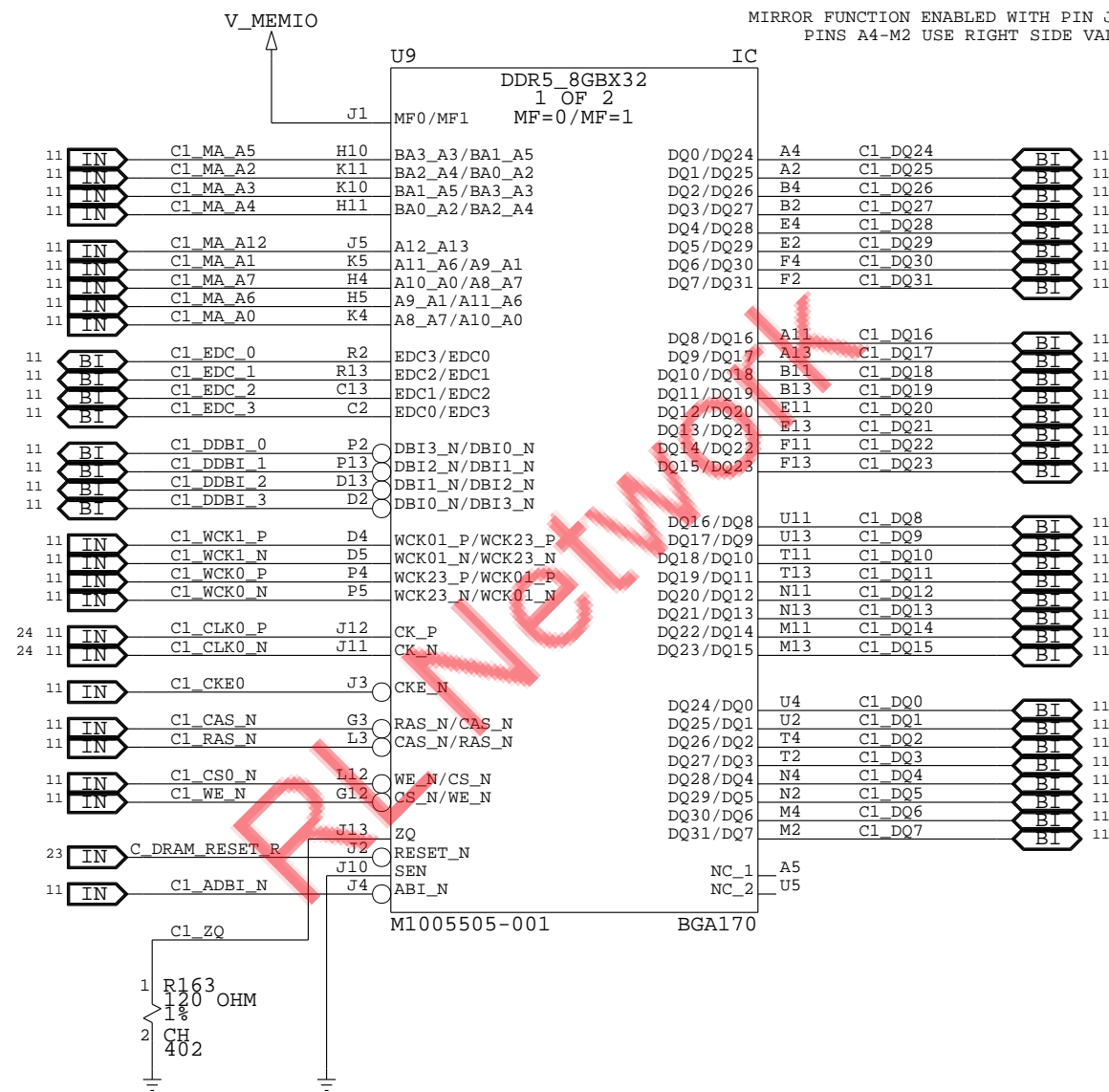
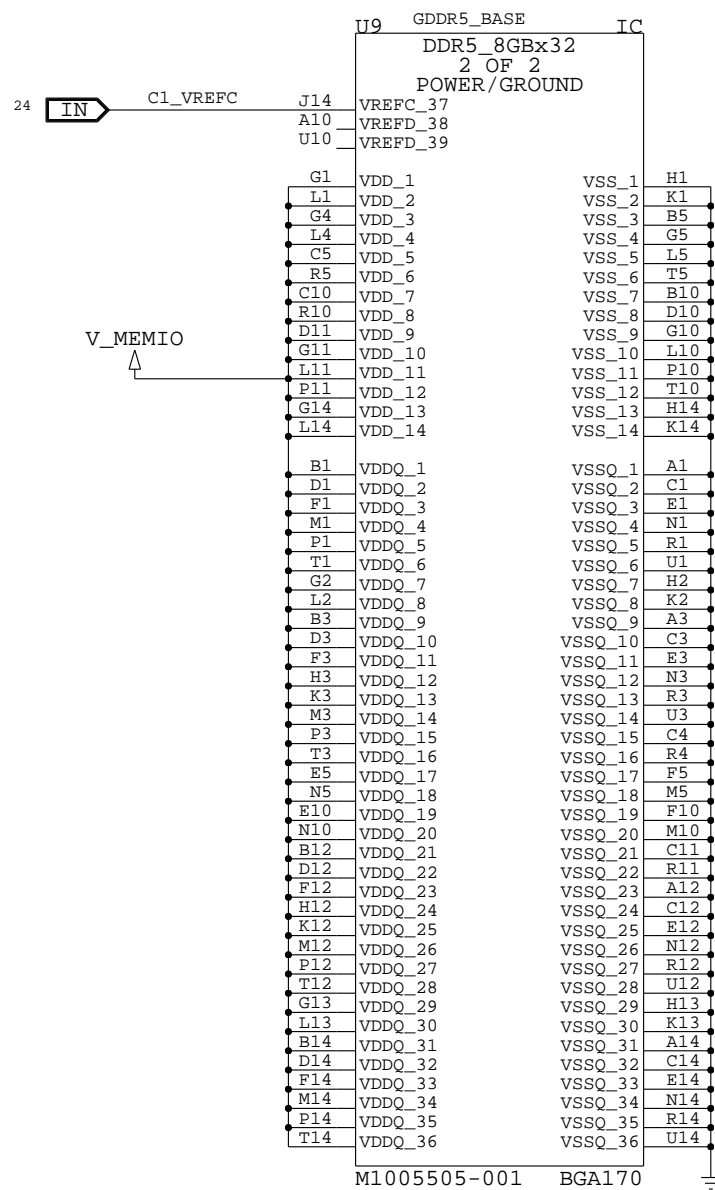
NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

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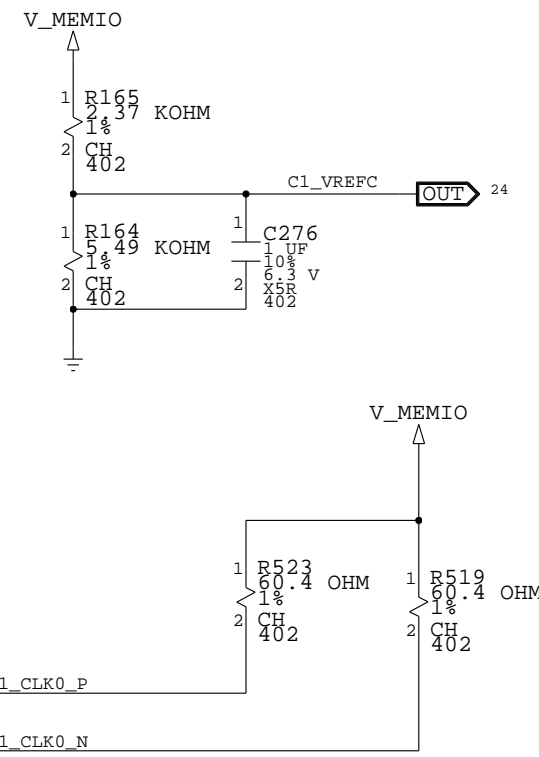
MEMORY: CHANNEL C0



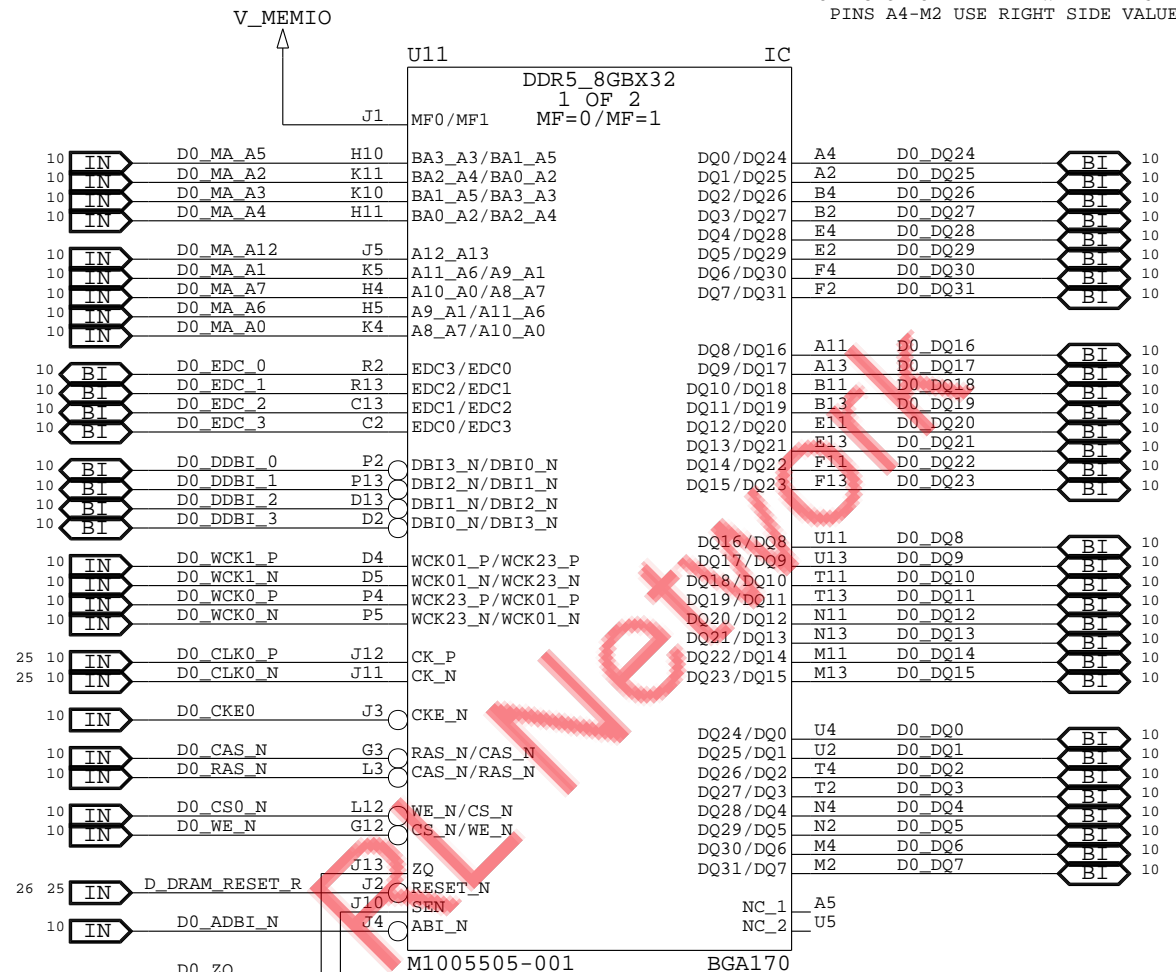
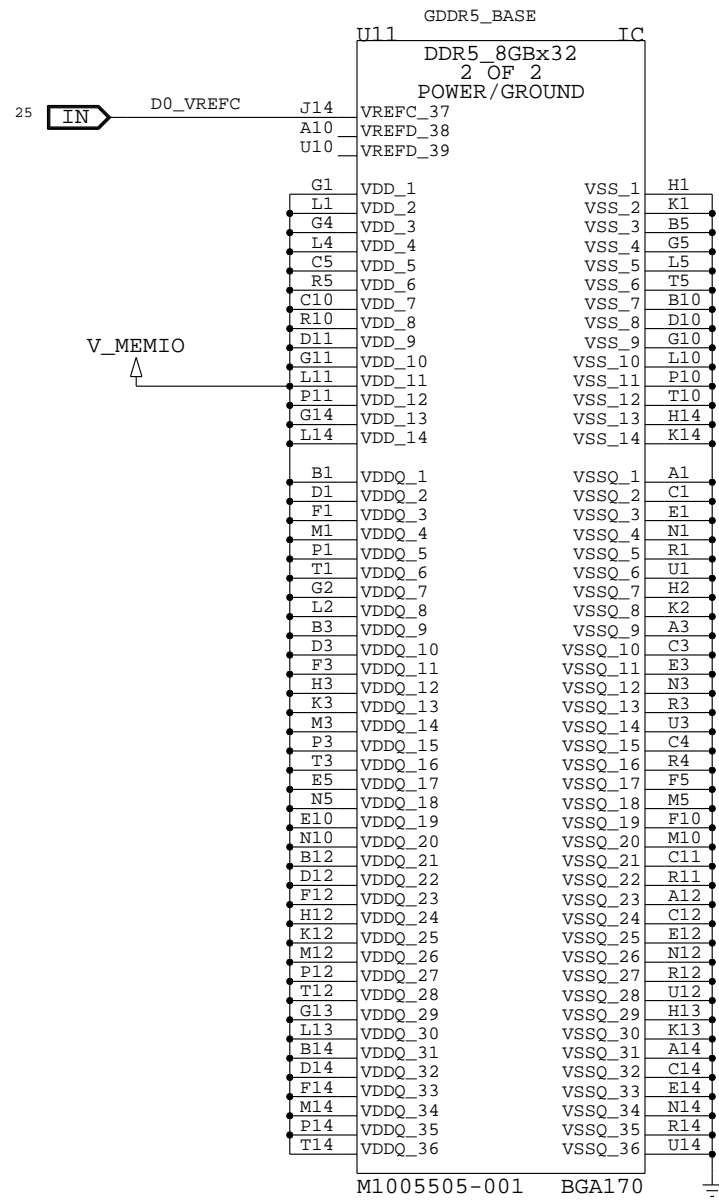
MEMORY: CHANNEL C1



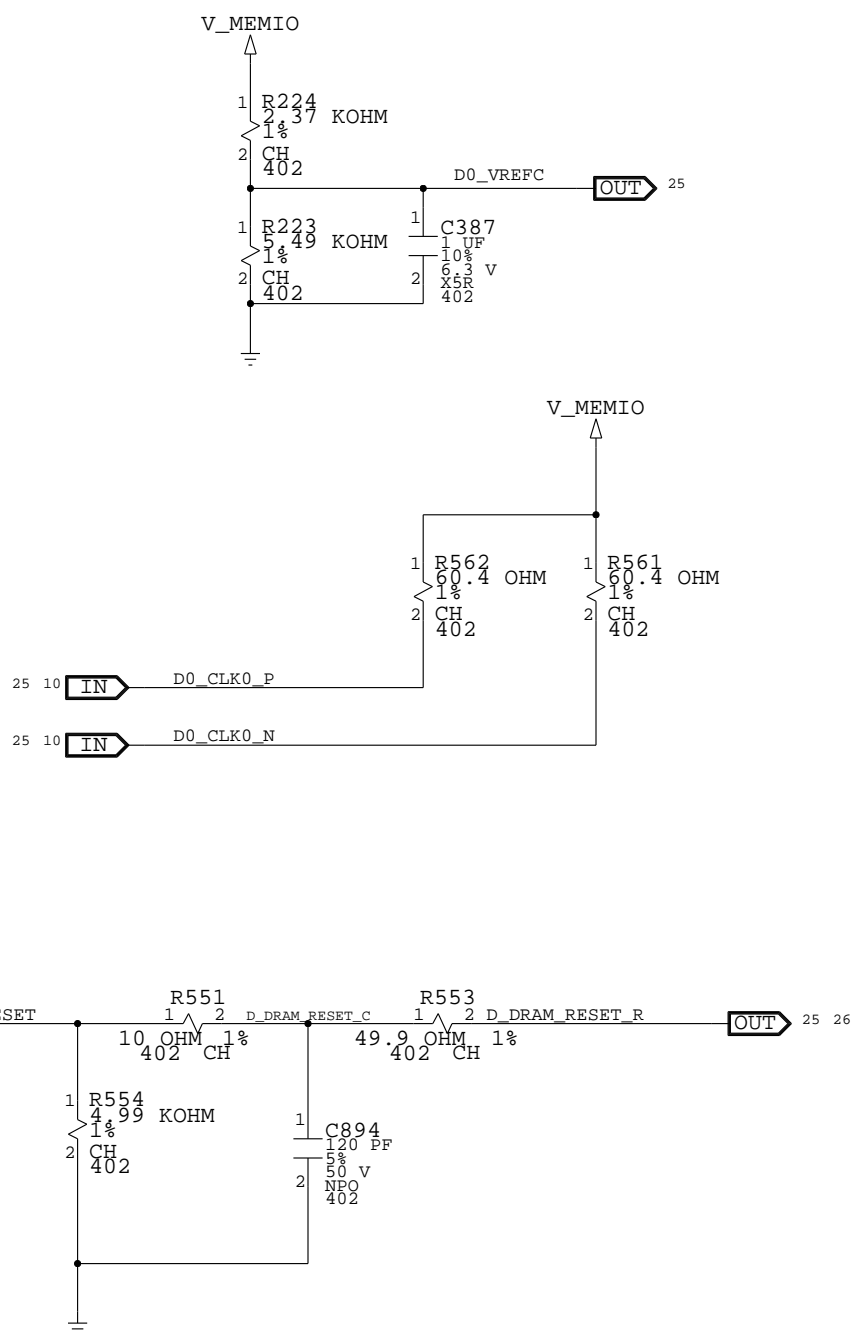
MIRROR FUNCTION ENABLED WITH PIN J1 HIGH
 PINS A4-M2 USE RIGHT SIDE VALUES



MEMORY: CHANNEL D0

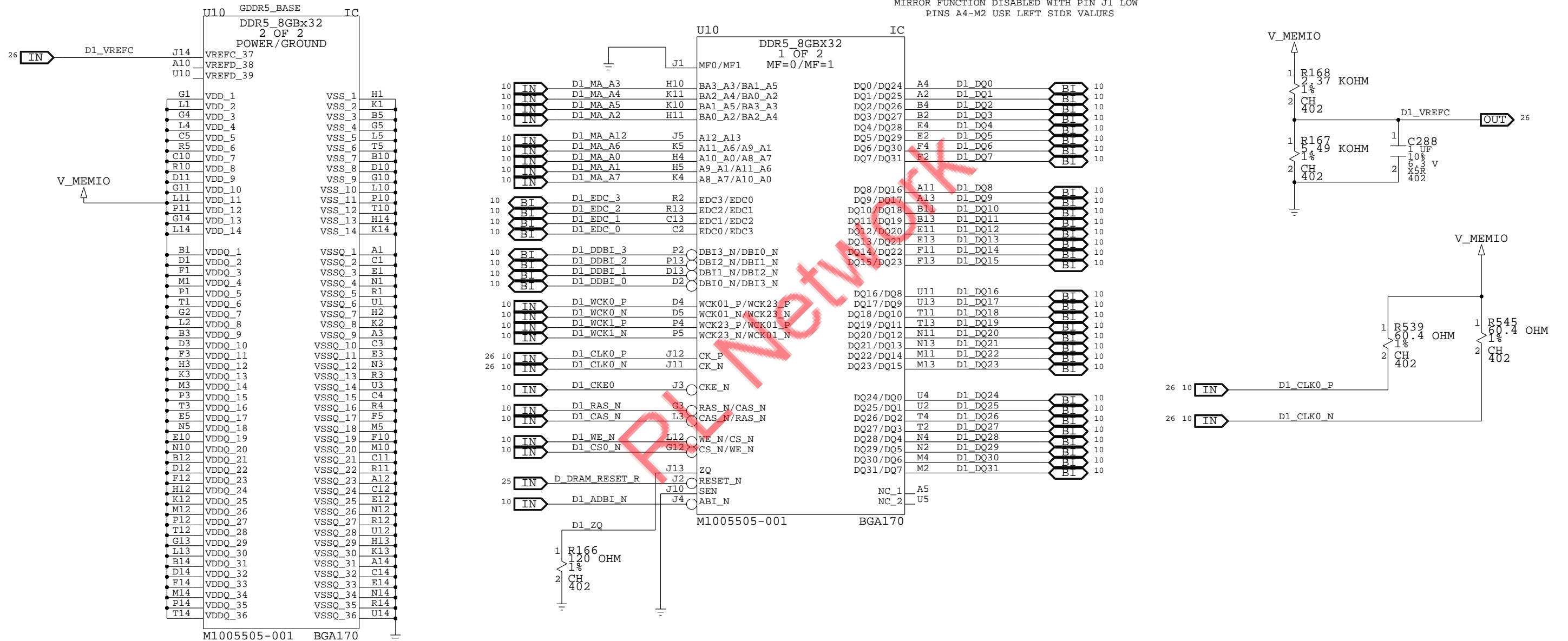


MIRROR FUNCTION ENABLED WITH PIN J1 HIGH
PINS A4-M2 USE RIGHT SIDE VALUES

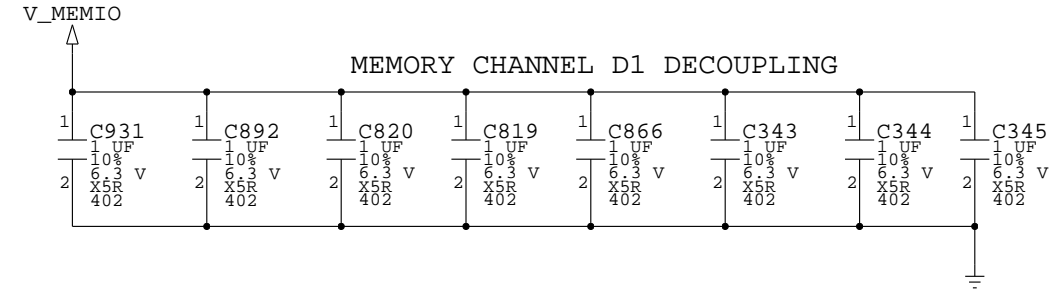
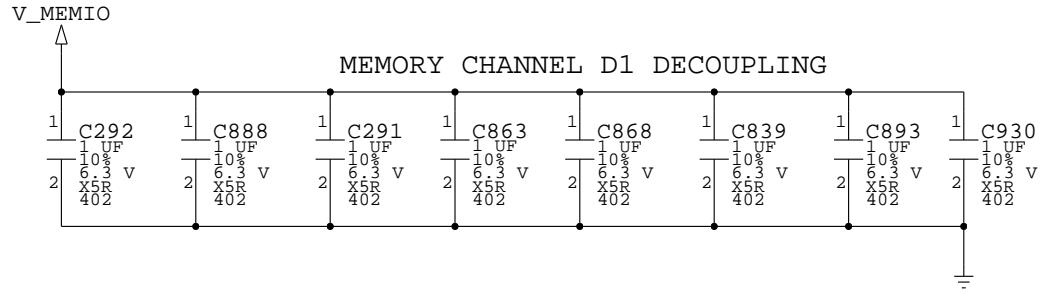
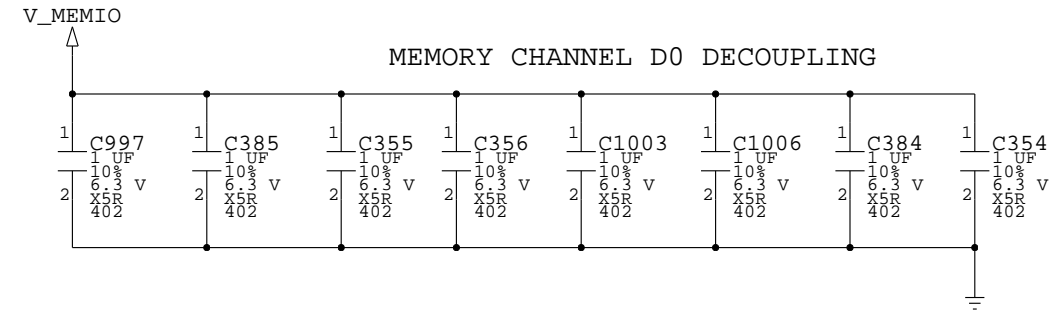
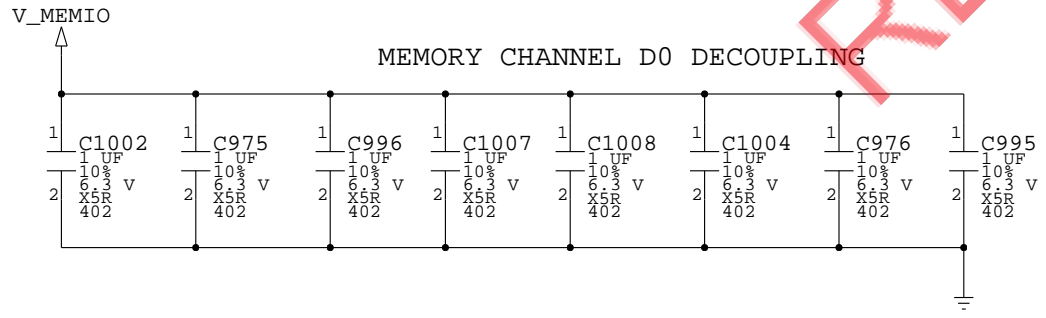
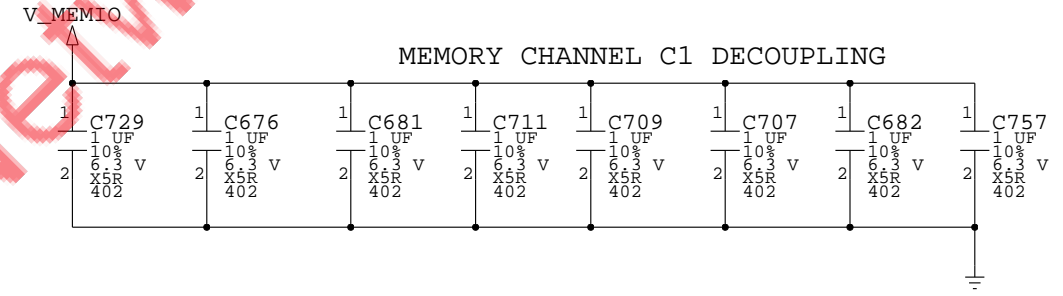
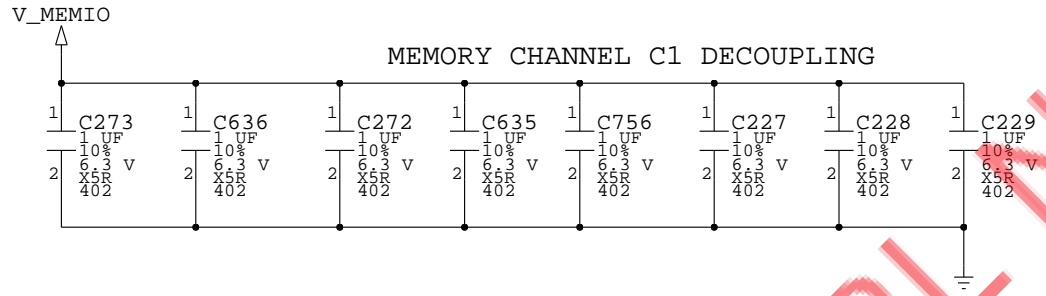
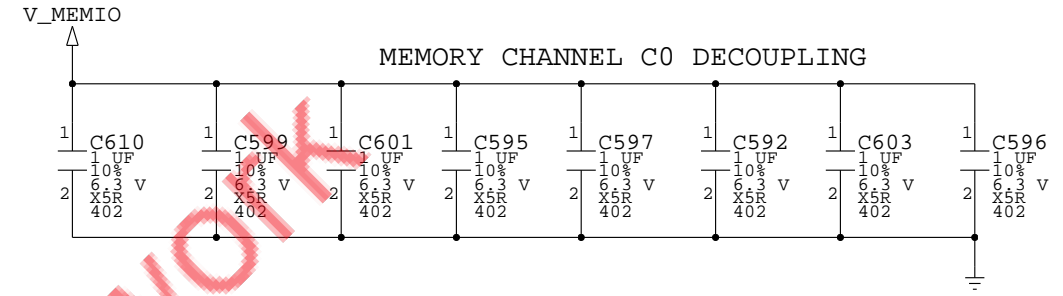
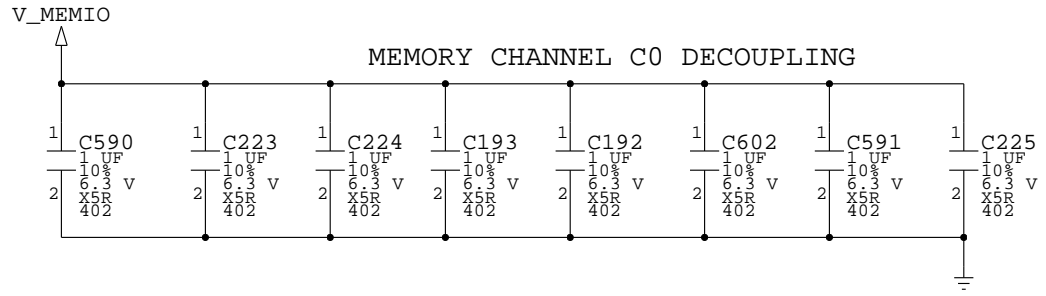
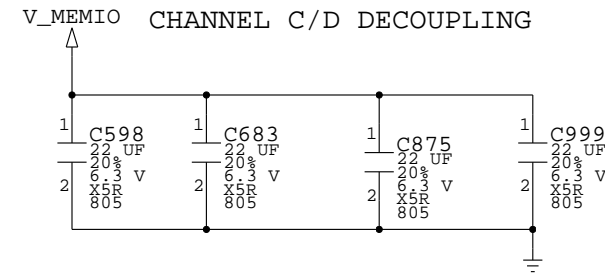


MEMORY: CHANNEL D1

MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES



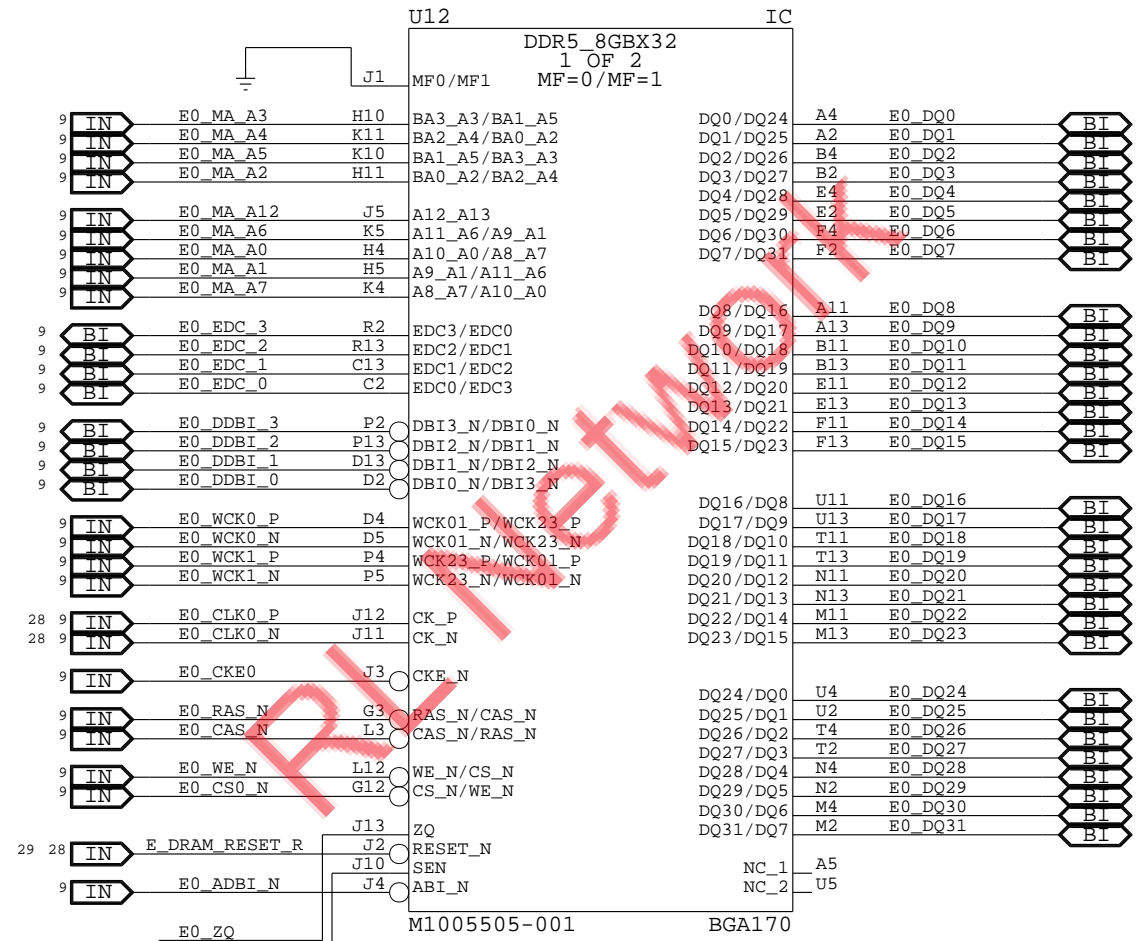
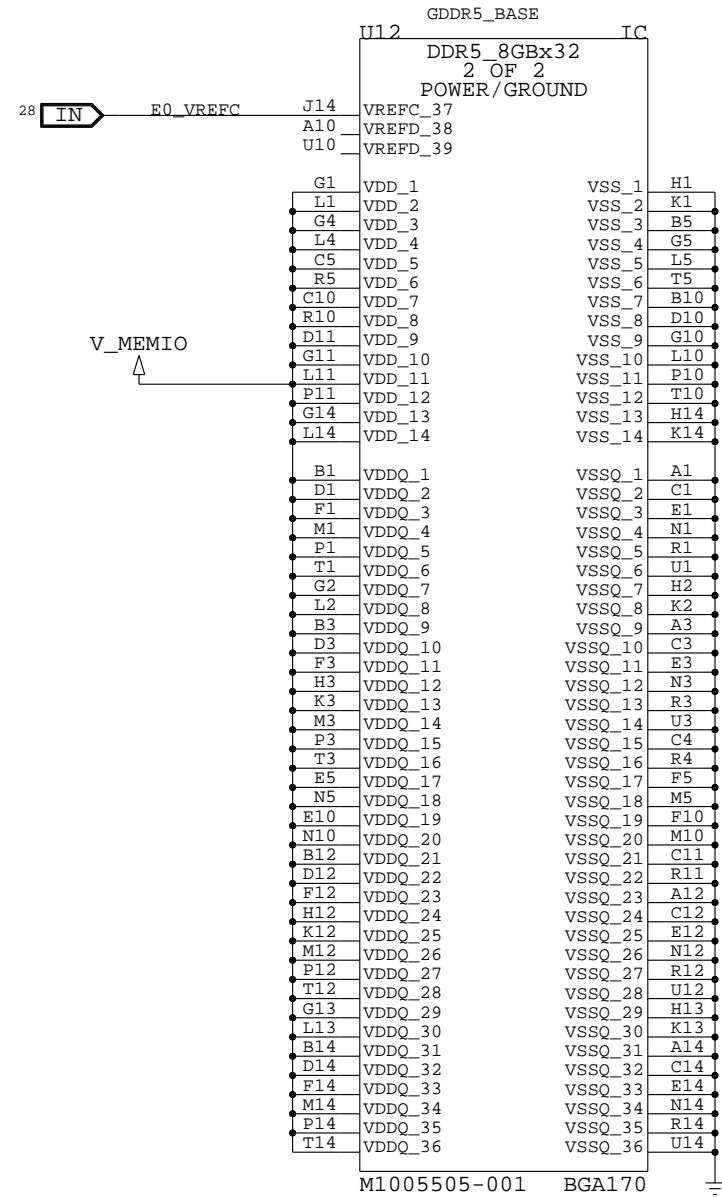
MEMORY: CHANNEL C/D DECOUPLING



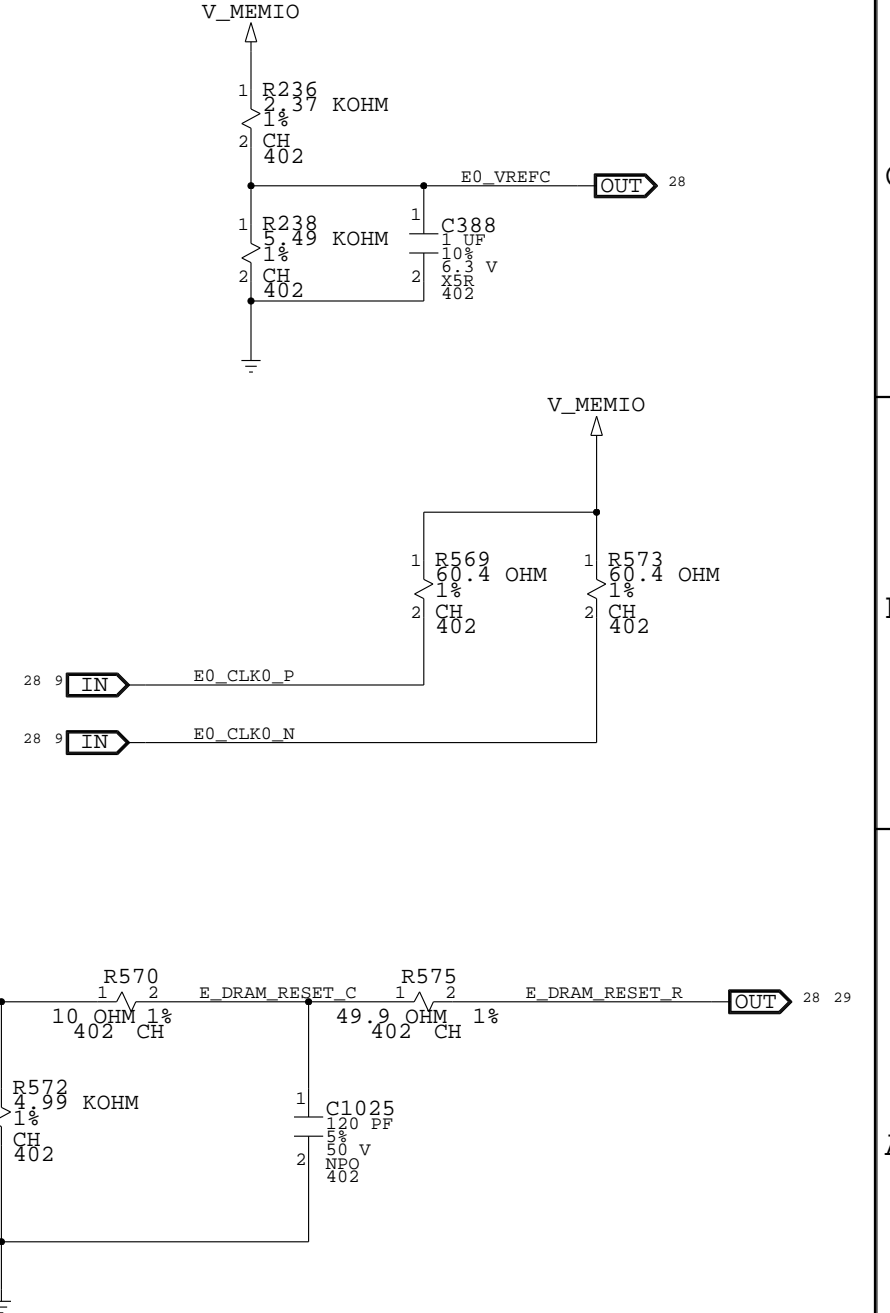
NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

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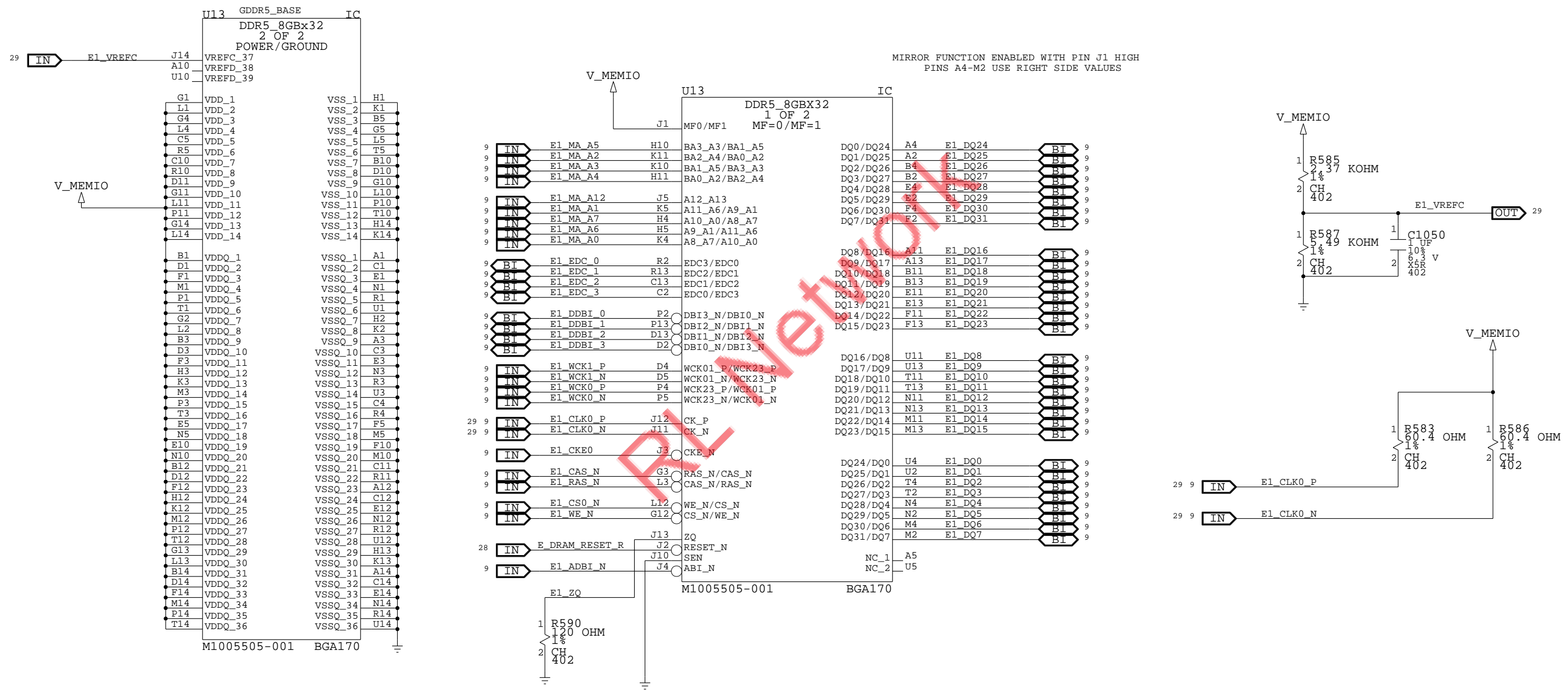
MEMORY: CHANNEL E0



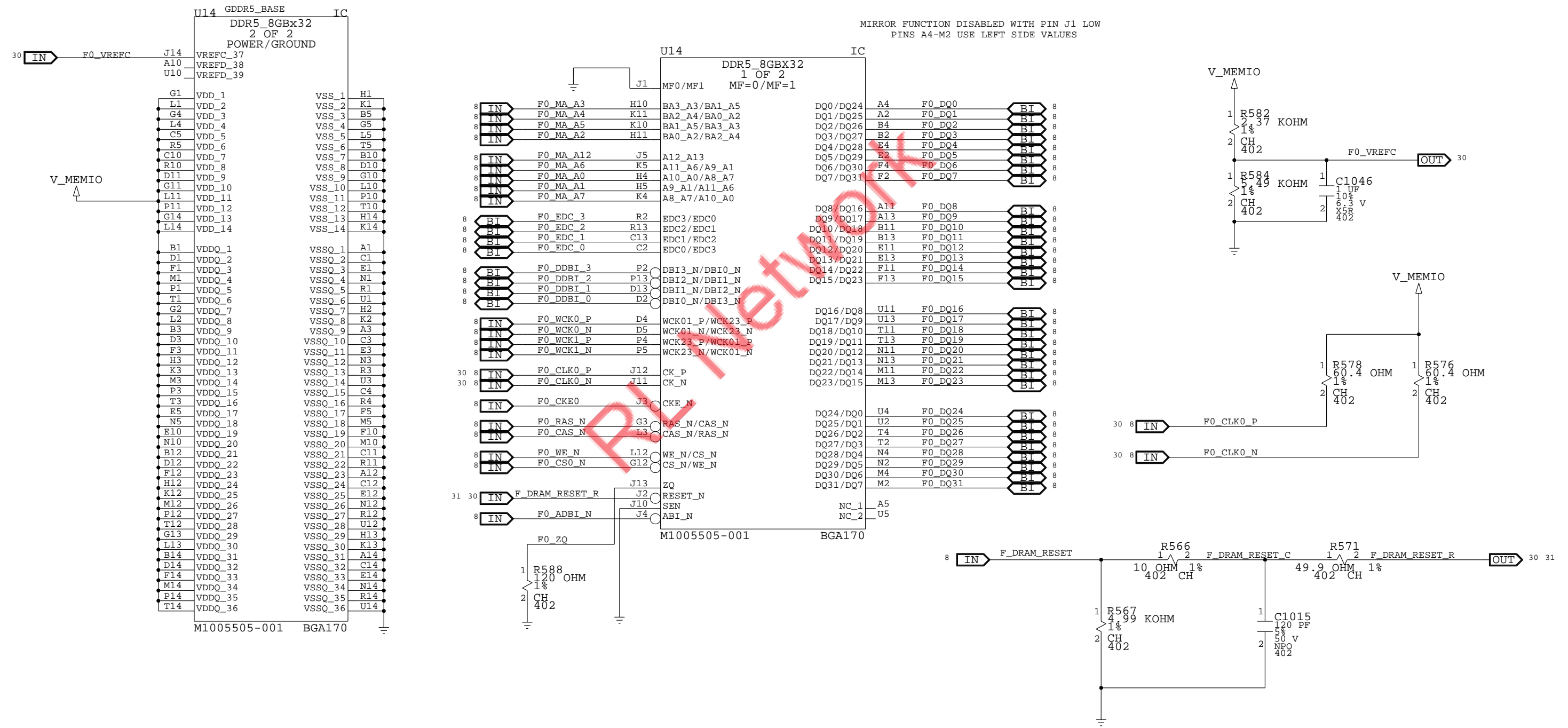
MIRROR FUNCTION DISABLED WITH PIN J1 LOW
PINS A4-M2 USE LEFT SIDE VALUES



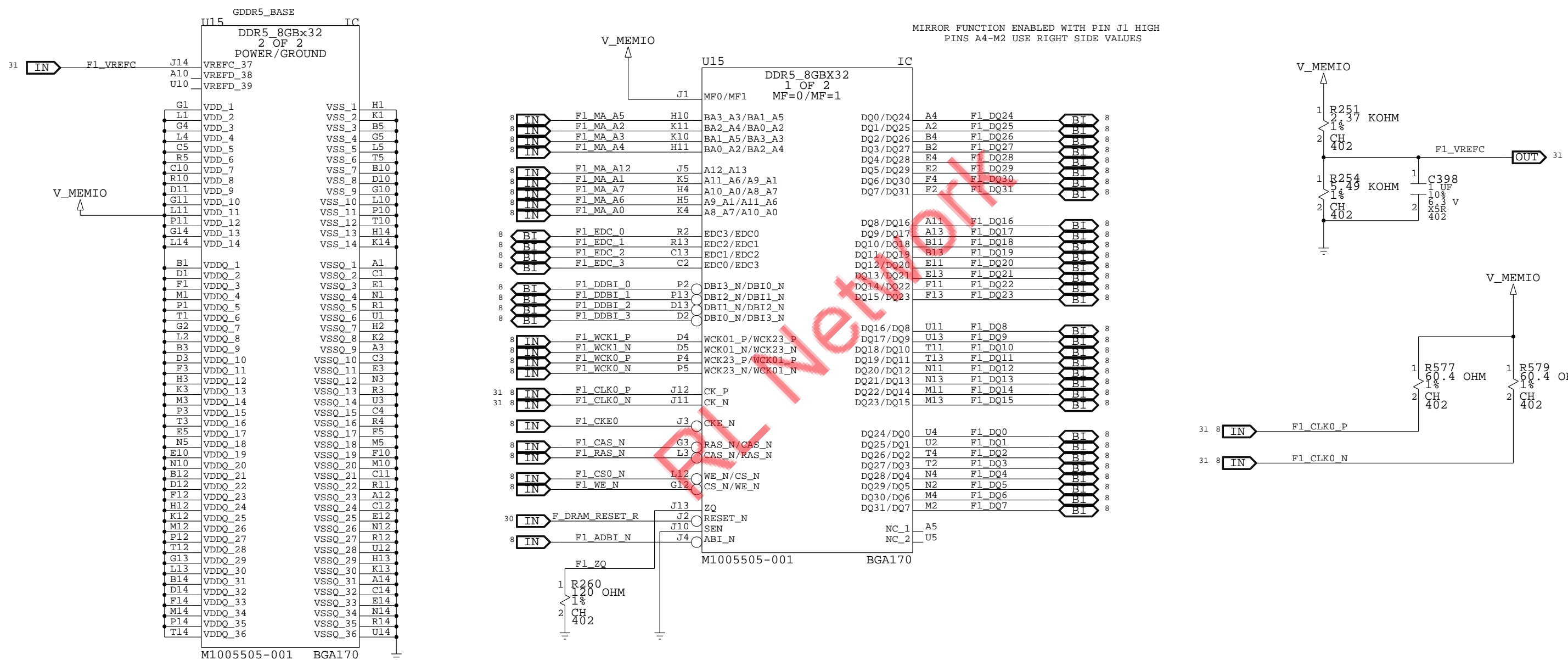
MEMORY: CHANNEL E1



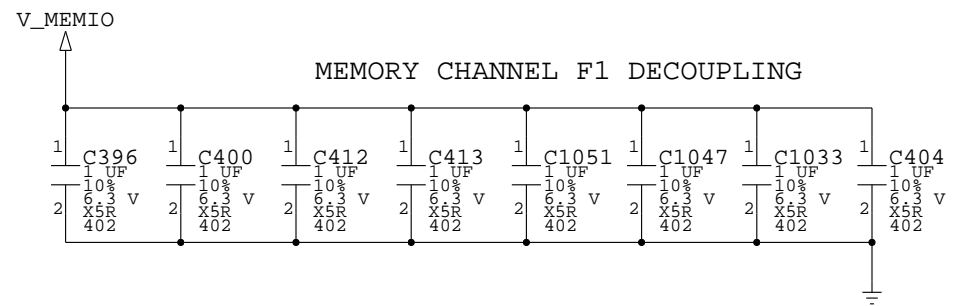
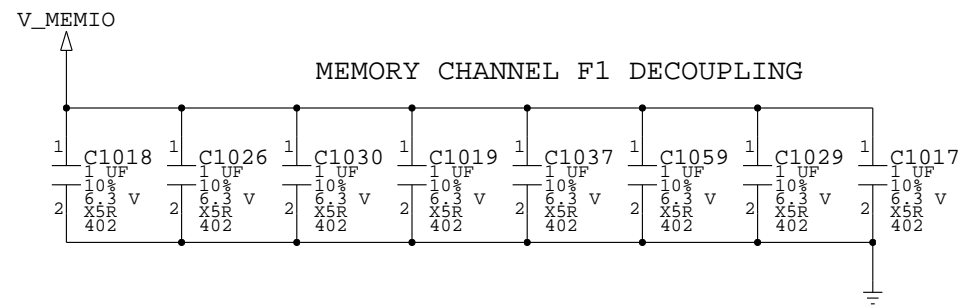
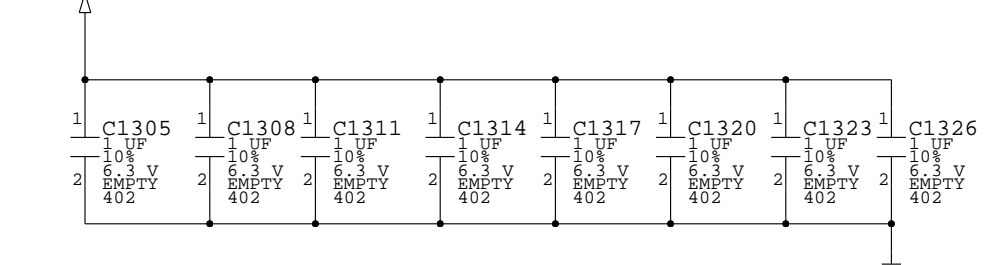
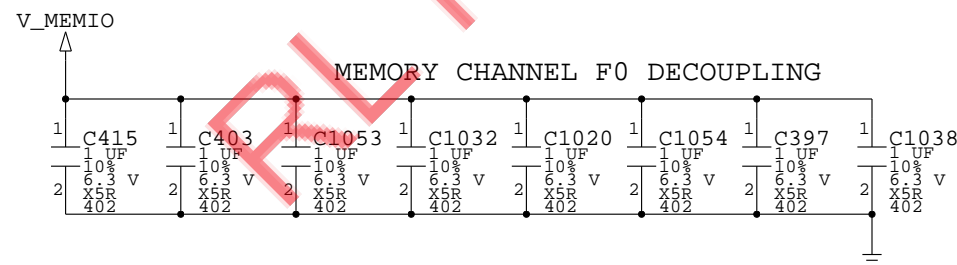
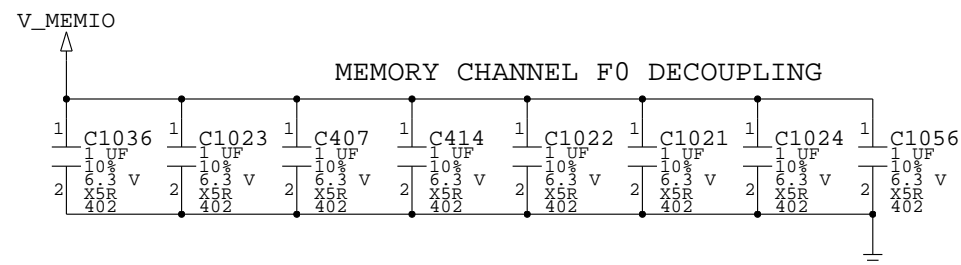
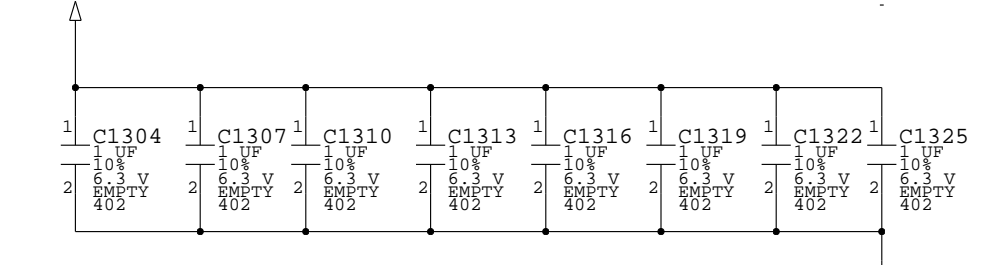
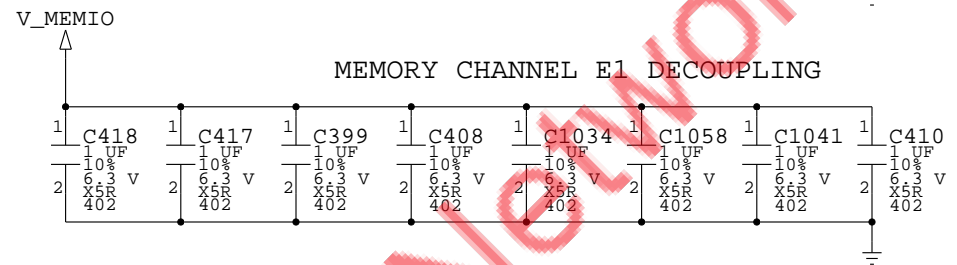
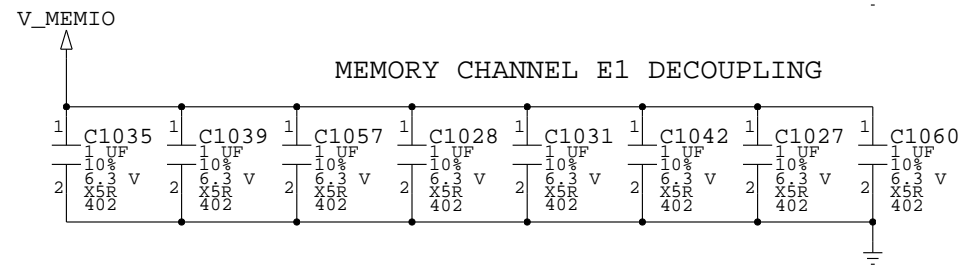
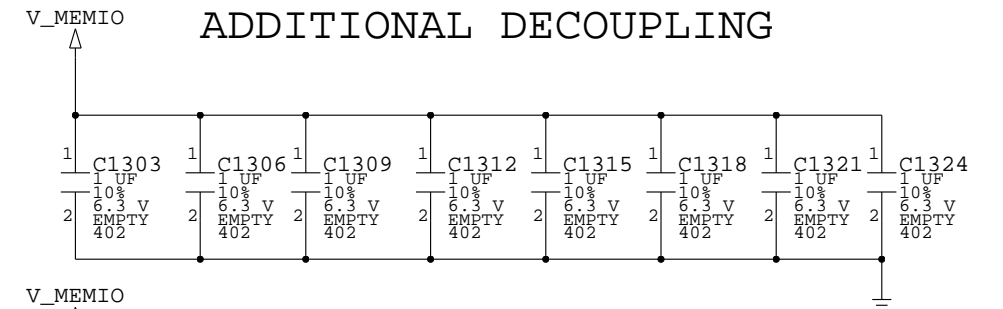
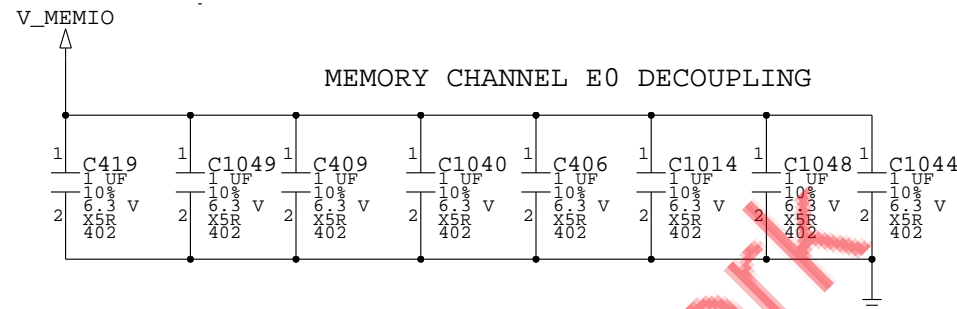
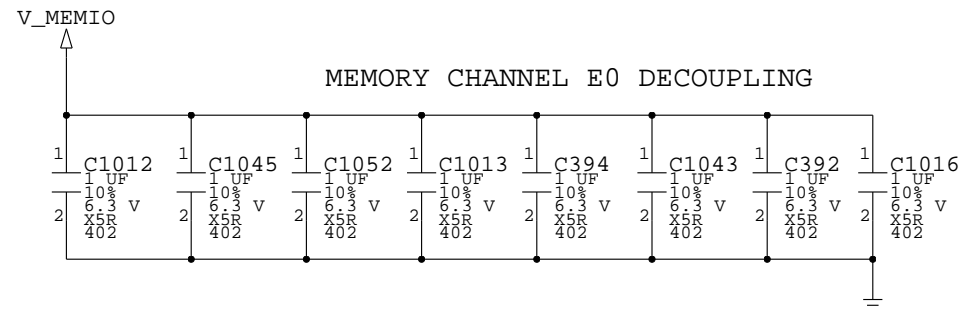
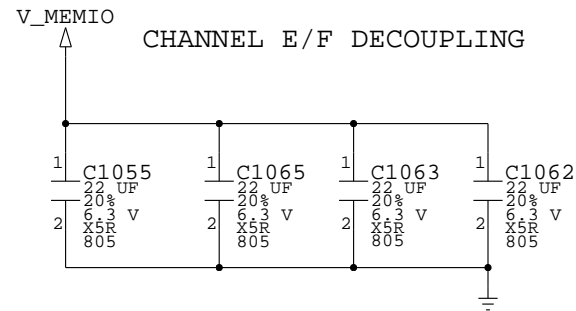
MEMORY: CHANNEL F0



MEMORY: CHANNEL F1



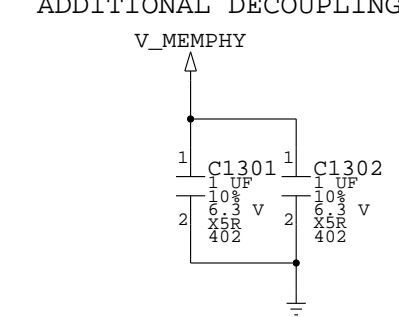
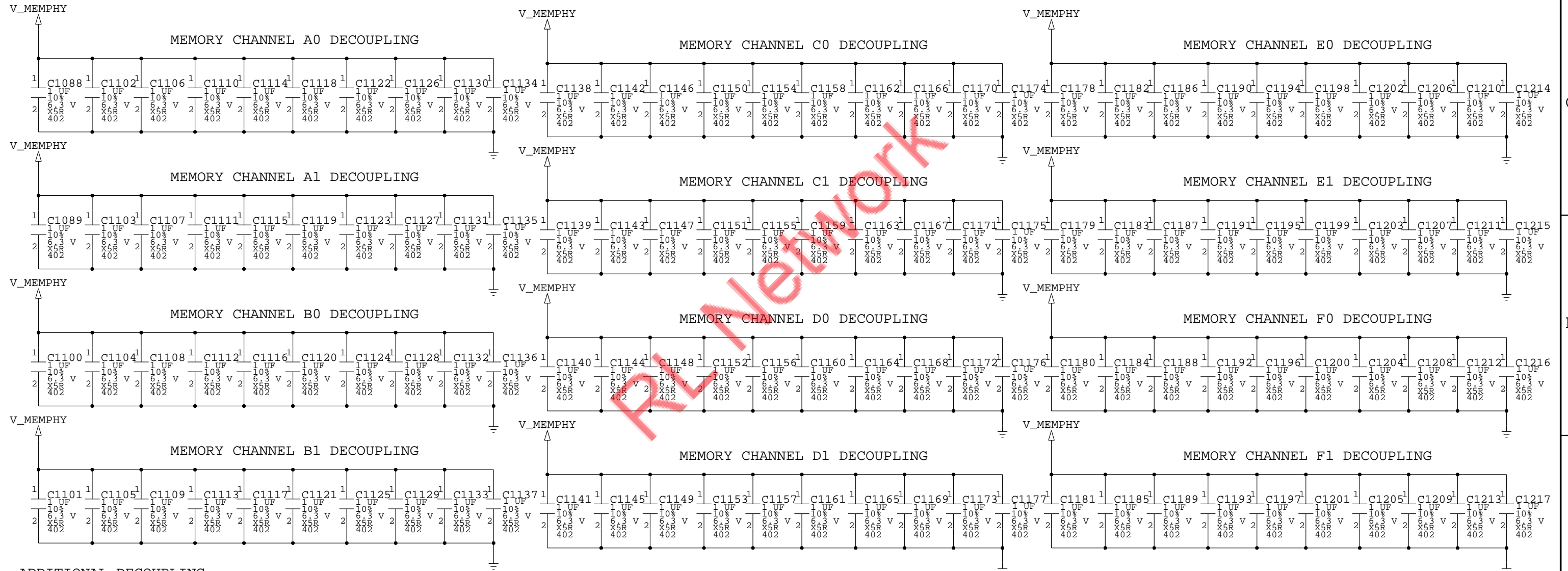
MEMORY: CHANNEL E/F DECOUPLING



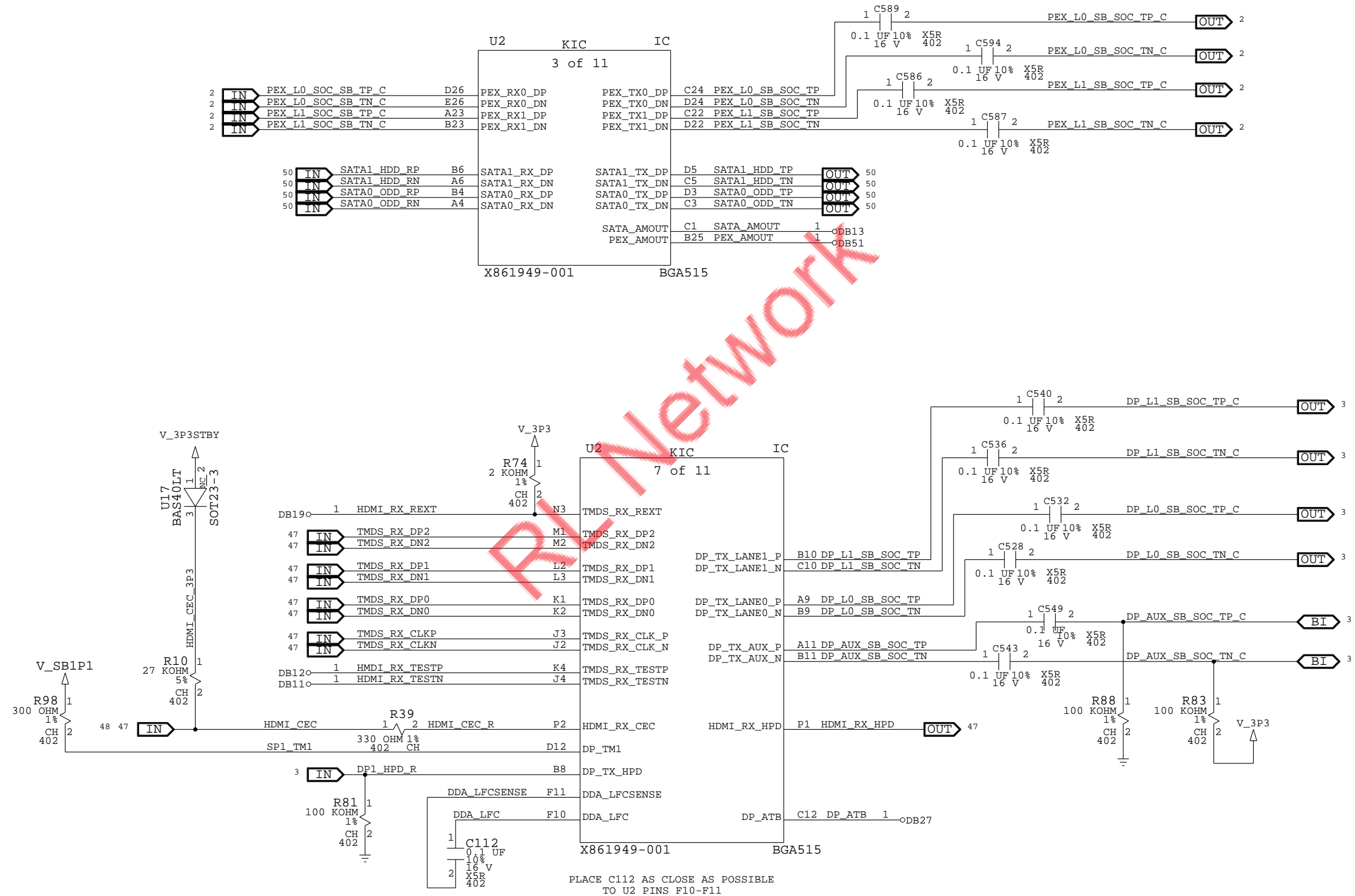
NOTE: ADDITIONAL MEMORY DECOUPLING ON PAGE 33

MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 32/82	CSA PAGE 32/82	FAB G-R	VER 0.99L
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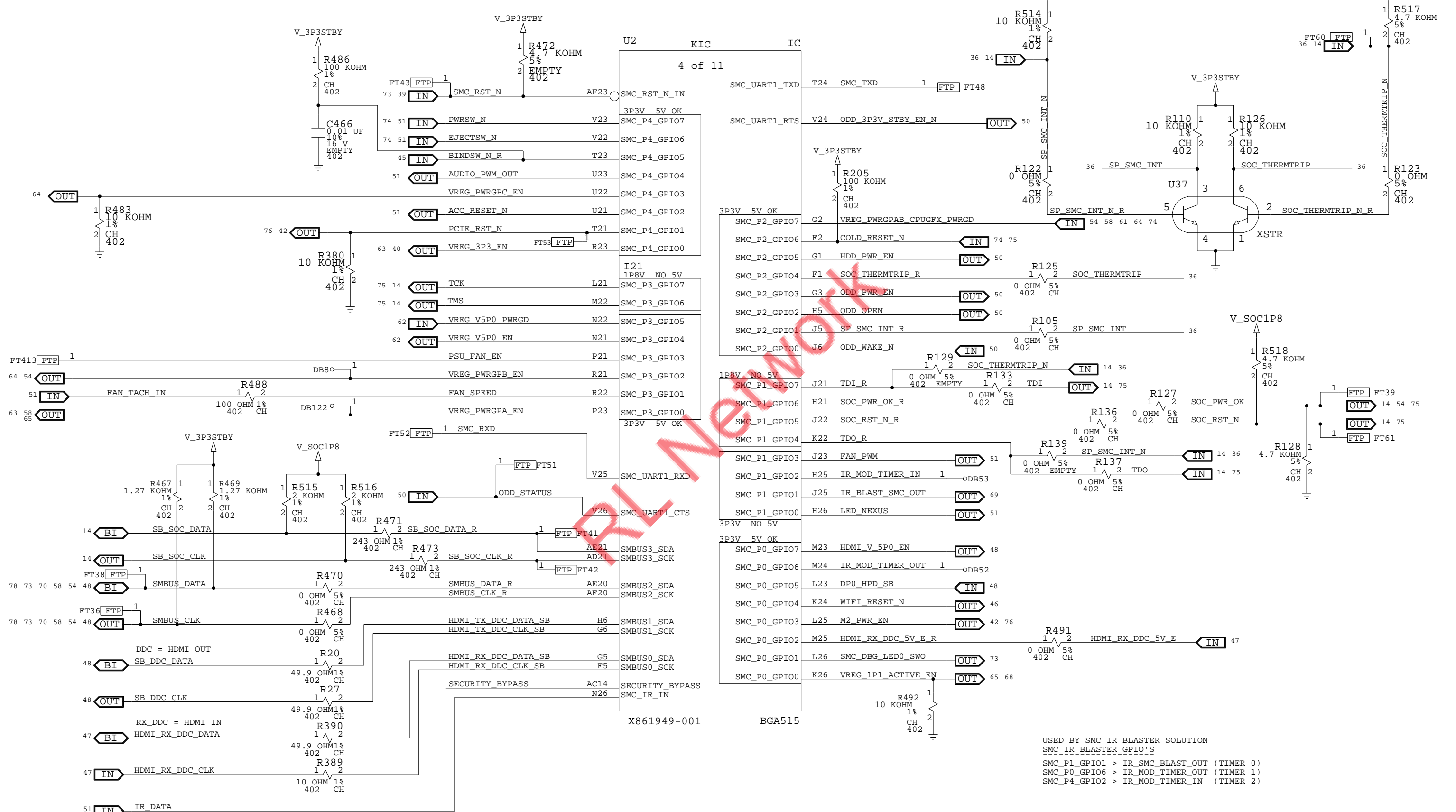
MEMORY: ADDITIONAL DECOUPLING



KIC: PCIE, SATA, VIDEO



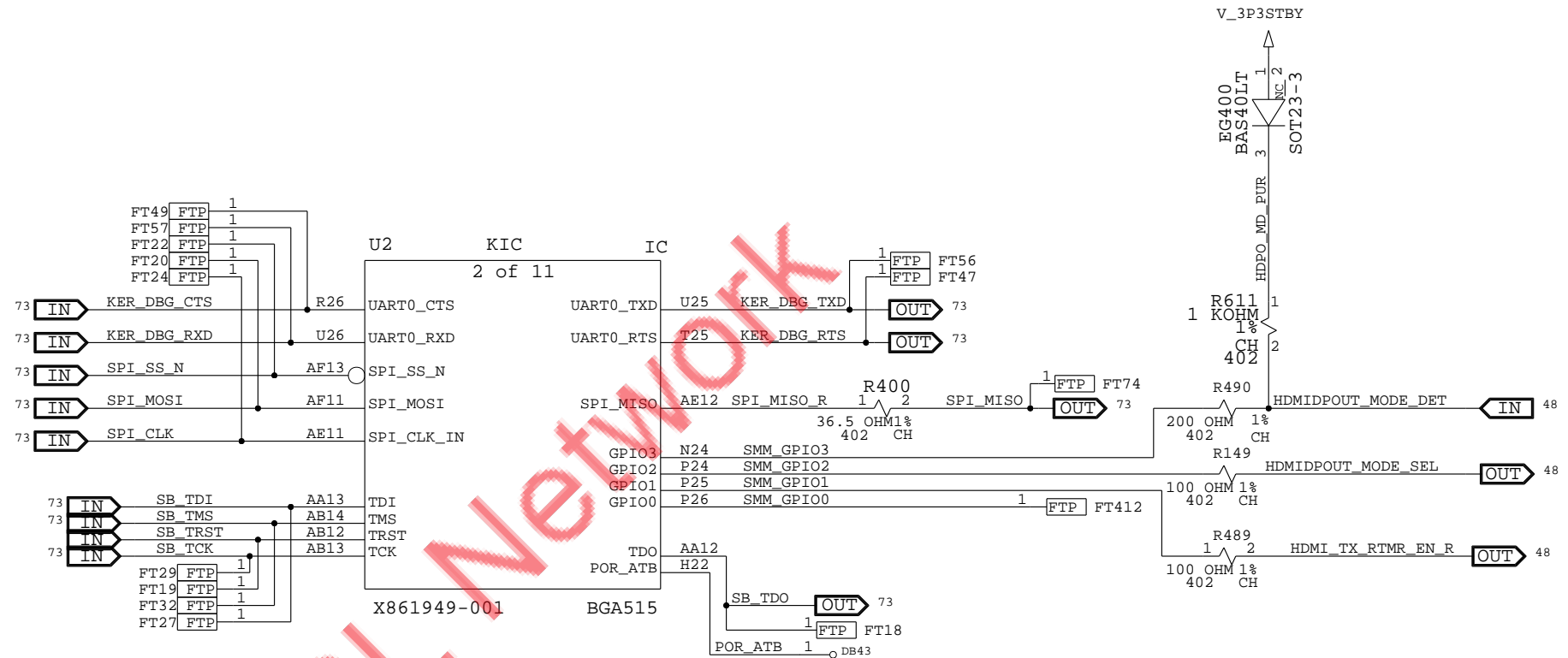
KIC: SMC



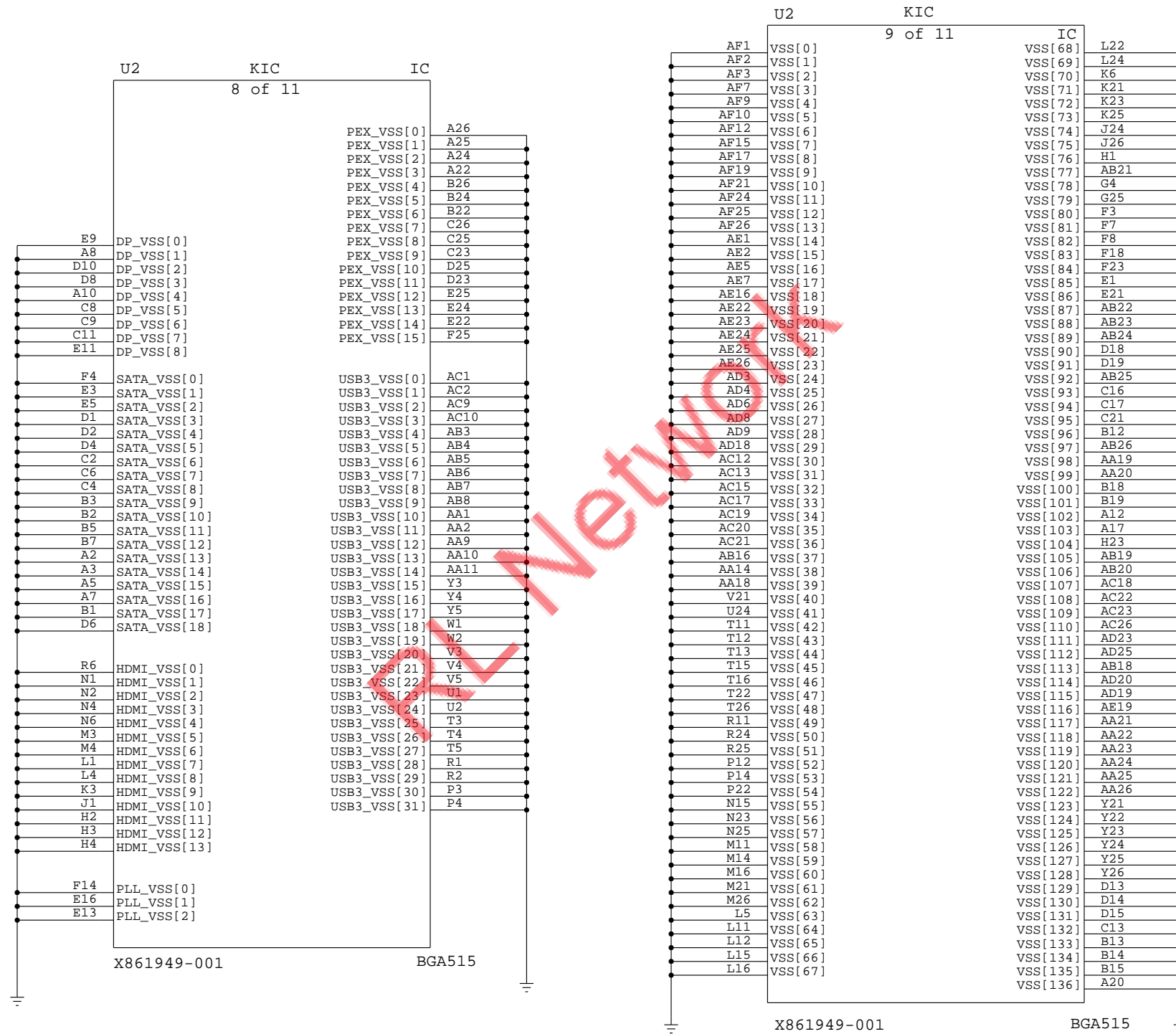
USED BY SMC IR BLASTER SOLUTION
 SMC_IR_BLASTER_GPIO'S
 SMC_P1_GPIO1 > IR_SMC_BLAST_OUT (TIMER 0)
 SMC_P0_GPIO6 > IR_MOD_TIMER_OUT (TIMER 1)
 SMC_P4_GPIO2 > IR_MOD_TIMER_IN (TIMER 2)

MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 36/82	CSA PAGE 36/82	FAB G-R	VER 0.99L
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KIC: FACET

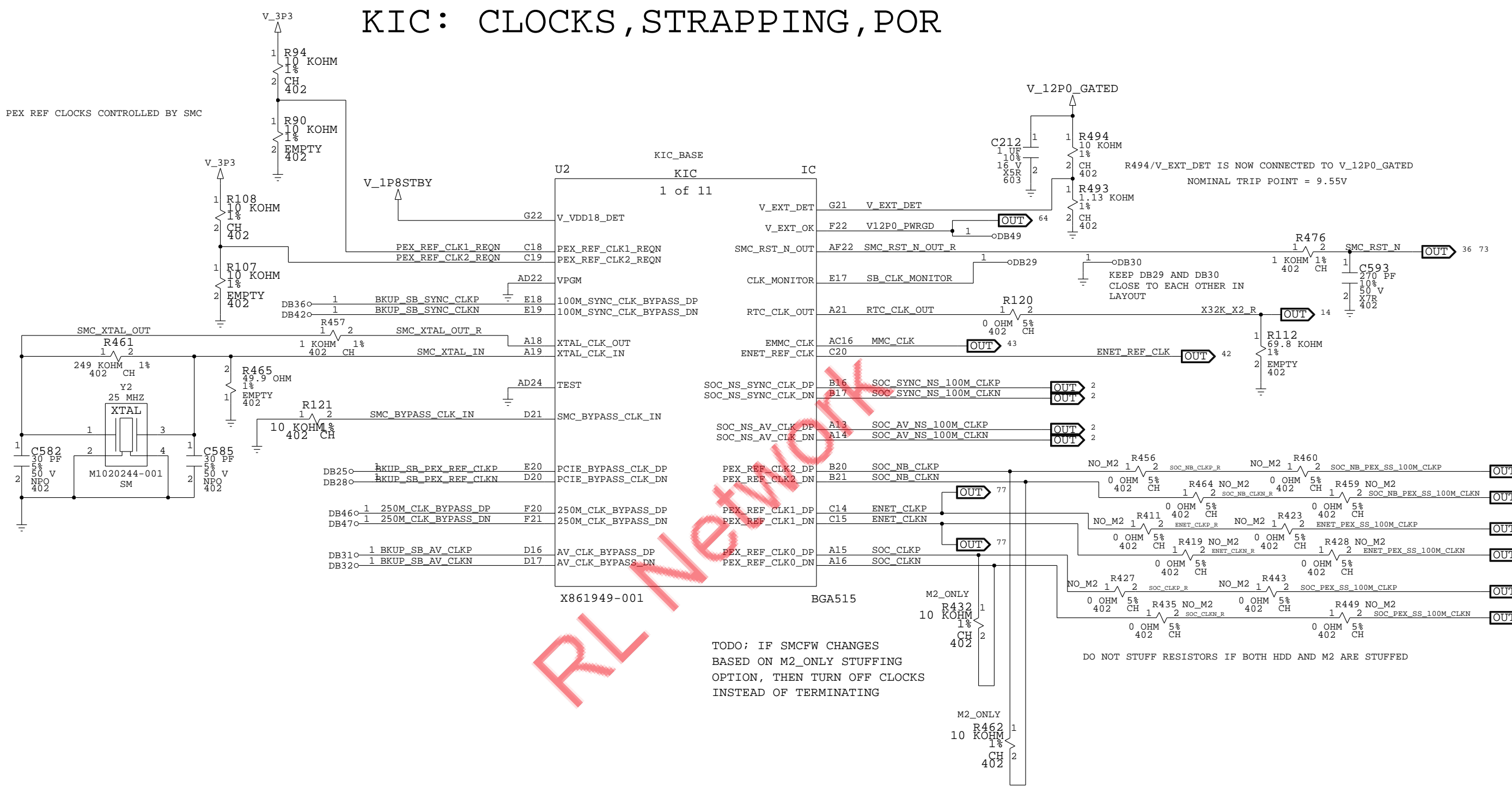


KIC: POWER



KIC: CLOCKS, STRAPPING, POR

PEX REF CLOCKS CONTROLLED BY SMC



TODO; IF SMC FW CHANGES
BASED ON M2_ONLY STUFFING
OPTION, THEN TURN OFF CLOCKS
INSTEAD OF TERMINATING

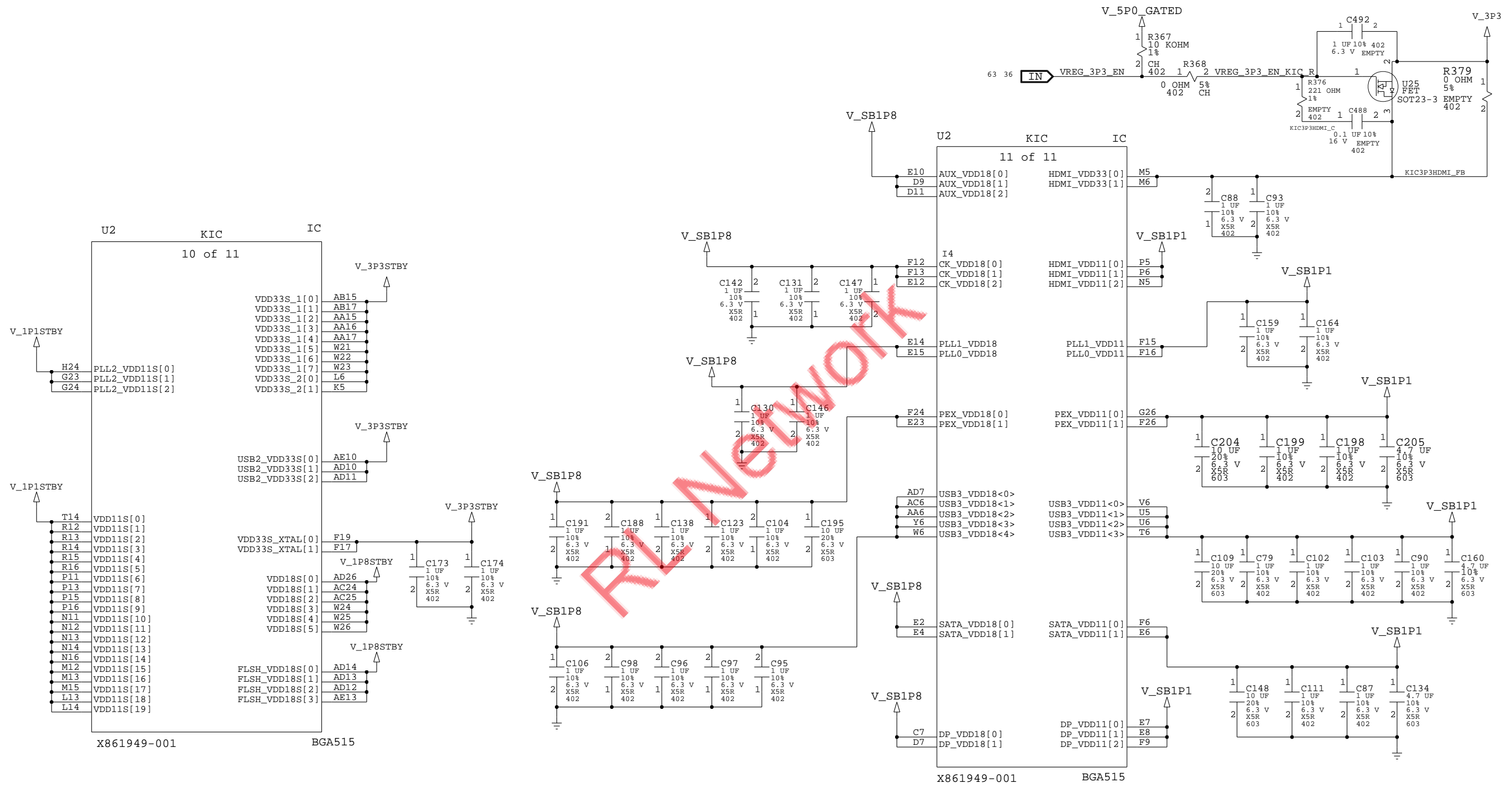
DO NOT STUFF RESISTORS IF BOTH HDD AND M2 ARE STUFFED

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X861949-007	IC	U2	IC, KRAKEN SB, BGA515	KIC_RETAIL
X861949-008	IC	U2	IC, KRAKEN SB, BGA515	KIC_DEV
X861949-008	EMPTY	U2	IC, KRAKEN SB, BGA515	KIC_EMPTY

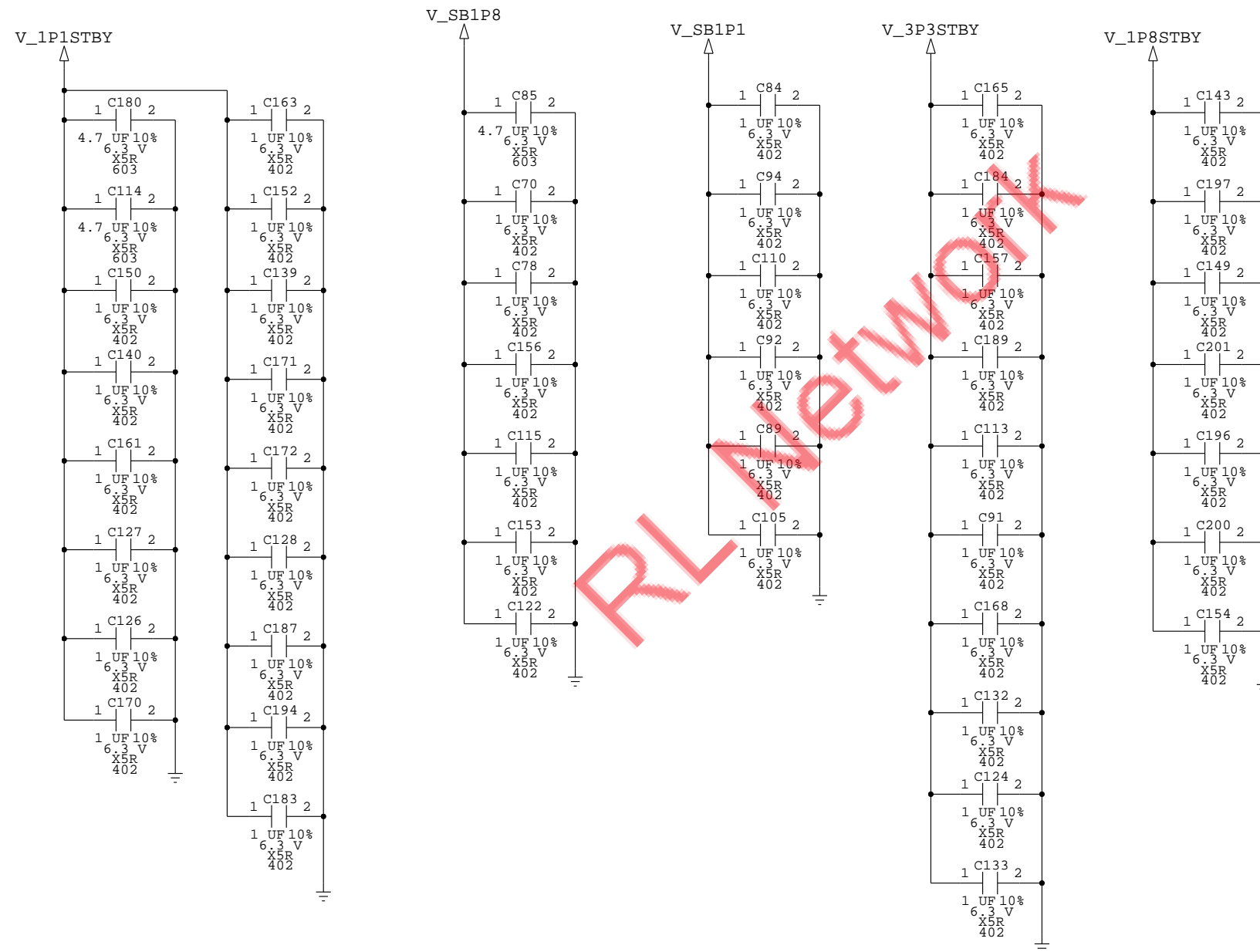
MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 39/82	CSA PAGE 39/82	FAB G-R	VER 0.99L
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KIC: POWER

FET PREVENTS LEAKAGE THROUGH KRAKEN
FROM STANDBY RAILS TO 3P3 RAIL

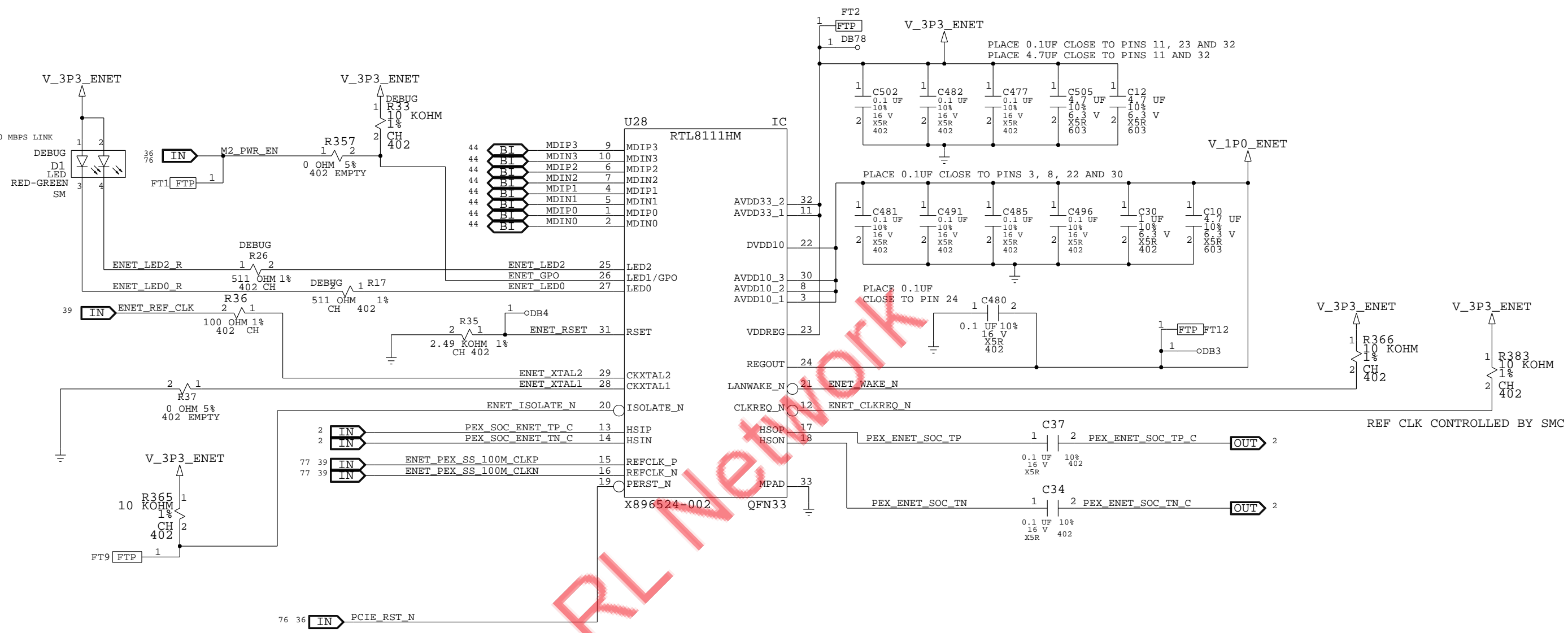


KIC: DECOUPLING

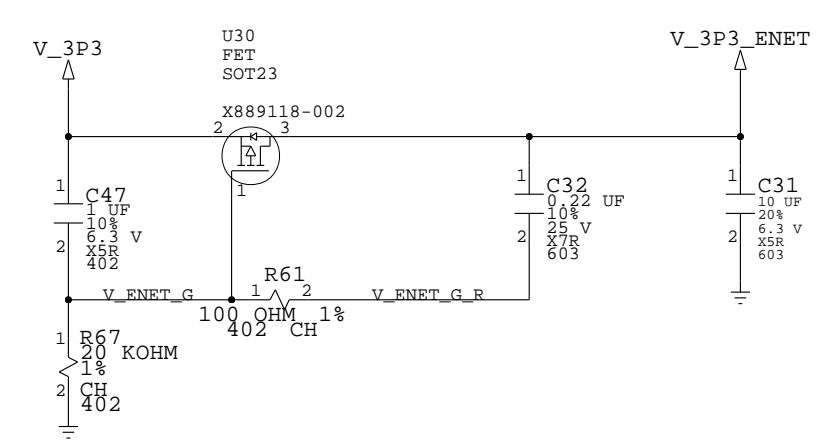


ETHERNET CONTROLLER

RED = 1 GBPS LINK
GREEN = 10 MBPS LINK
NO INDICATION FOR 100 MBPS LINK



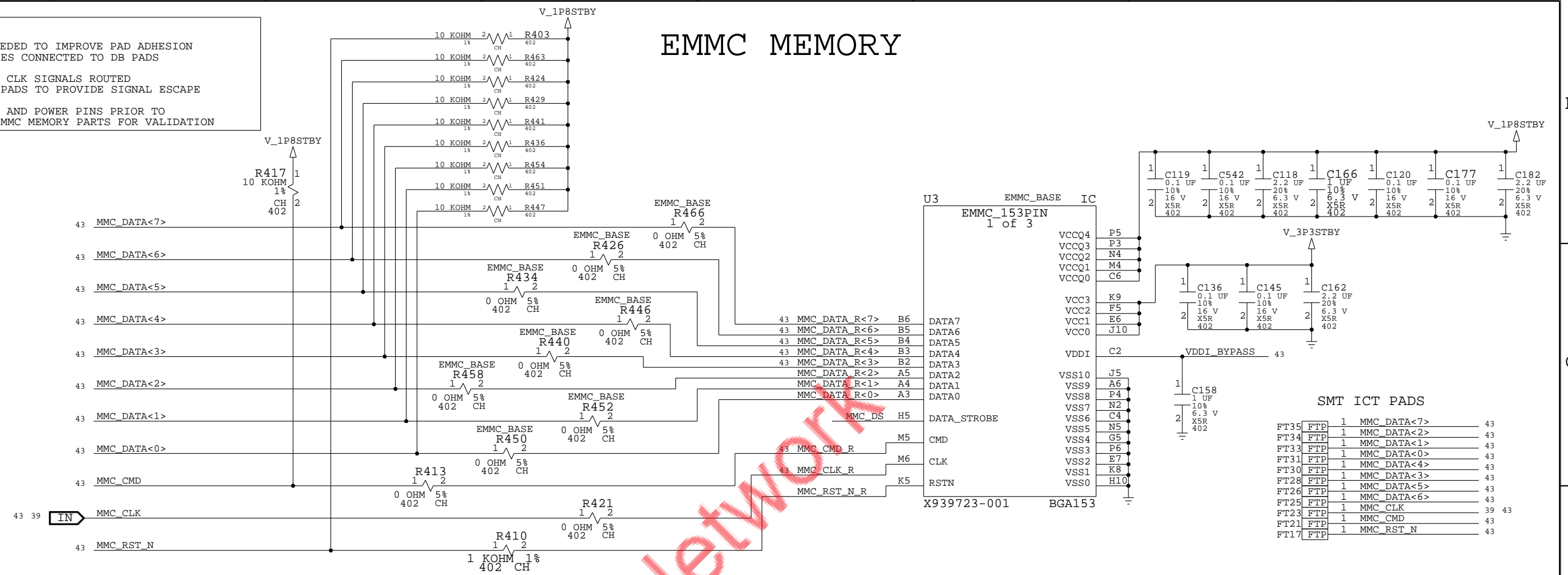
SOFT START
NOM. VOLTAGE: 3.3V
MAX POWER: 590MW



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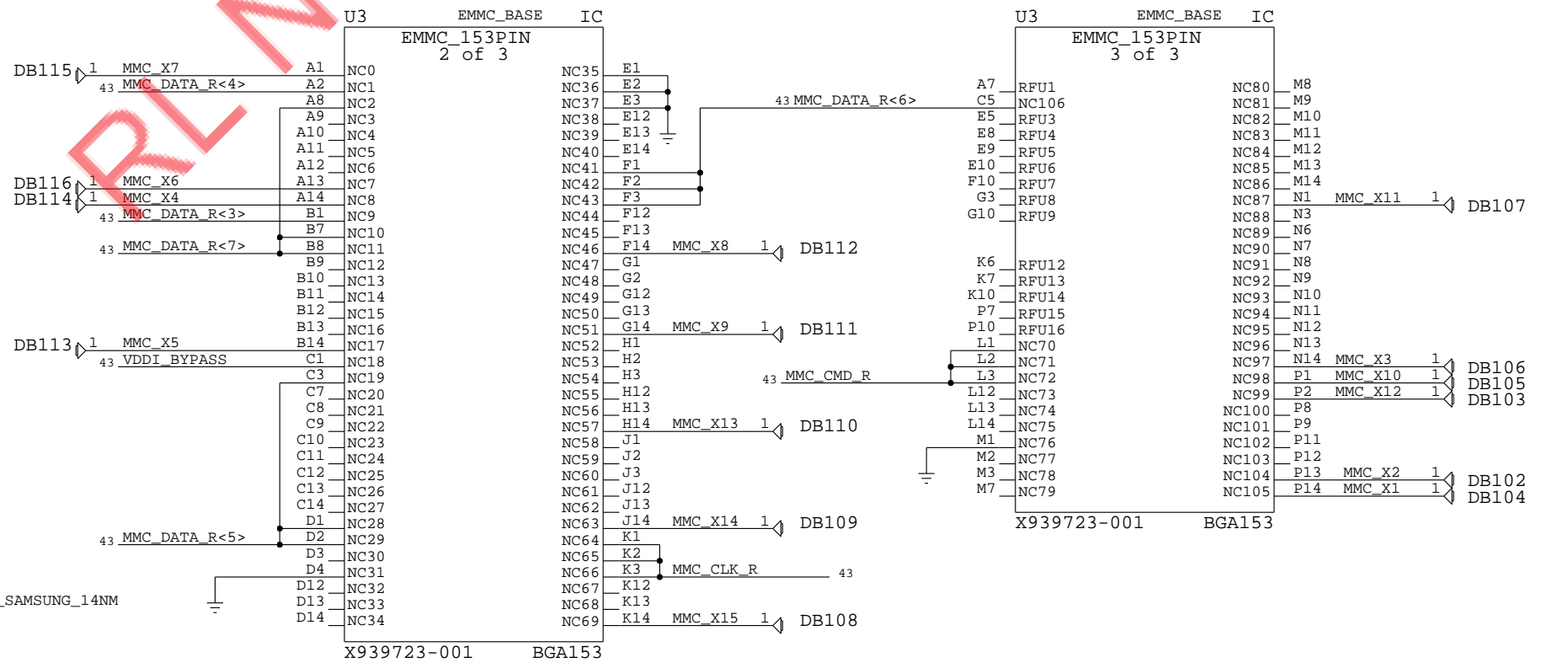
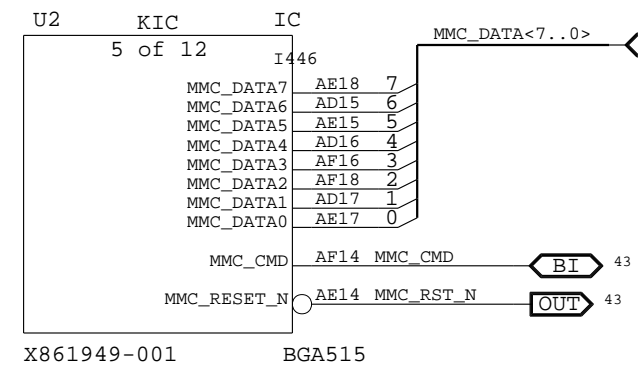
EMMC MEMORY

NOTES:
 1. MMC_X NETS ARE NEEDED TO IMPROVE PAD ADHESION USING 13 MIL TRACES CONNECTED TO DB PADS
 2. EMMC DATA, CMD AND CLK SIGNALS ROUTED THROUGH MULTIPLE PADS TO PROVIDE SIGNAL ESCAPE
 3. VERIFY ALL SIGNAL AND POWER PINS PRIOR TO CONSIDERING NEW EMMC MEMORY PARTS FOR VALIDATION



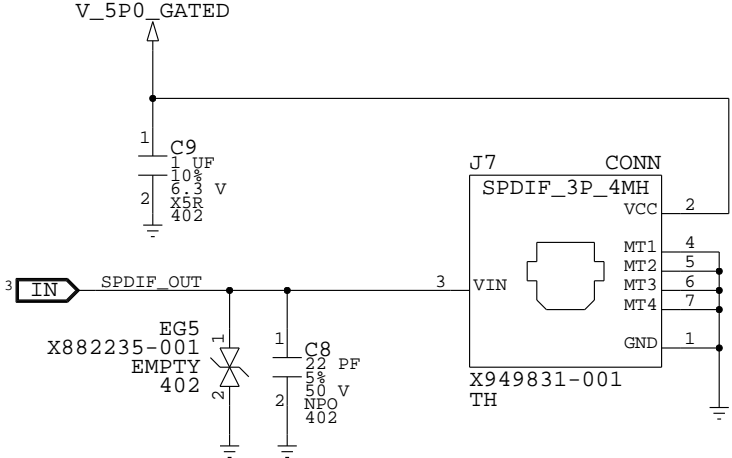
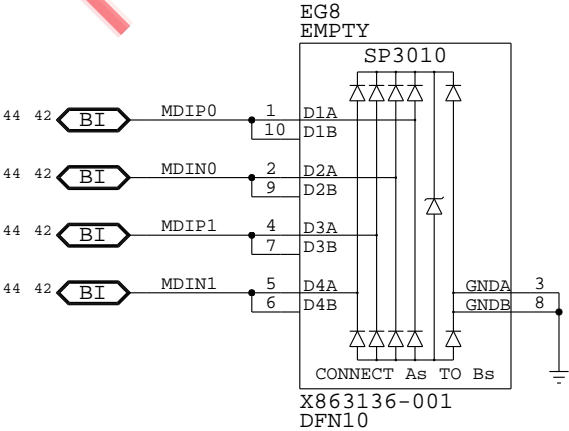
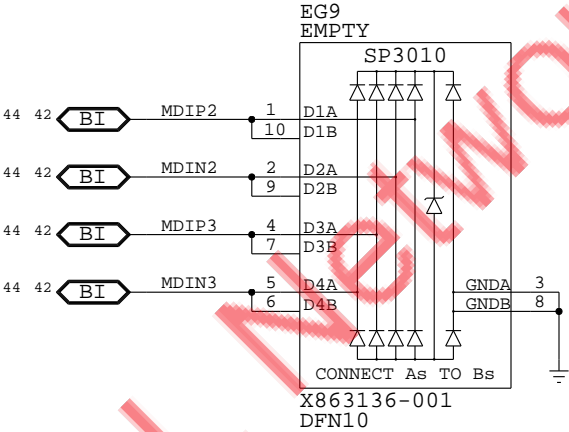
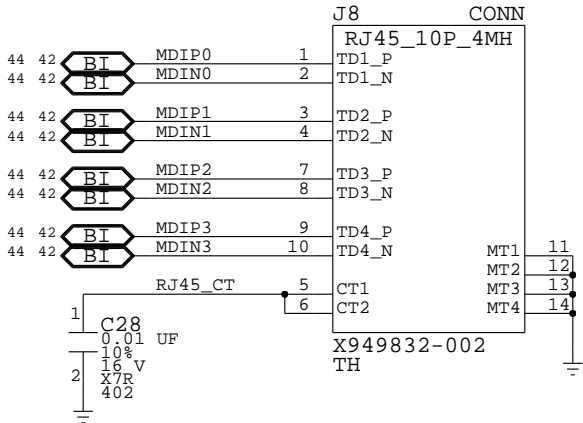
SMT ICT PADS

FT35	FTP	1	MMC_DATA<7>	43
FT34	FTP	1	MMC_DATA<2>	43
FT33	FTP	1	MMC_DATA<1>	43
FT30	FTP	1	MMC_DATA<0>	43
FT31	FTP	1	MMC_DATA<4>	43
FT30	FTP	1	MMC_DATA<3>	43
FT28	FTP	1	MMC_DATA<5>	43
FT26	FTP	1	MMC_DATA<6>	43
FT25	FTP	1	MMC_CLK	43
FT23	FTP	1	MMC_CMD	43
FT21	FTP	1	MMC_RST_N	43
FT17	FTP	1	MMC_RST_N	43

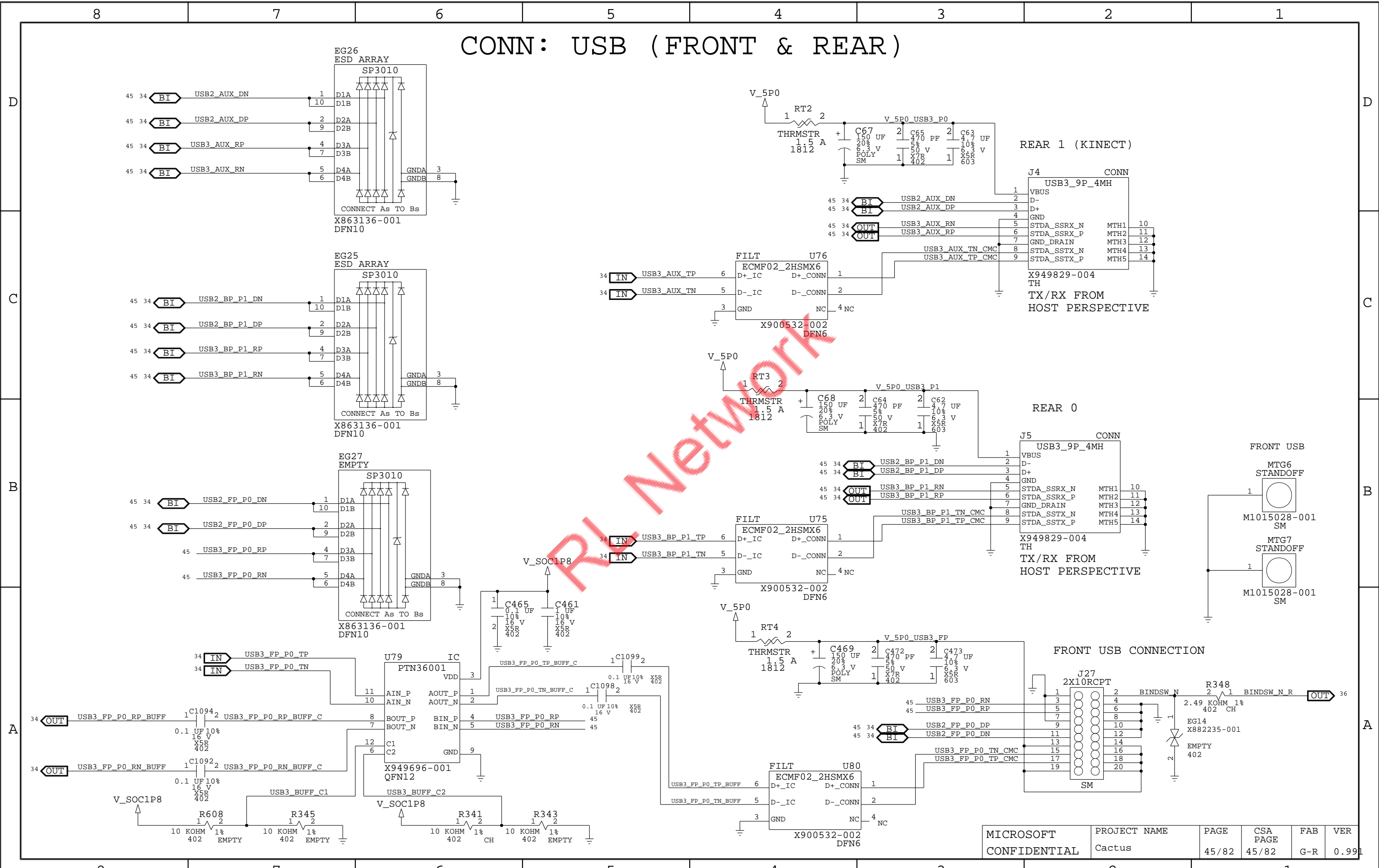


MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
X934261-001	IC	U3	MEM, 8GB, EMMC, FLASH, 15NM, BGA153, TOSHIBA	EMMC_TOSHIBA_15NM
X945540-002	IC	U3	MEM, 8GB, EMMC, FLASH, 14NM, BGA153, SAMSUNG	EMMC_SAMSUNG_14NM
X939723-001	IC	U3	MEM, 8GB, EMMC, FLASH, 16NM, BGA153, HYNIX	EMMC_HYNIX_16NM
X800617-001	RES	R426, R434, R440, R446, R450, R452, R458, R466	49.9 OHM 1%, 1/16W, 0402	EMMC_TOSHIBA_15NM, EMMC_SAMSUNG_14NM
X809936-001	RES	R426, R434, R440, R446, R450, R452, R458, R466	100 OHM 1%, 1/16W, 0402	EMMC_HYNIX_16NM

CONN: RJ45, TOSLINK

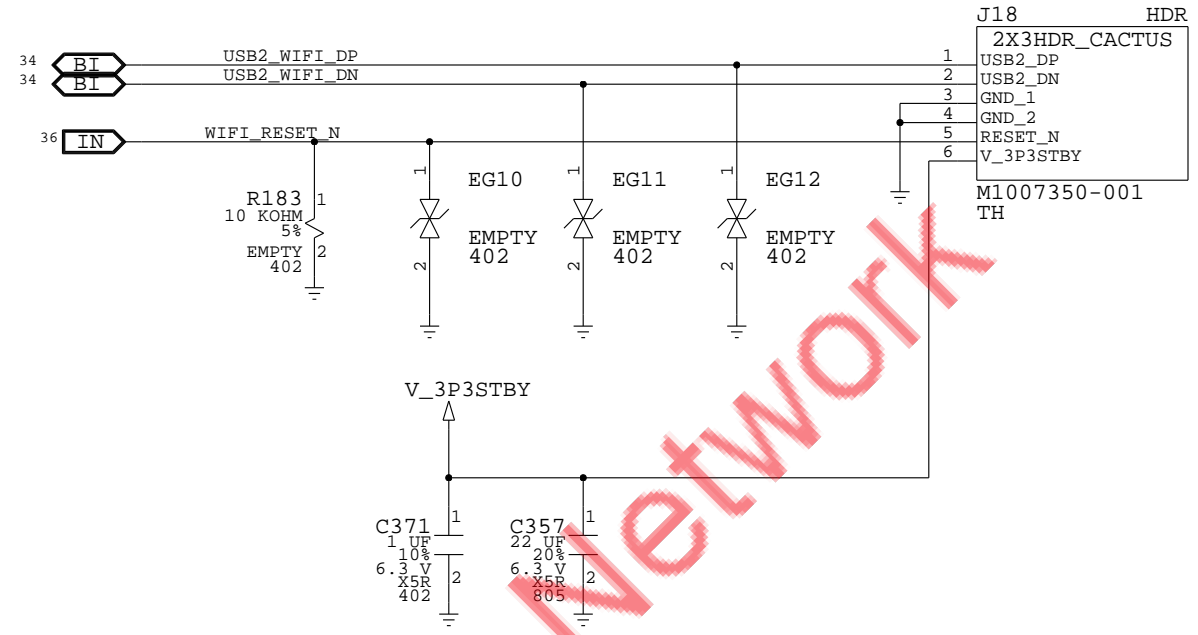


CONN: USB (FRONT & REAR)



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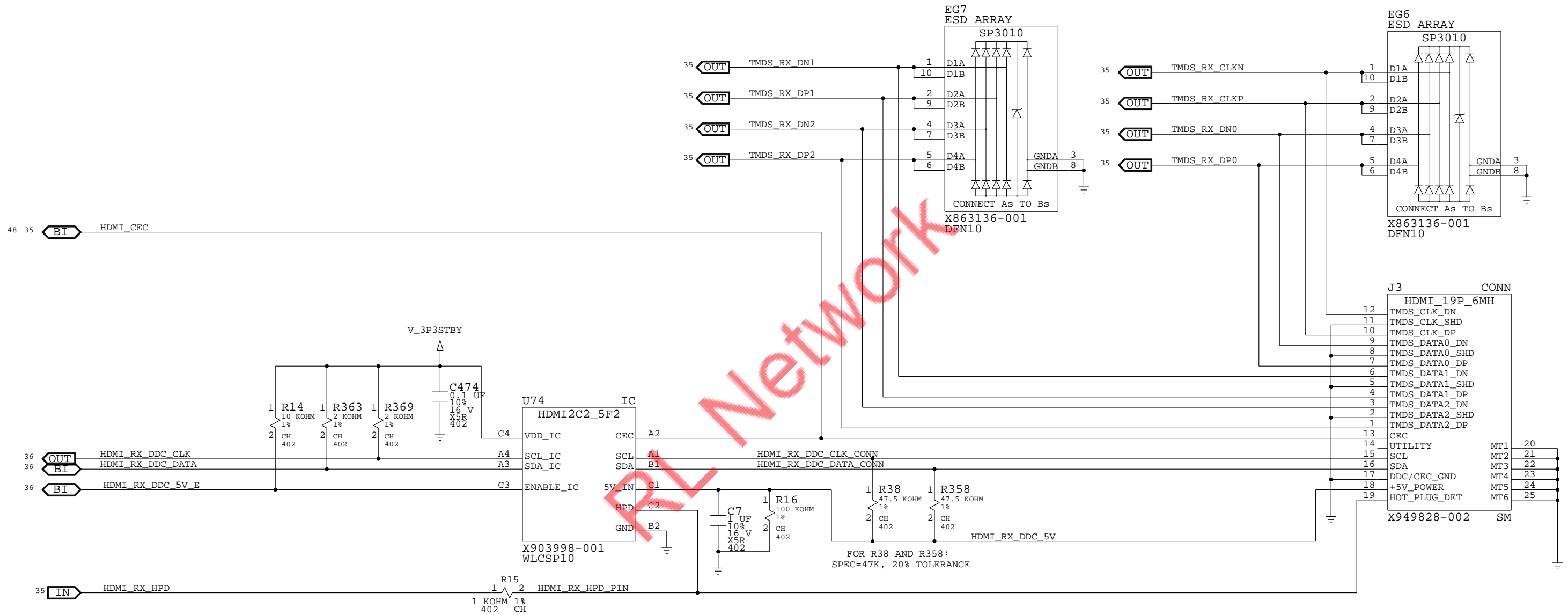
CONN: WIFI



RL Network

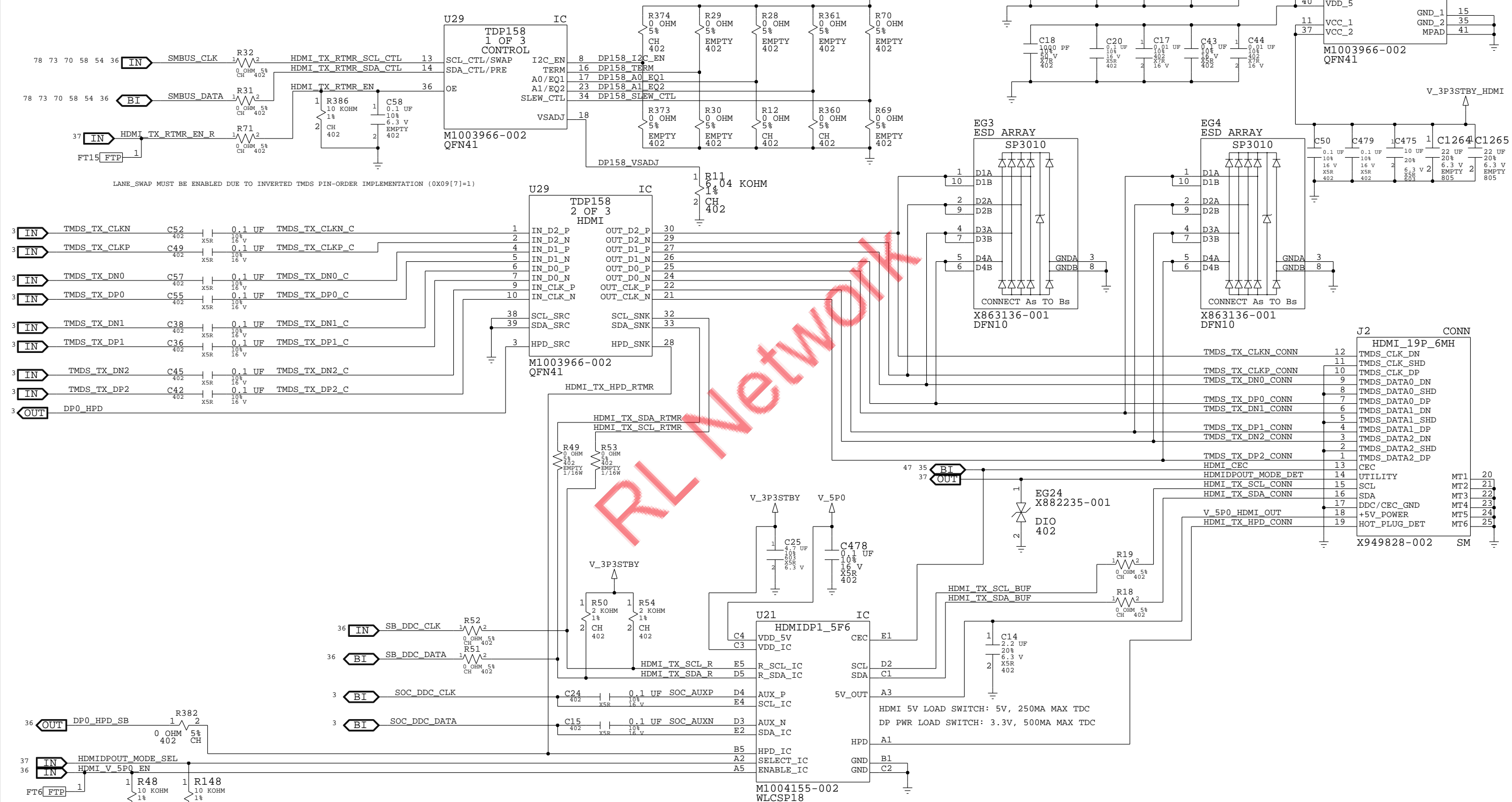
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Cactus	46/82	46/82	G-R	0.99L

CONN: HDMI IN



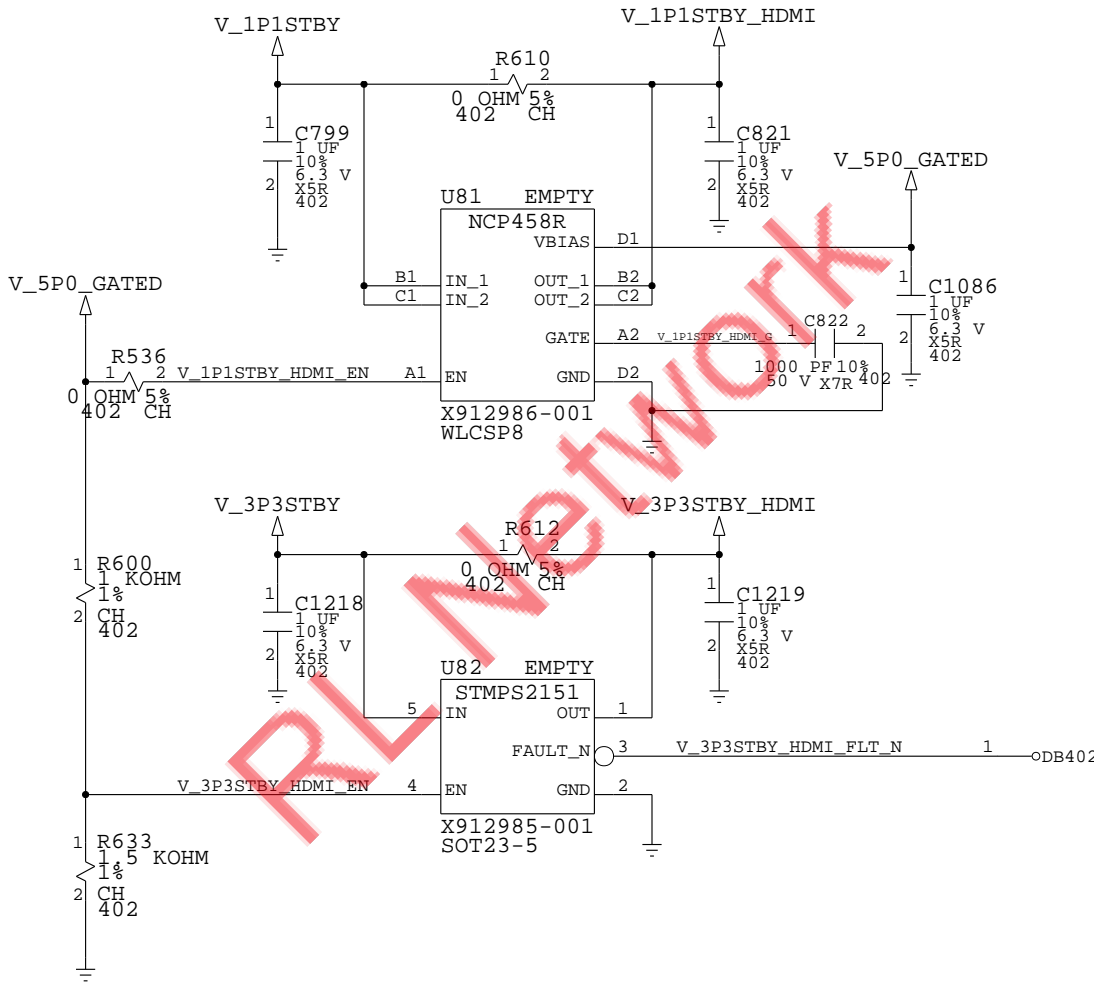
CONN: HDMI OUT

TDP158 CONTROL SLAVE ADDRESS			
SELECTED	A1/A0	7-BIT ADDRESS	8-BIT ADDRESS
---	00	0X5E	BC/BD
	01	0X5D	BA/BB
	10	0X5C	B8/B9
	11	0X5B	B6/B7



LANE_SWAP MUST BE ENABLED DUE TO INVERTED TMDS PIN-ORDER IMPLEMENTATION (0X09[7]=1)

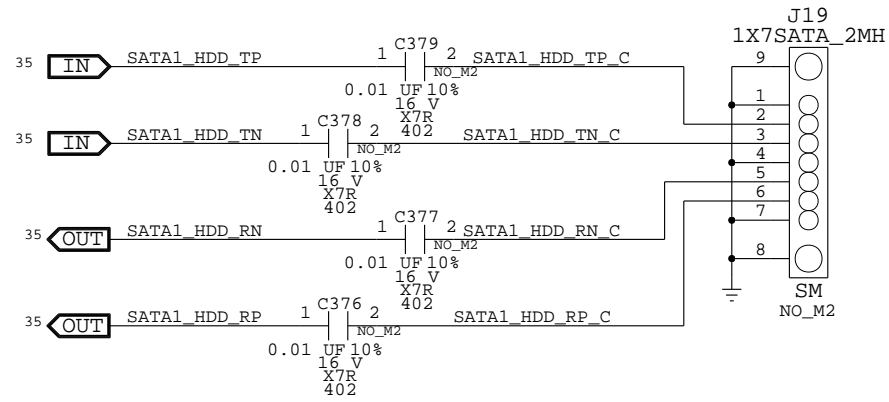
HDMI LOAD SWITCHES



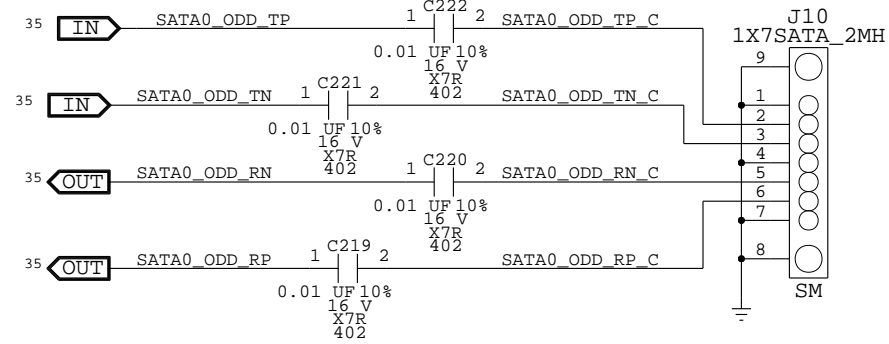
RE-DRIVER	U29	R610	R612	U81	U82
Pg1.0	M1003966-001	EMPTY	EMPTY	STUFF	STUFF
Pg1.1	M1003966-002	STUFF	STUFF	EMPTY	EMPTY

CONN: ODD & HDD

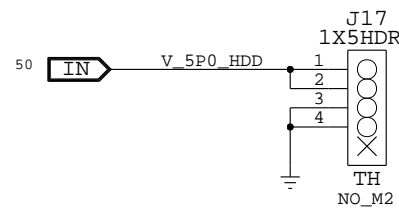
HDD SATA



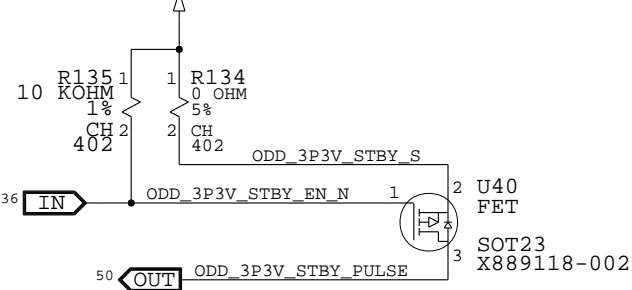
ODD SATA



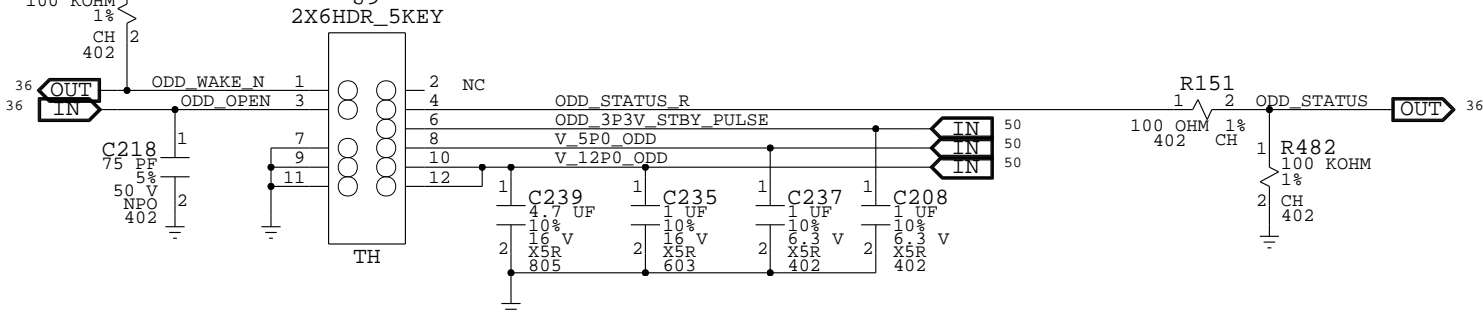
HDD POWER



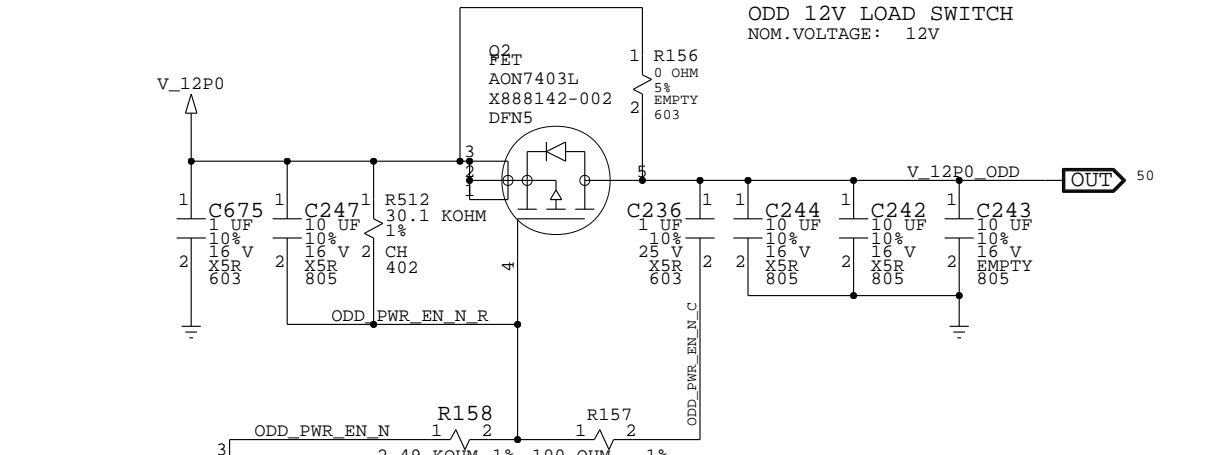
ODD 3P3V STBY



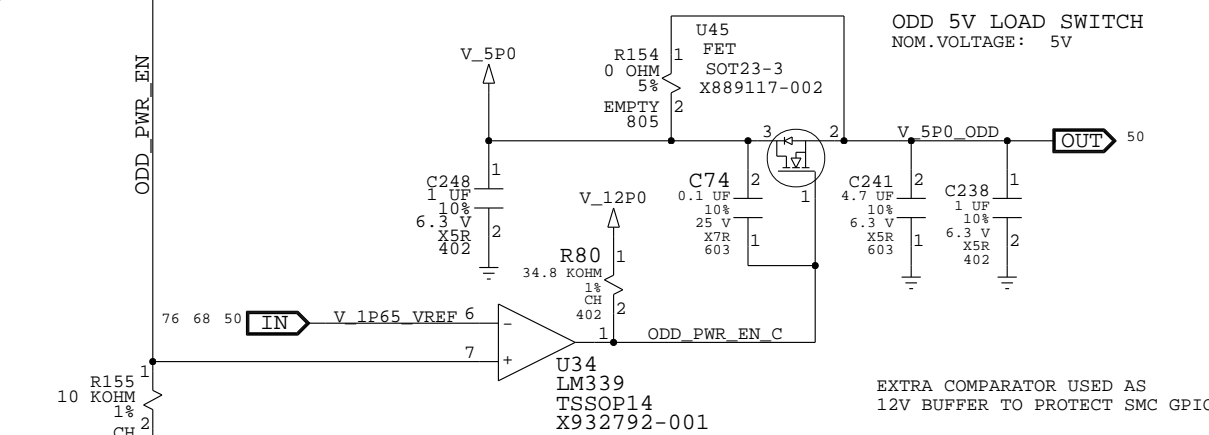
ODD POWER & GPIOs



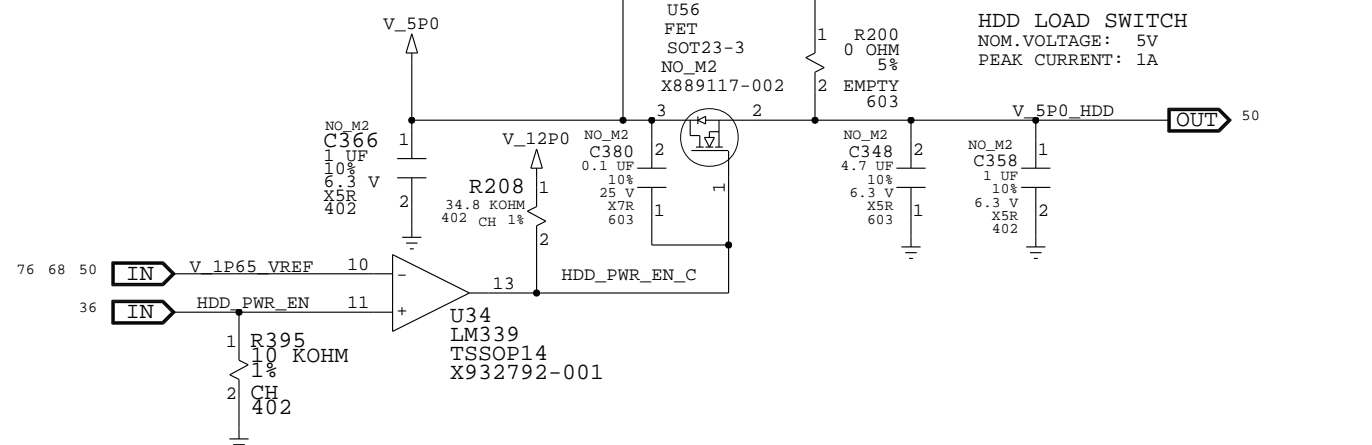
ODD 12V LOAD SWITCH



ODD 5V LOAD SWITCH

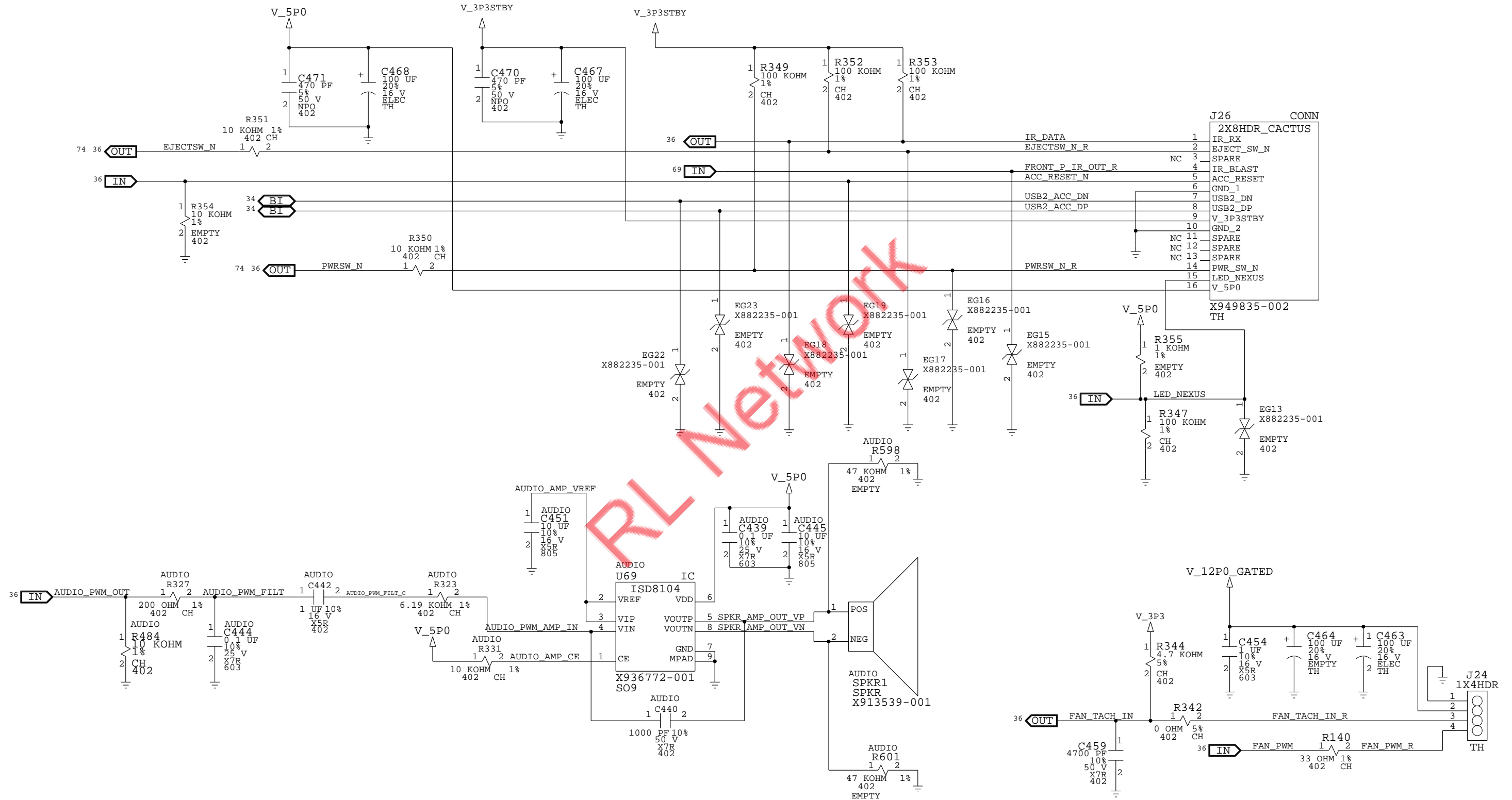


HDD LOAD SWITCH

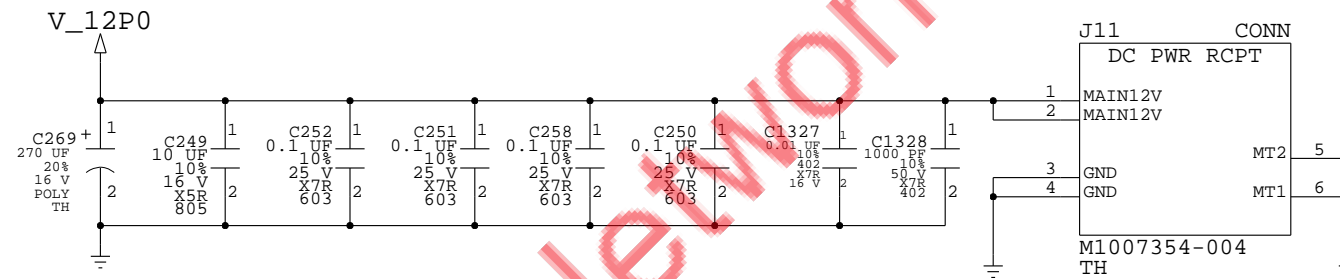


MICROSOFT CONFIDENTIAL	PROJECT NAME Cactus	PAGE 50/82	CSA PAGE 50/82	FAB G-R	VER 0.99L
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CONN: FRONT PANEL, FAN, AUDIO



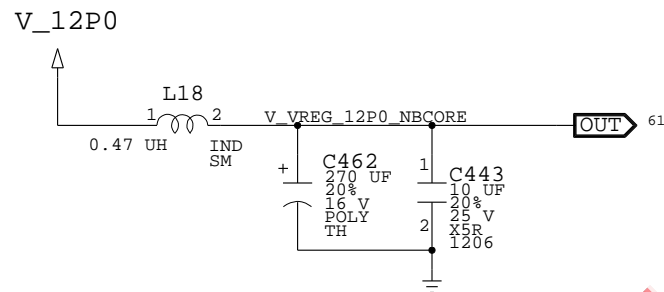
CONN: POWER



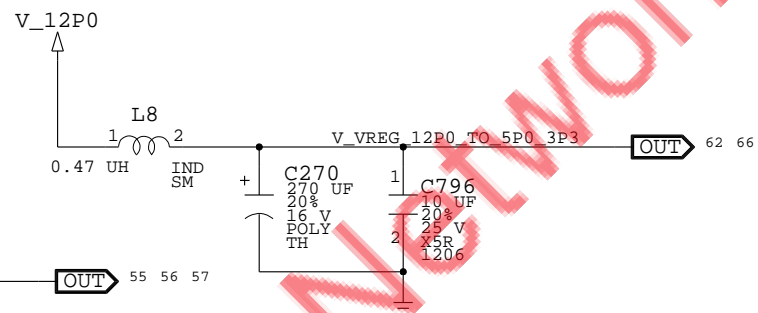
RL NETWORK

VREGS: INPUT AND OUTPUT FILTERS

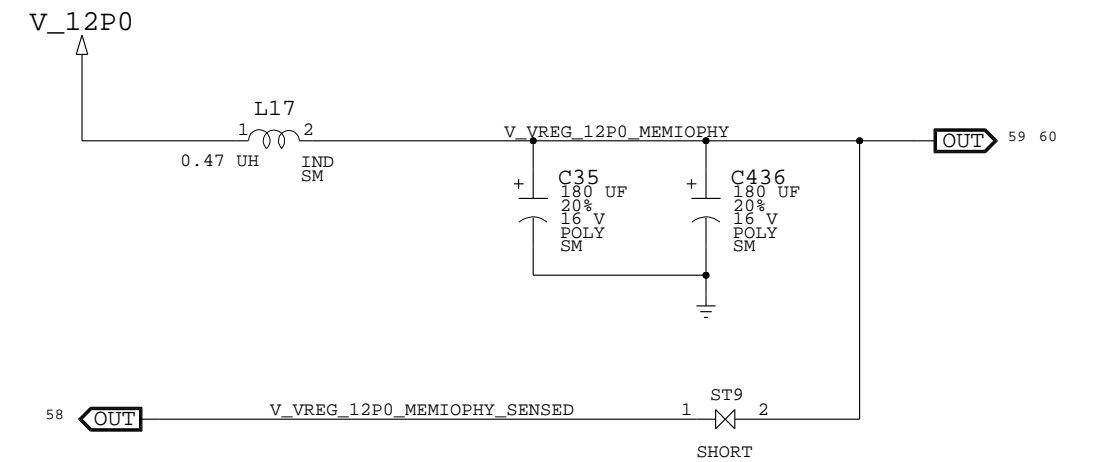
NBCORE INPUT FILTER



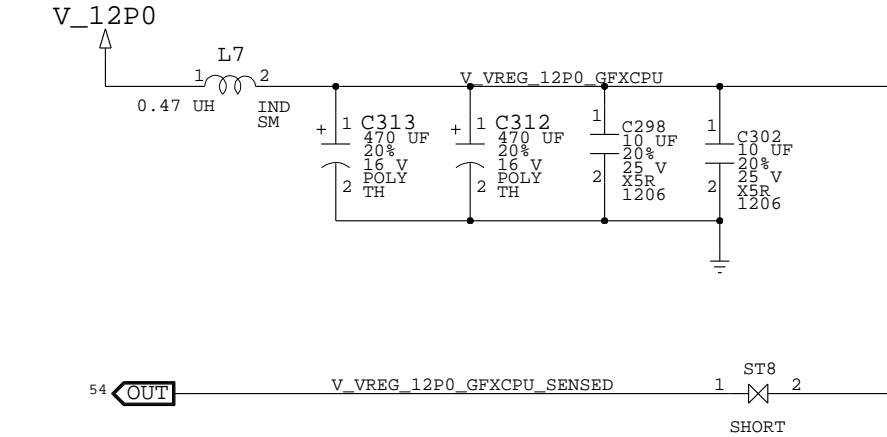
V_5P0 AND V_3P3 INPUT FILTER



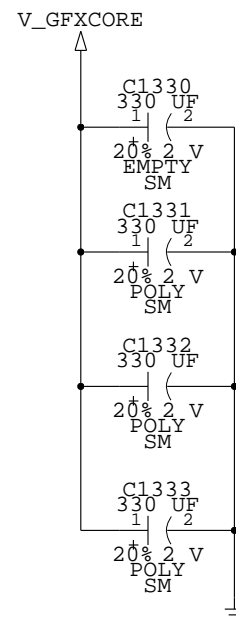
MEMIO/MEMPHY INPUT FILTER



GFX/CPU INPUT FILTER

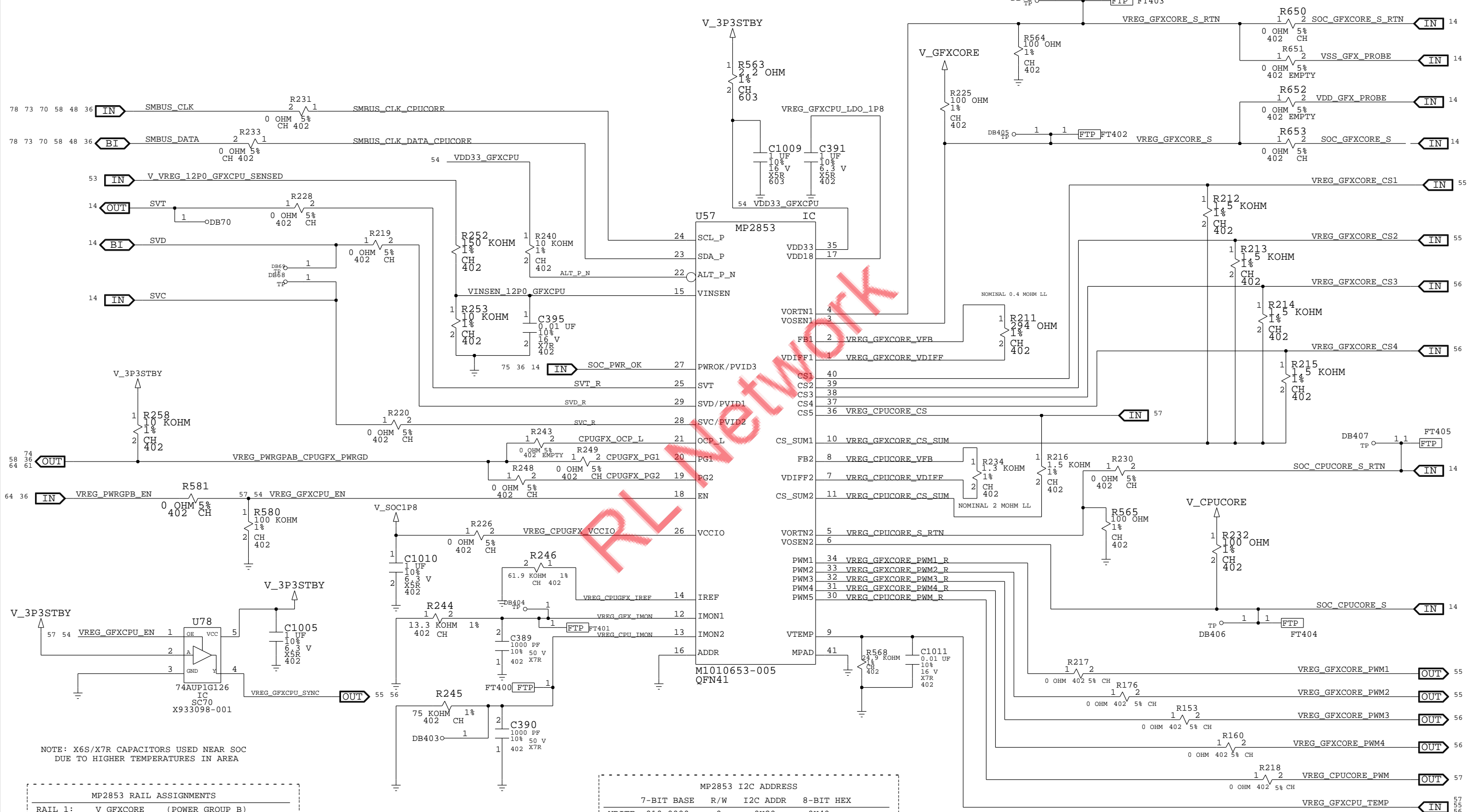


GFXCORE OUTPUT FILTER



VREGS: GFXCORE / CPUCORE

D
C
B
A



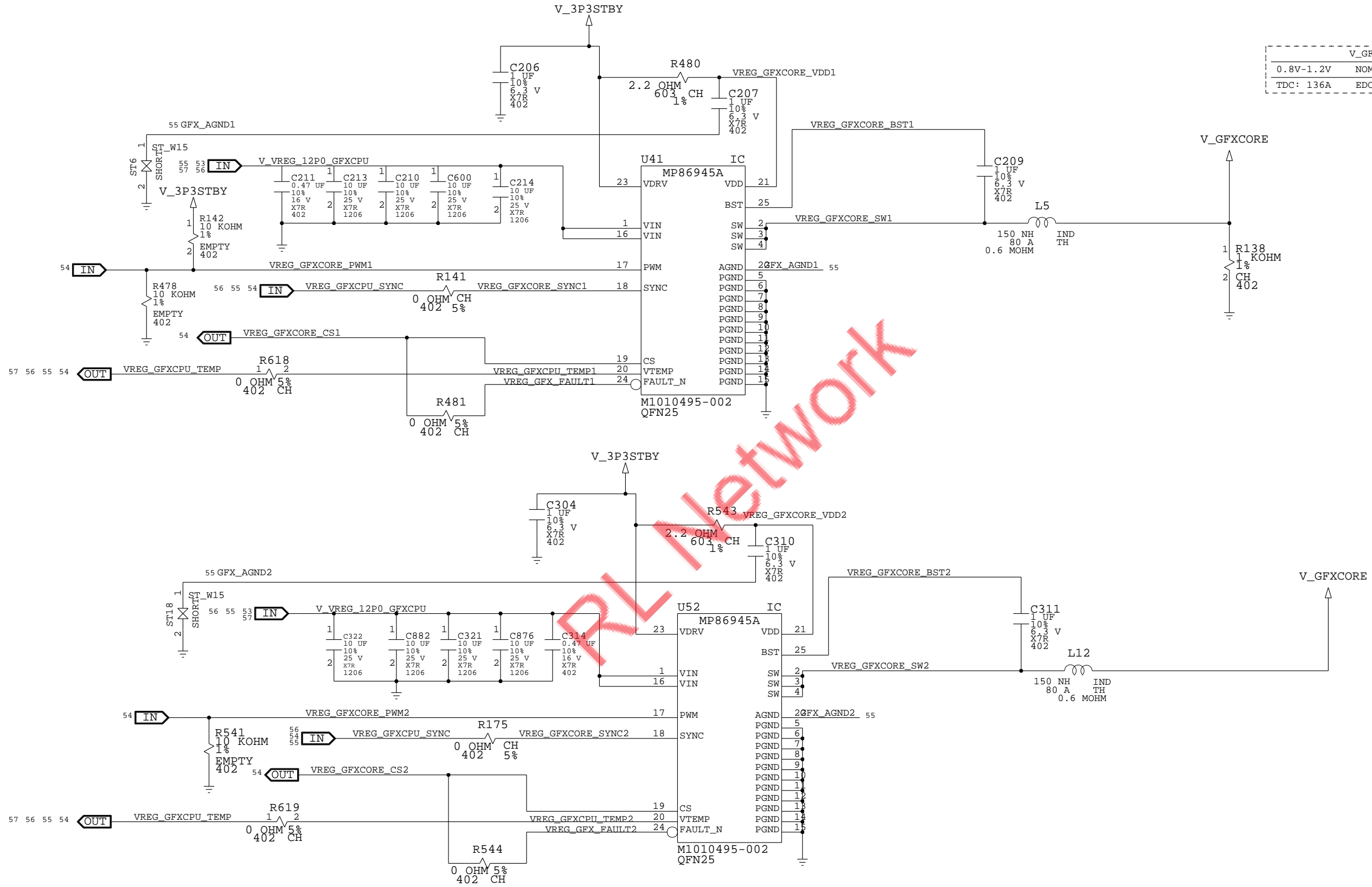
NOTE: X6S/X7R CAPACITORS USED NEAR SOC DUE TO HIGHER TEMPERATURES IN AREA

MP2853 RAIL ASSIGNMENTS	
RAIL 1:	V_GFXCORE (POWER GROUP B)
RAIL 2:	V_CPUCORE (POWER GROUP B)

MP2853 I2C ADDRESS			
	7-BIT BASE	R/W	I2C ADDR
WRITE	010 0000	0	0X20 0X40
READ	010 0000	1	0X20 0X41

8 7 6 5 4 3 2 1

VREGS: GFXCORE OUTPUT PHASE 1 & 2

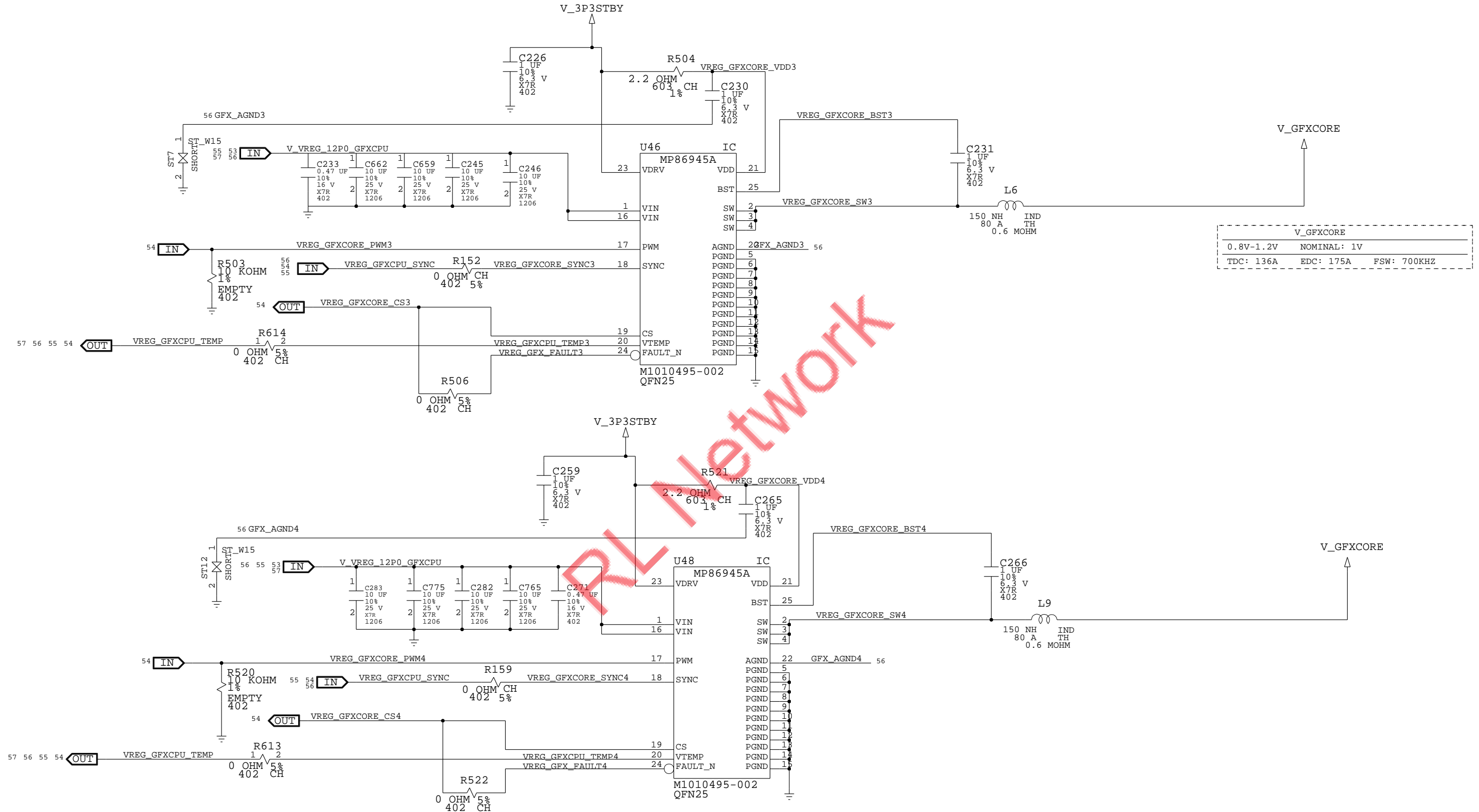


V_GFXCORE	
0.8V-1.2V	NOMINAL: 1V
TDC: 136A	EDC: 175A FSW: 700KHZ

NOTE: X6S/X7R CAPACITORS USED NEAR SOC DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Cactus	55/82	55/82	G-R	0.99L

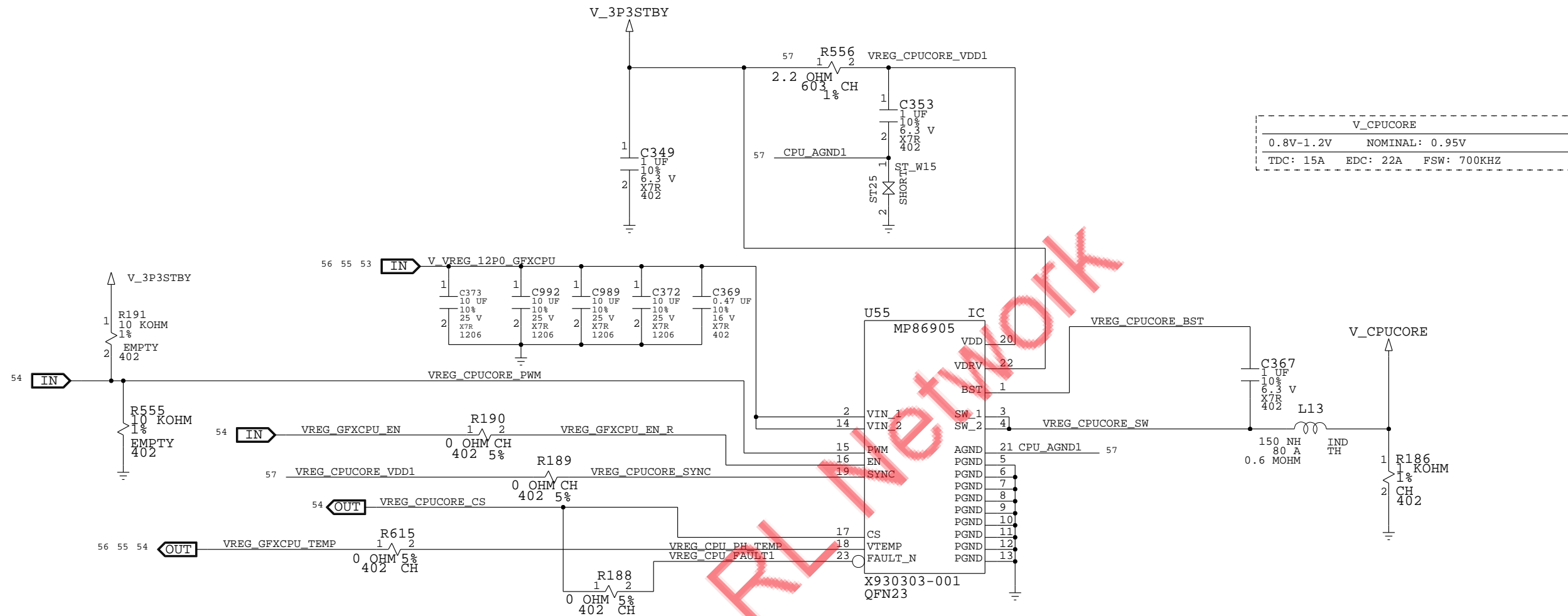
VREGS: GFXCORE OUTPUT PHASE 3 & 4



NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

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VREGS: CPUCORE OUTPUT PHASE

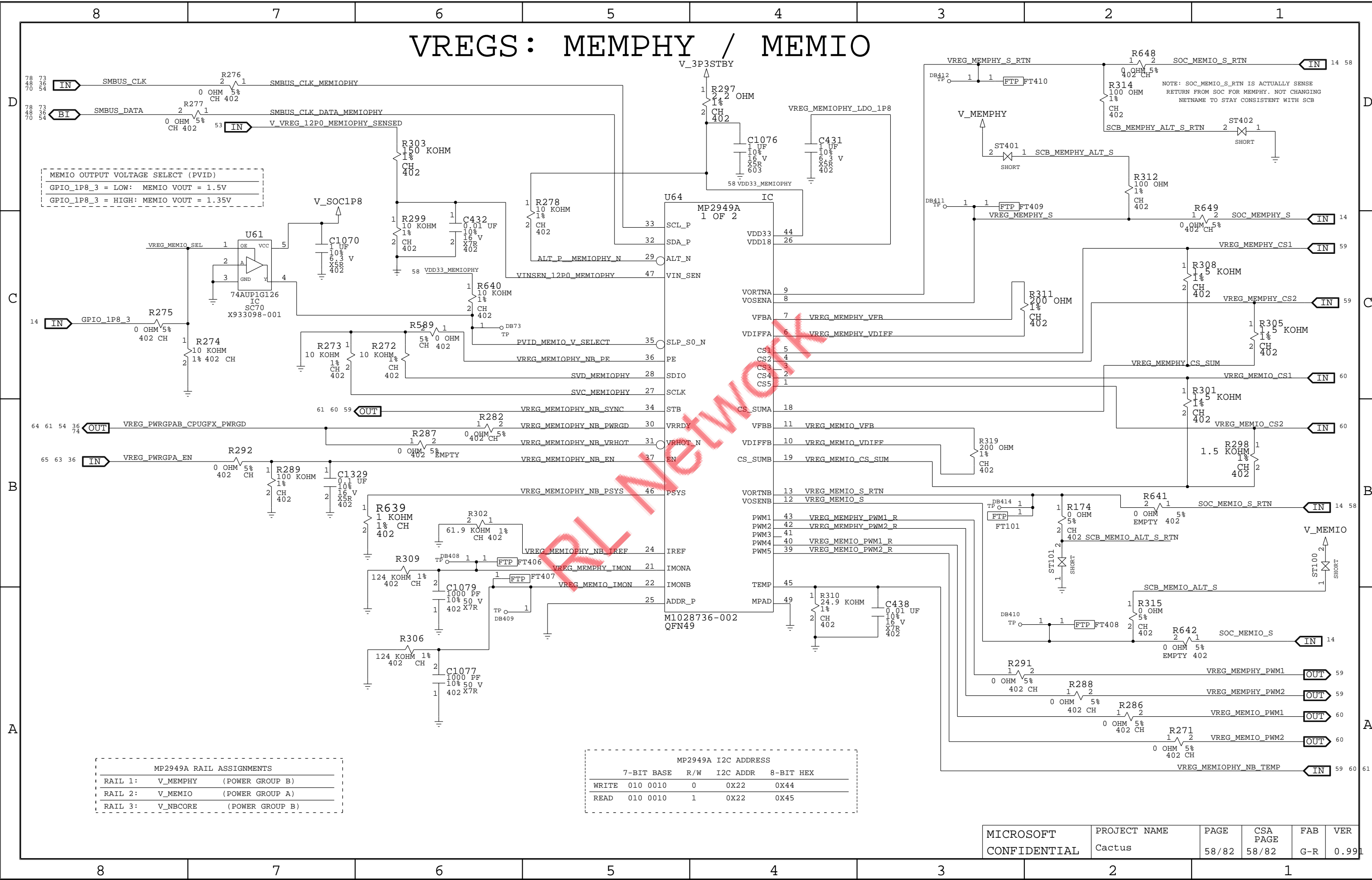


V_CPUCORE	
0.8V-1.2V	NOMINAL: 0.95V
TDC: 15A	EDC: 22A FSW: 700KHZ

NOTE: X6S/X7R CAPACITORS USED NEAR SOC
DUE TO HIGHER TEMPERATURES IN AREA

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Cactus	57/82	57/82	G-R	0.99L

VREGS: MEMPHY / MEMIO

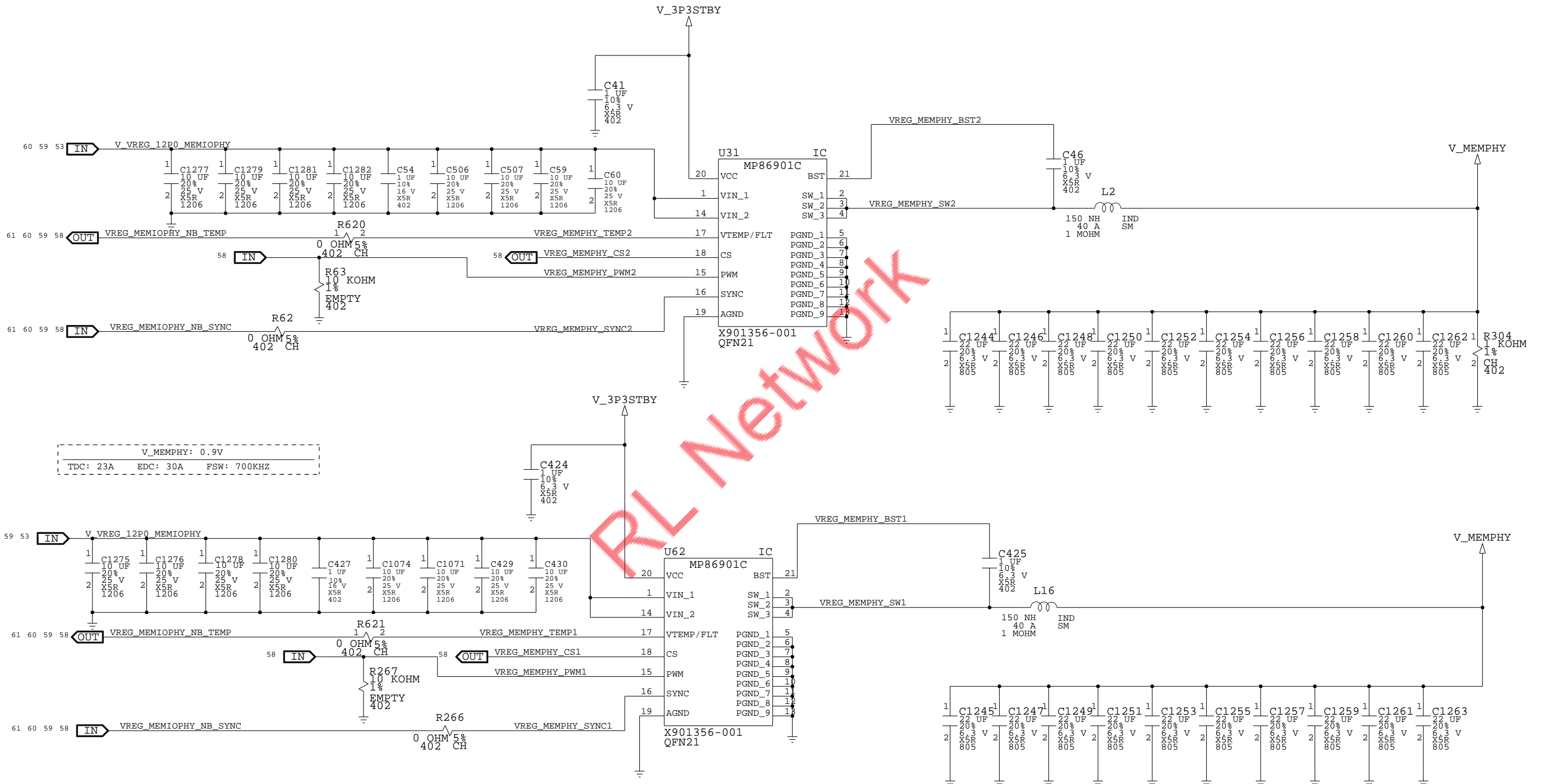


MEMIO OUTPUT VOLTAGE SELECT (PVID)
 GPIO_1P8_3 = LOW: MEMIO VOUT = 1.5V
 GPIO_1P8_3 = HIGH: MEMIO VOUT = 1.35V

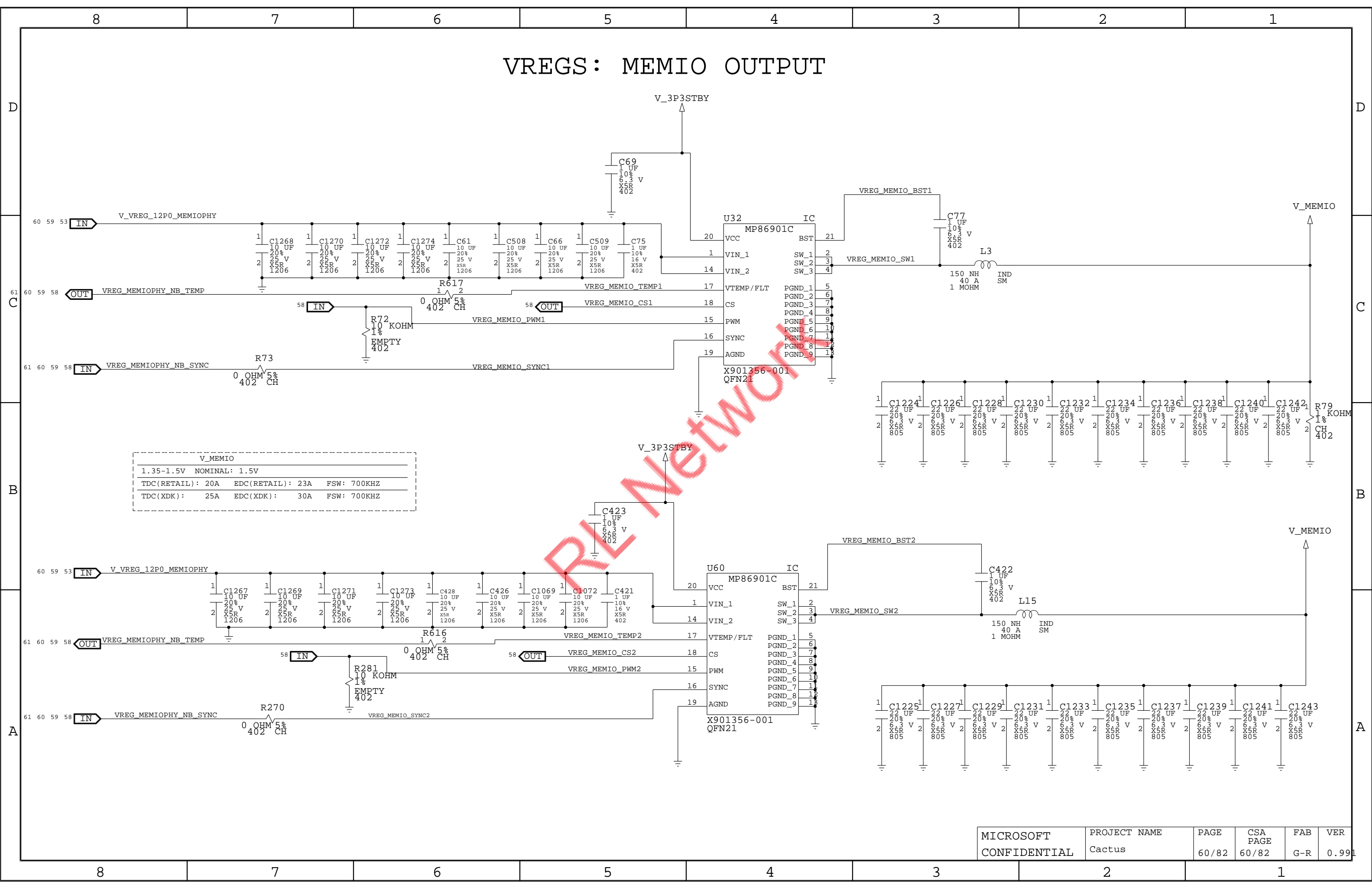
MP2949A RAIL ASSIGNMENTS	
RAIL 1:	V_MEMPHY (POWER GROUP B)
RAIL 2:	V_MEMIO (POWER GROUP A)
RAIL 3:	V_NBCORE (POWER GROUP B)

MP2949A I2C ADDRESS				
	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0010	0	0X22	0X44
READ	010 0010	1	0X22	0X45

VREGS: MEMPHY OUTPUT

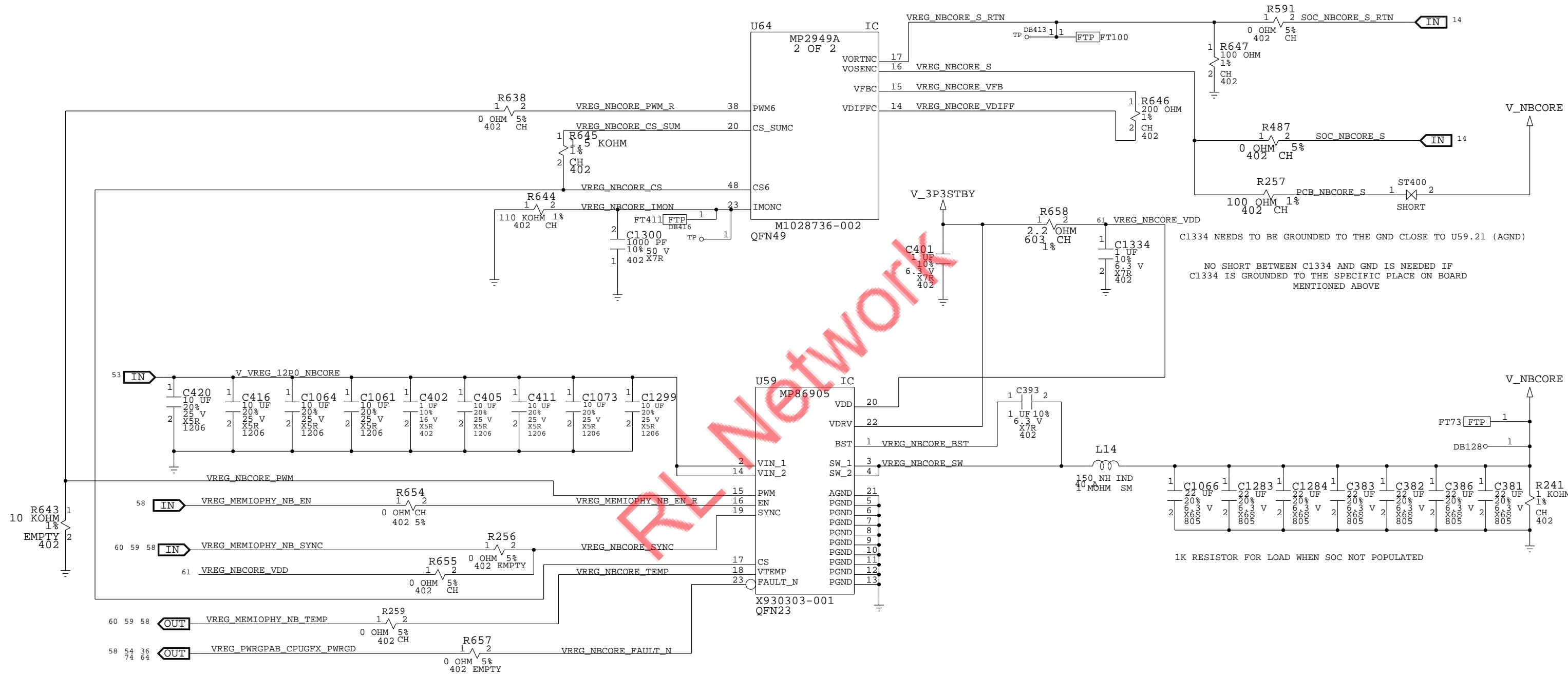


VREGS: MEMIO OUTPUT



V_MEMIO					
1.35-1.5V	NOMINAL:	1.5V			
TDC(RETAIL): 20A	EDC(RETAIL): 23A	FSW: 700KHZ			
TDC(XDK): 25A	EDC(XDK): 30A	FSW: 700KHZ			

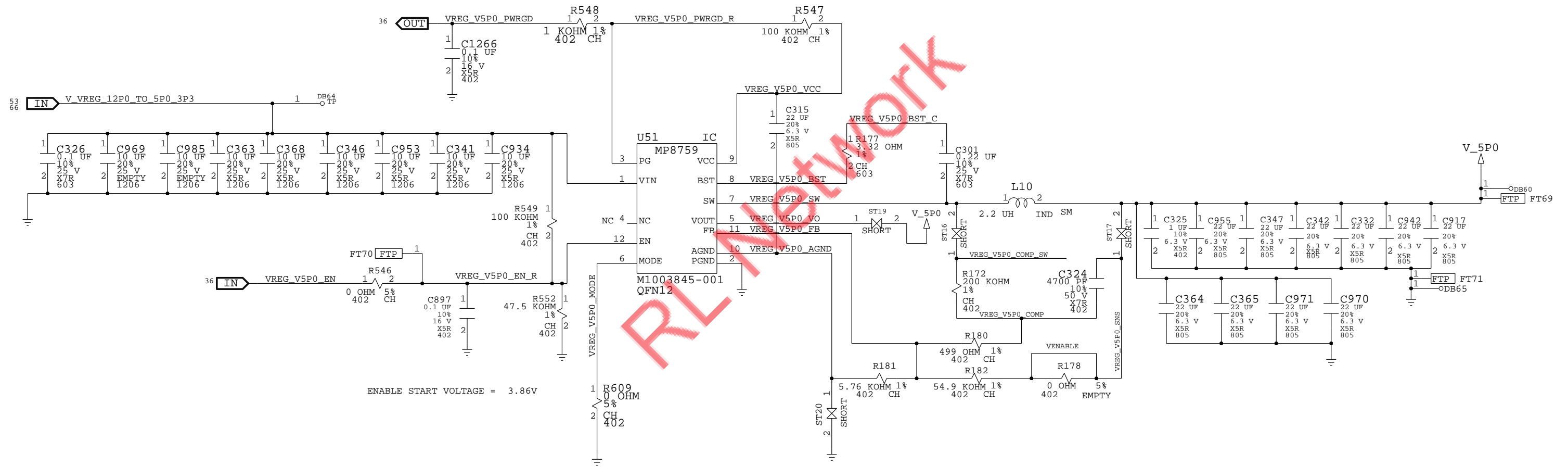
VREGS : NBCORE



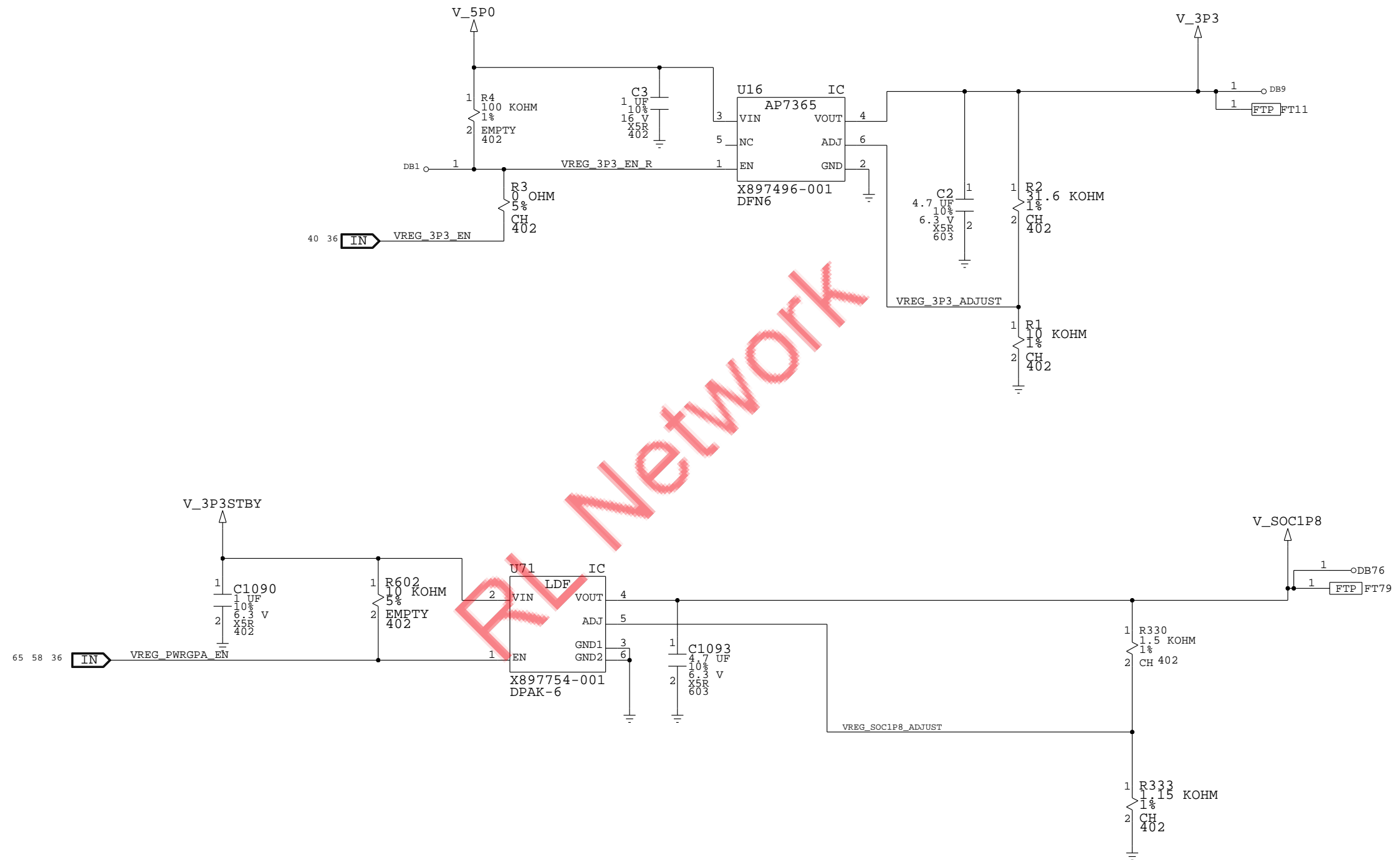
V_NBCORE	
0.8V-1.2V	NOMINAL: 0.95V
TDC: 16A	EDC: 25A FSW: 700KHZ

VREGS: V5P0

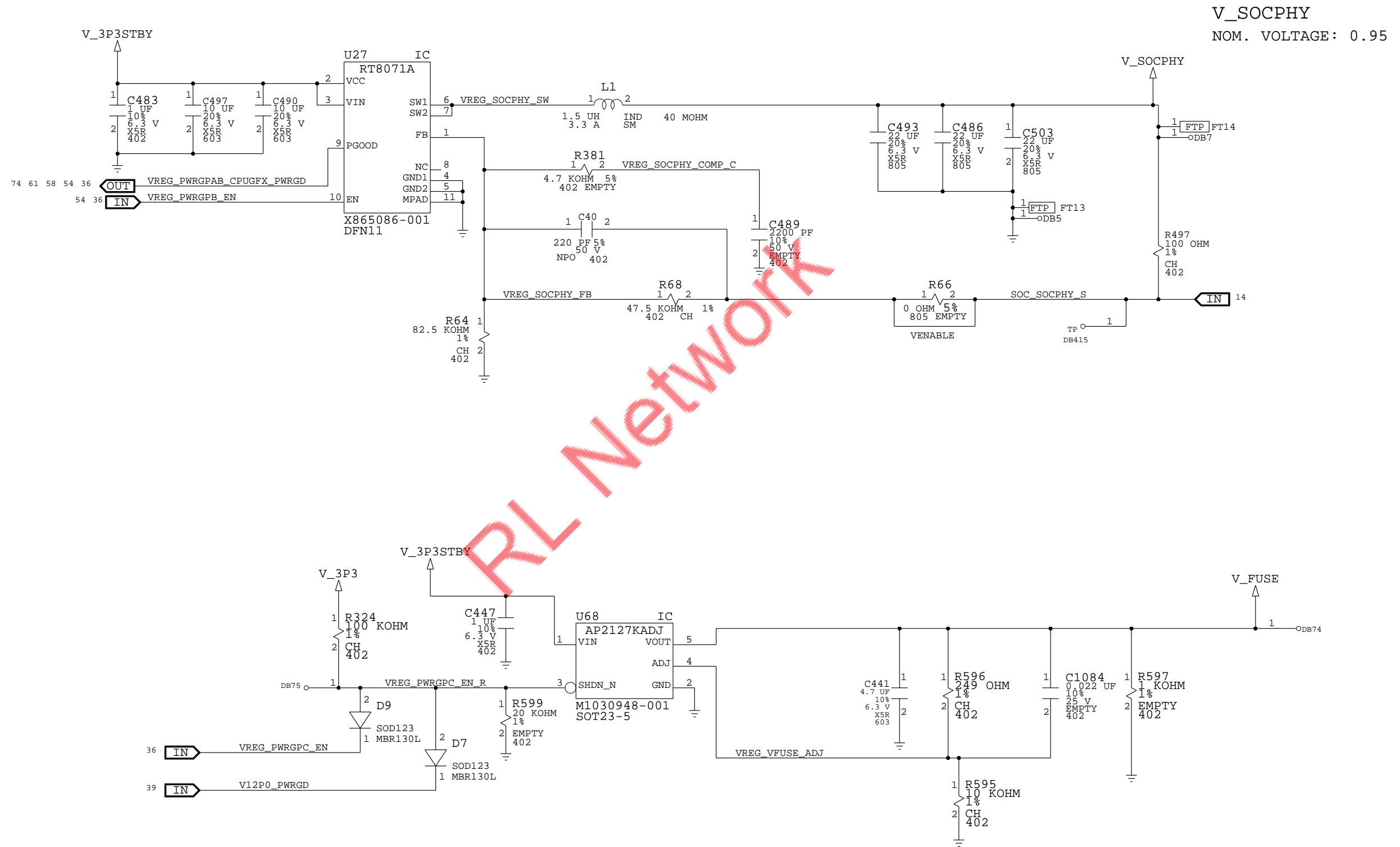
V_5P0
 NOM. VOLTAGE: 5.1



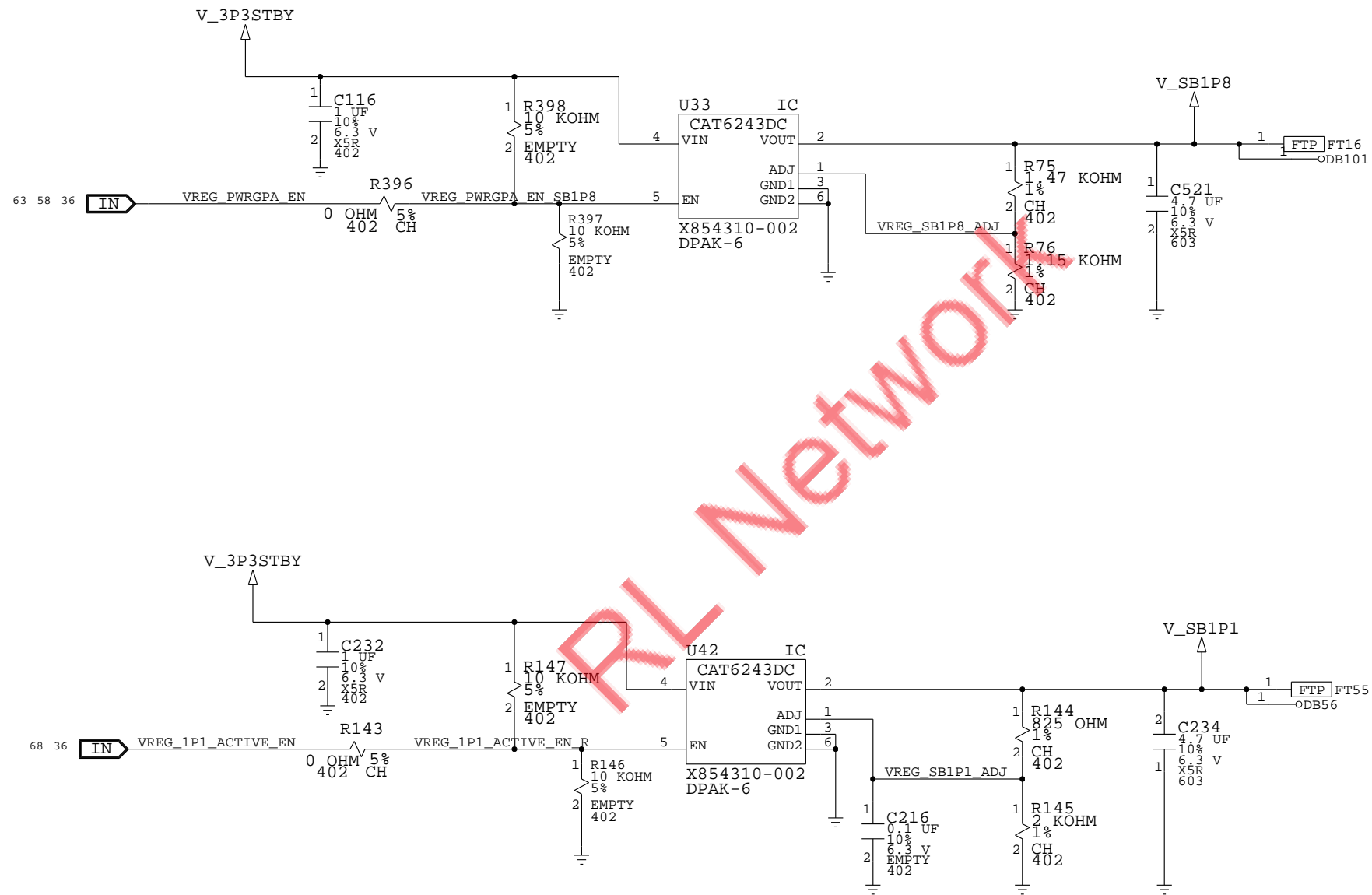
VREGS: V3P3, VSOC1P8



VREGS: VSOCPHY/VFUSE

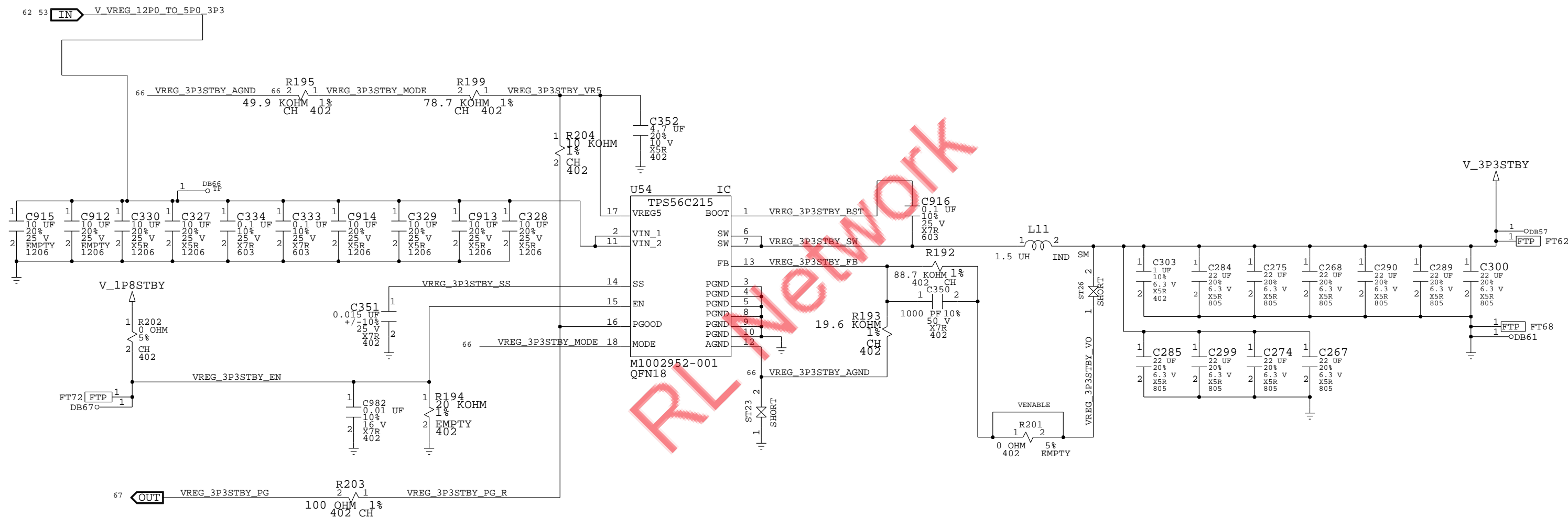


VREGS: V_SB1P8, V_SB1P1

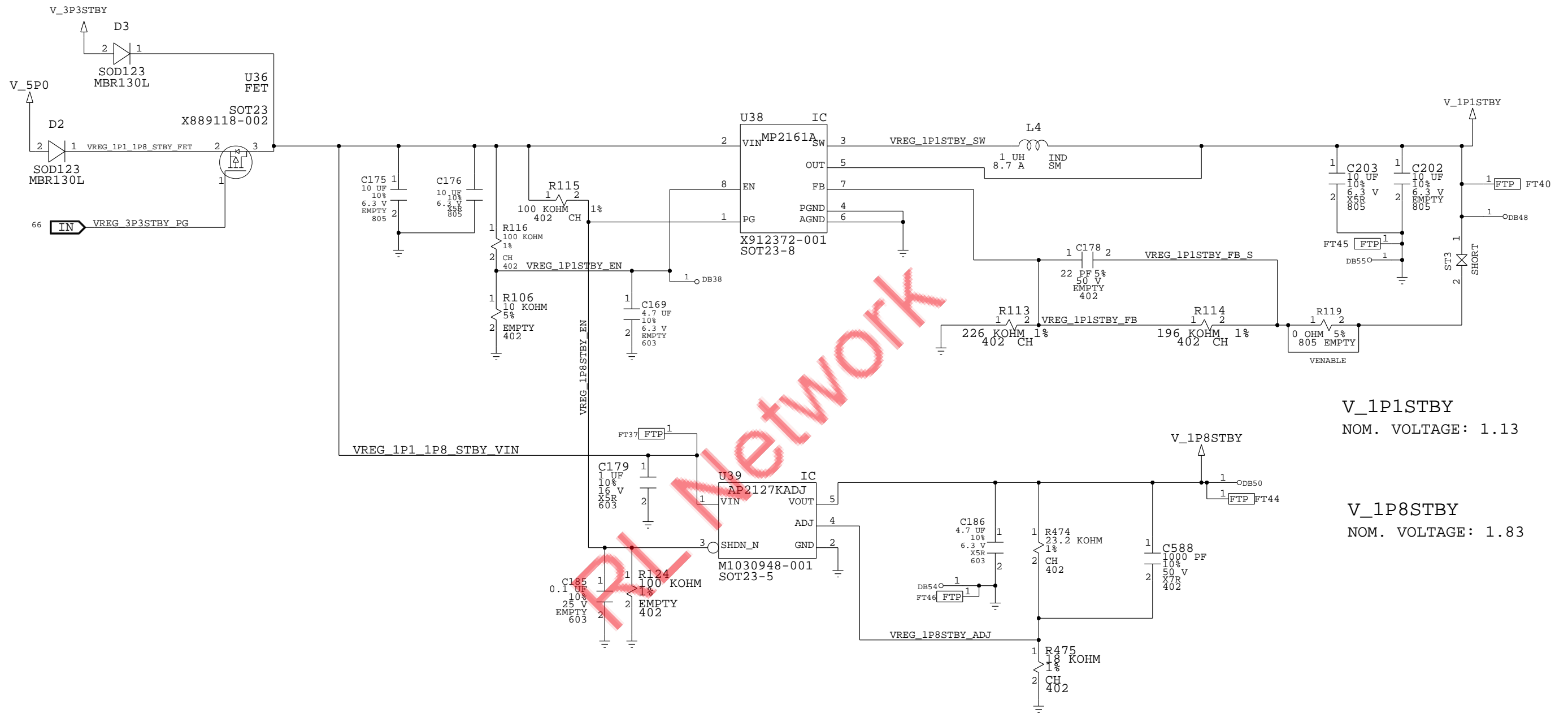


VREGS: V3P3 STANDBY

V_3P3STBY
 NOM. VOLTAGE: 3.32



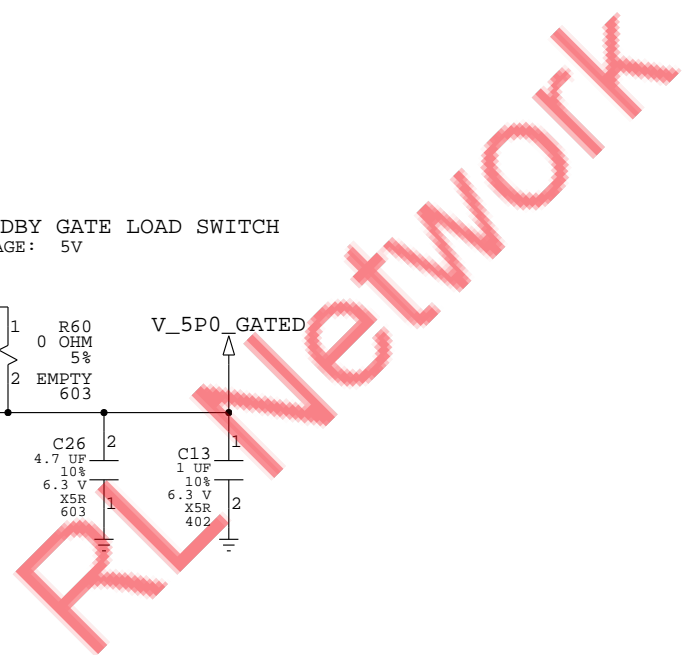
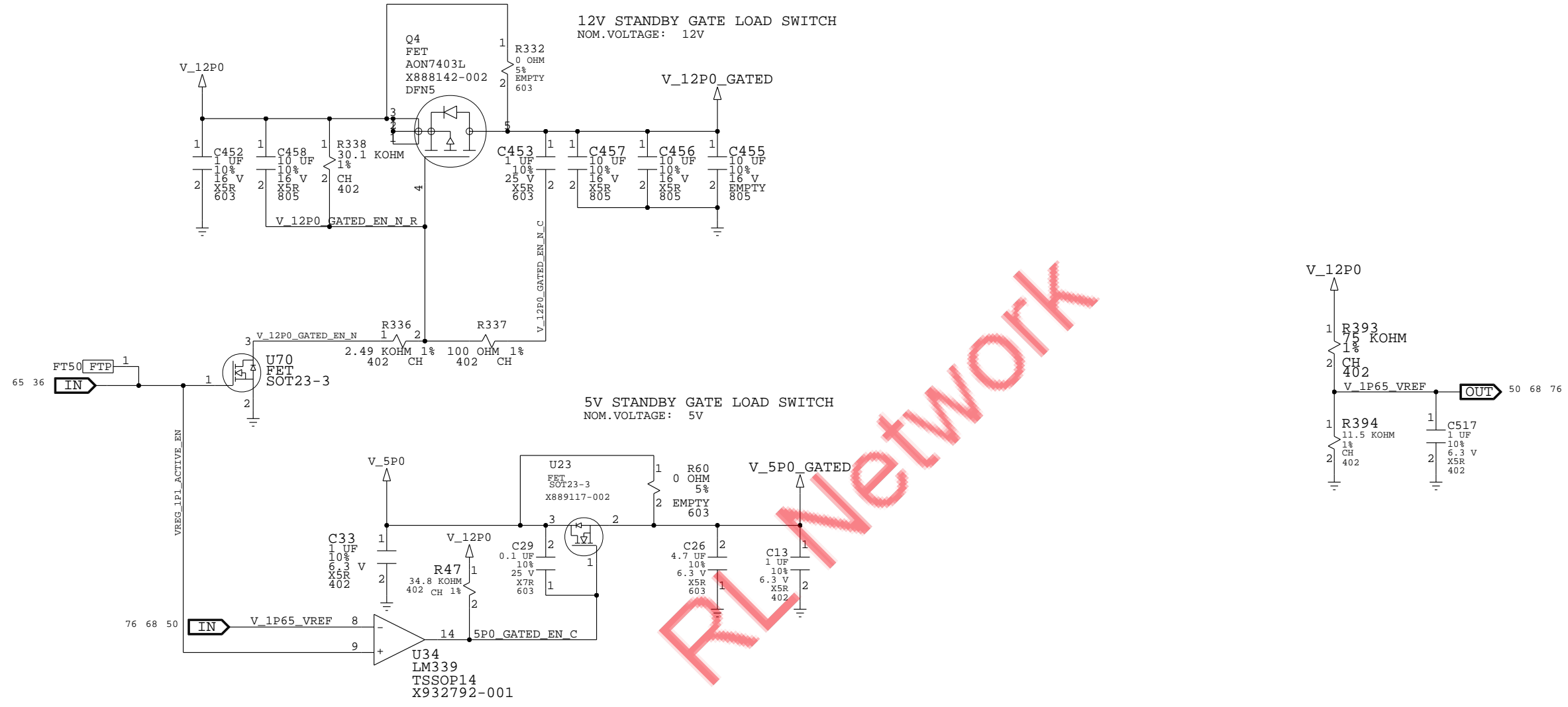
VREGS: V1P1 STANDBY, V1P8 STANDBY



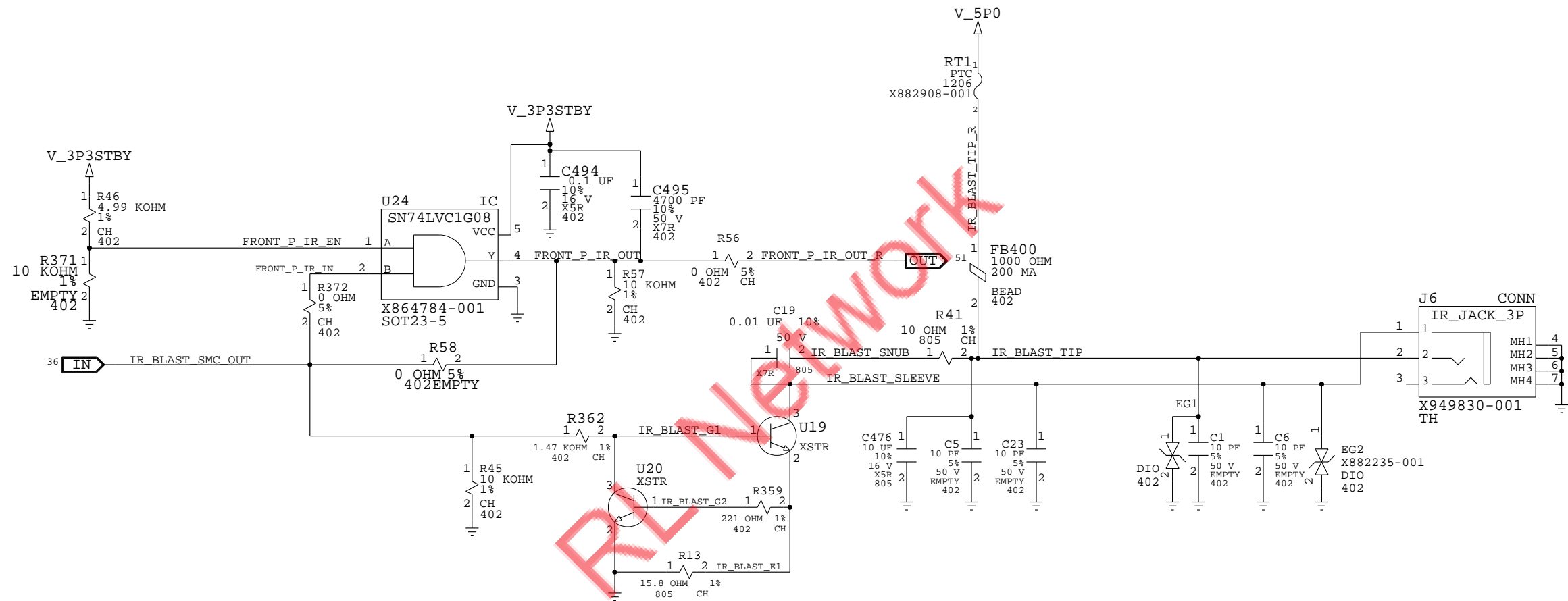
V_1P1STBY
NOM. VOLTAGE: 1.13

V_1P8STBY
NOM. VOLTAGE: 1.83

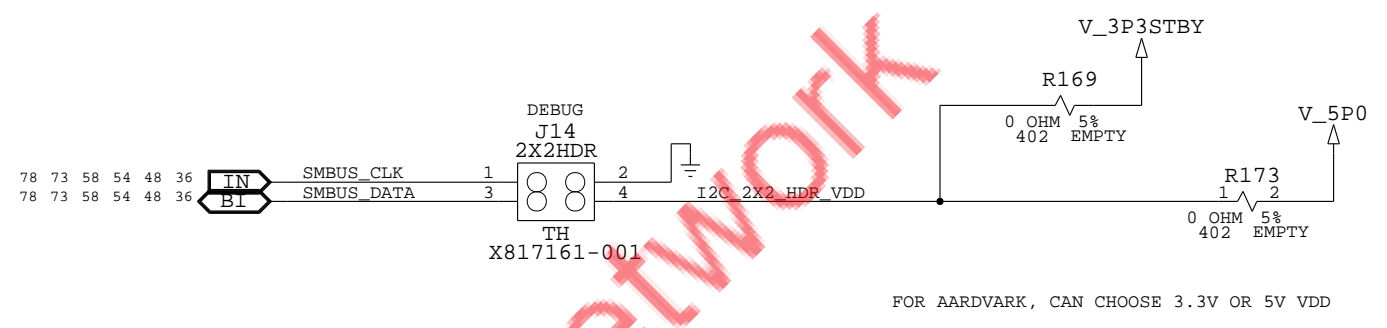
STANDBY GATES



IR BLASTER



I2C



RL Network

MARGIN: SOCPHY ,SOC1P8

D
C
B
A

D
C
B
A

BLANK

RL Network

8 7 6 5 4 3 2 1

MONITOR: VSOC1P8,VSOCPHY,V12P0

D

D

C

C

B

B

A

A

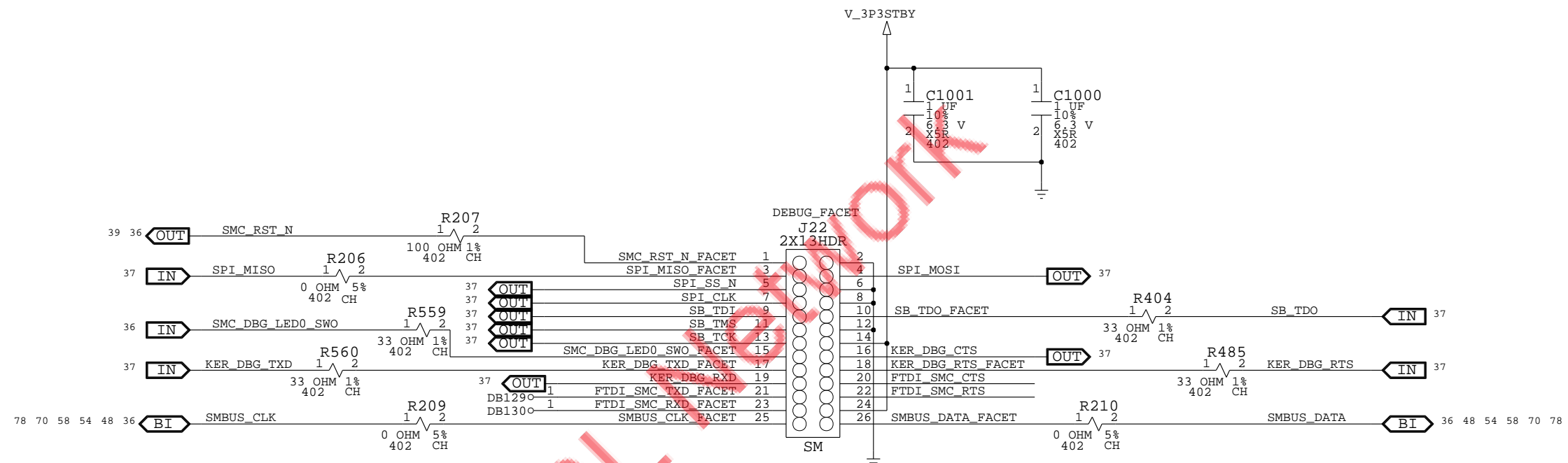
BLANK

RL Network

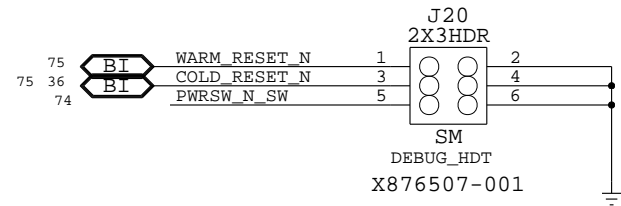
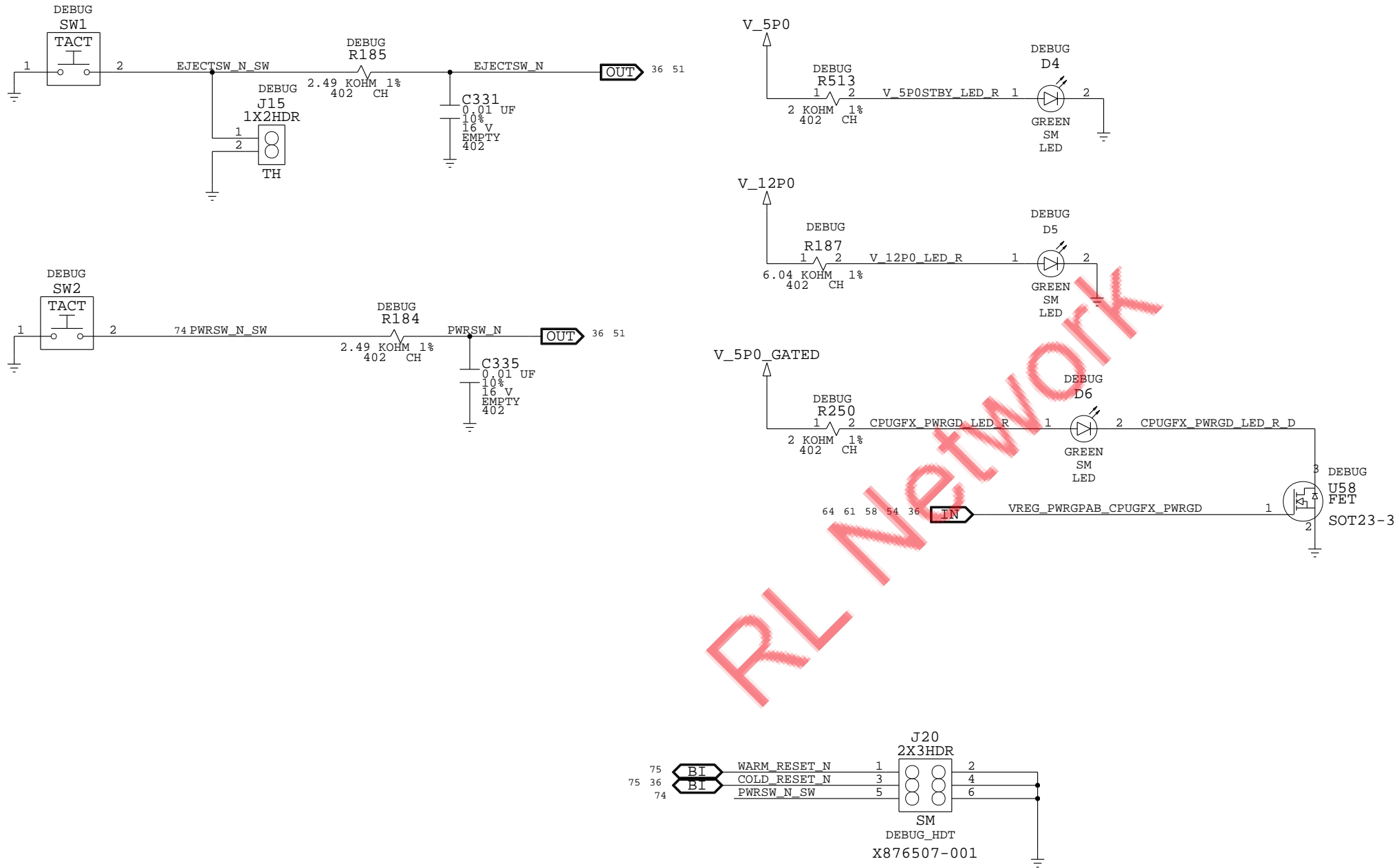
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	VER
CONFIDENTIAL	Cactus	72/82	72/82	G-R	0.991

8 7 6 5 4 3 2 1

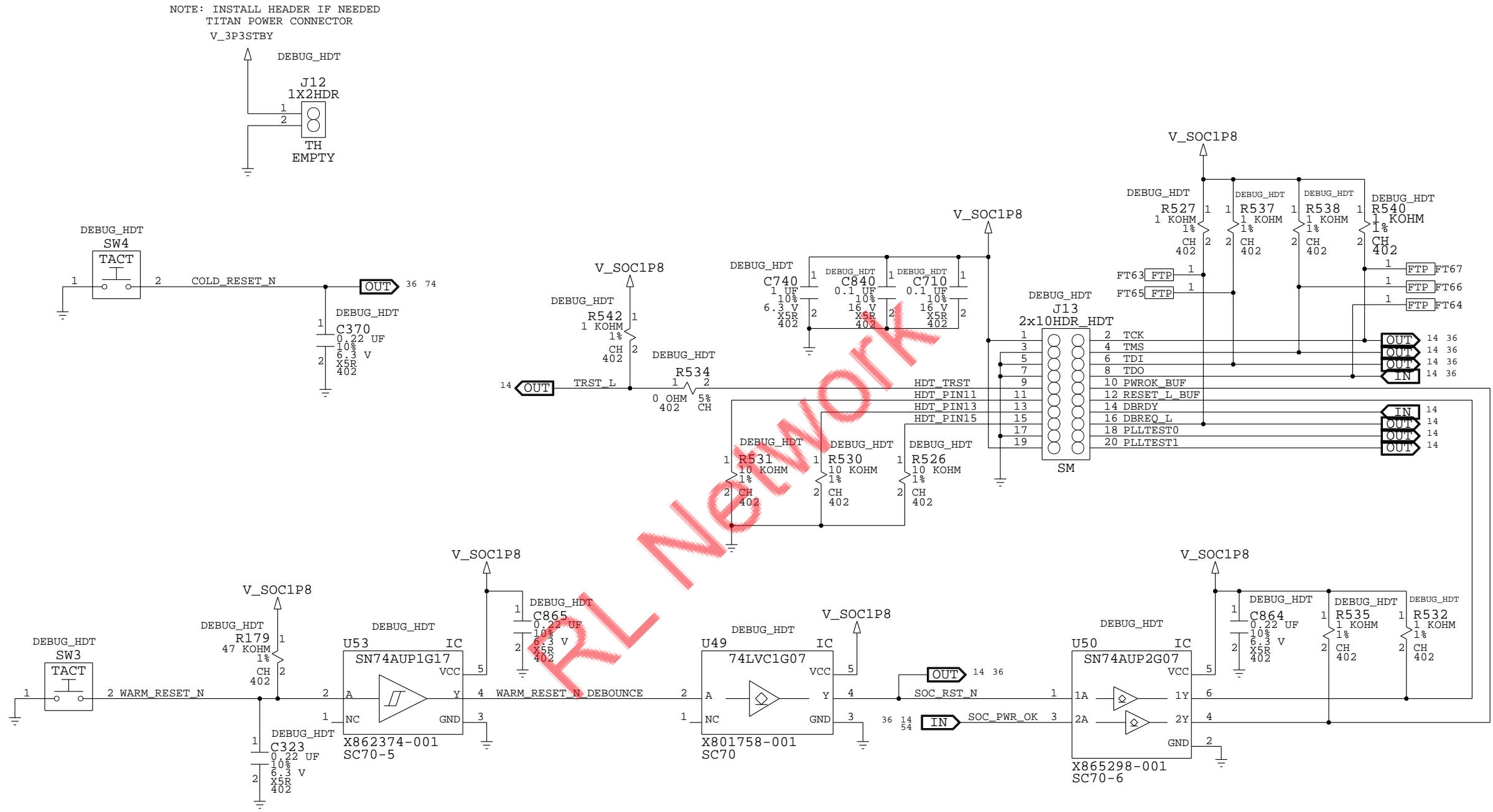
CONN: FACET BOARD



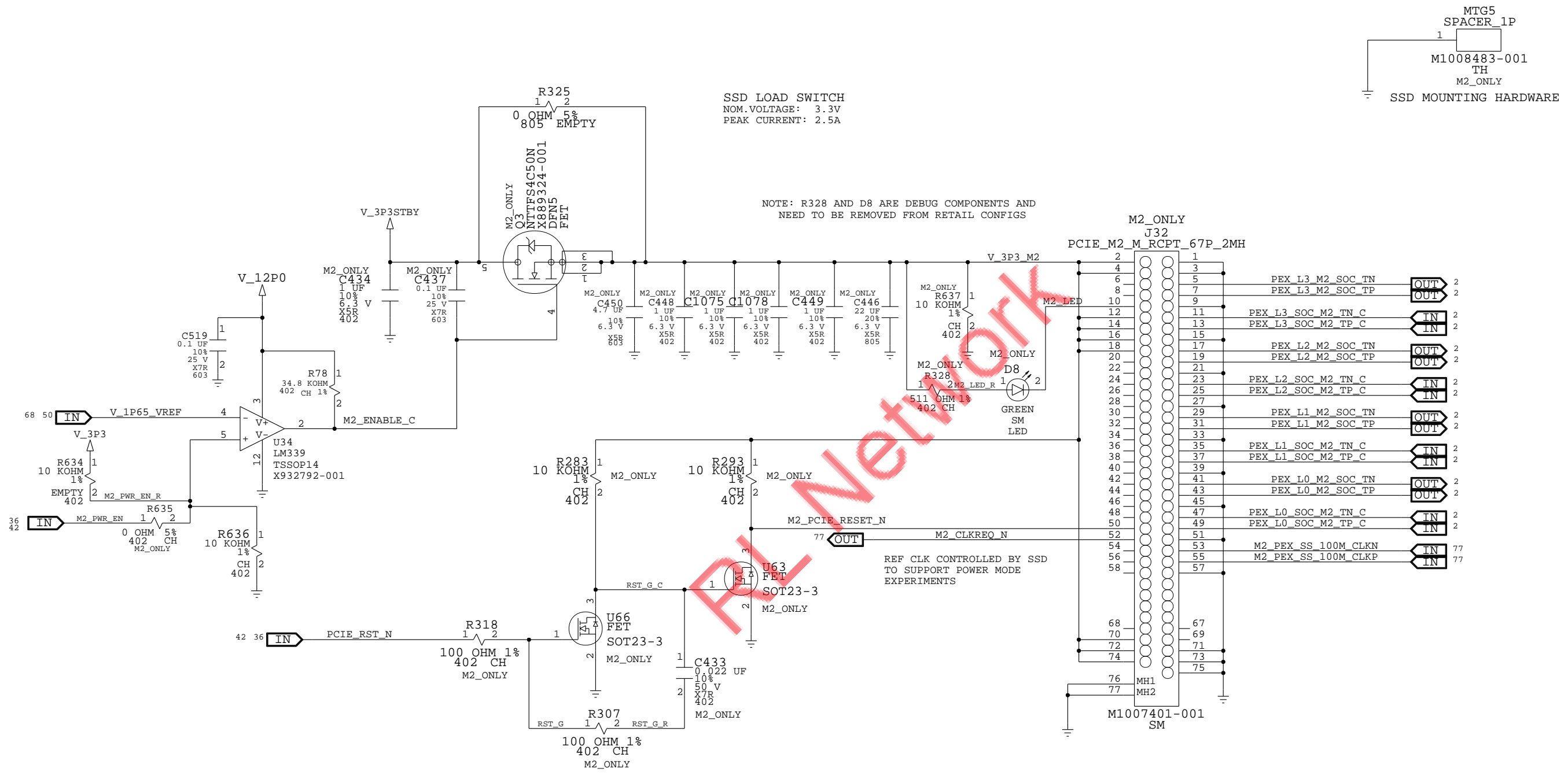
CONN: SWITCHES



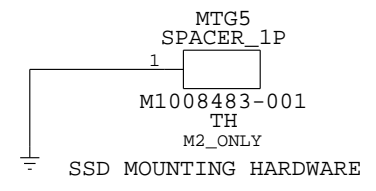
CONN: HDT



CONN: M.2



NOTE: R328 AND D8 ARE DEBUG COMPONENTS AND
 NEED TO BE REMOVED FROM RETAIL CONFIGS

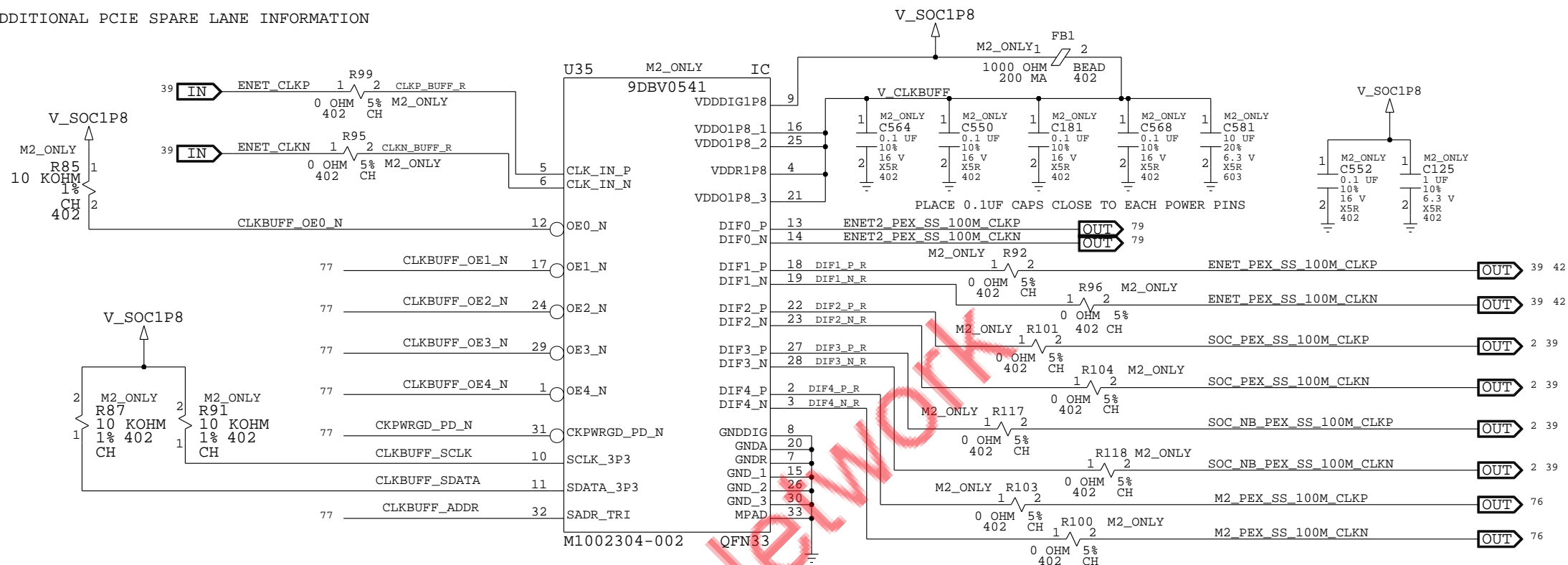


THE SSD HAS AN INTERNAL PULL-UP ON ITS PCIE RESET INPUT.
 ISOLATION OF SIGNAL PCIE_RST_N IS NEEDED TO ISOLATE
 SOUTHBRIDGE OUTPUT FROM SSD PULLUP

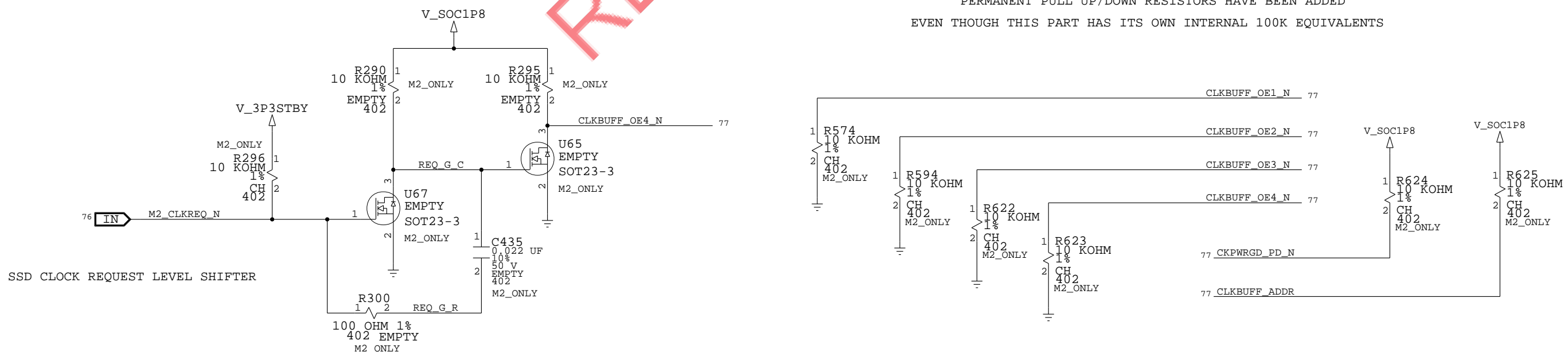
CLOCK BUFFER

NOTES:

- 1. TO ENABLE ENET2 CLOCK ON J28 HEADER, UNSTUFF R85. U35 HAS INTERNAL PULL DOWN.
- 2. SEE PAGES 2 AND 79 FOR ADDITIONAL PCIE SPARE LANE INFORMATION

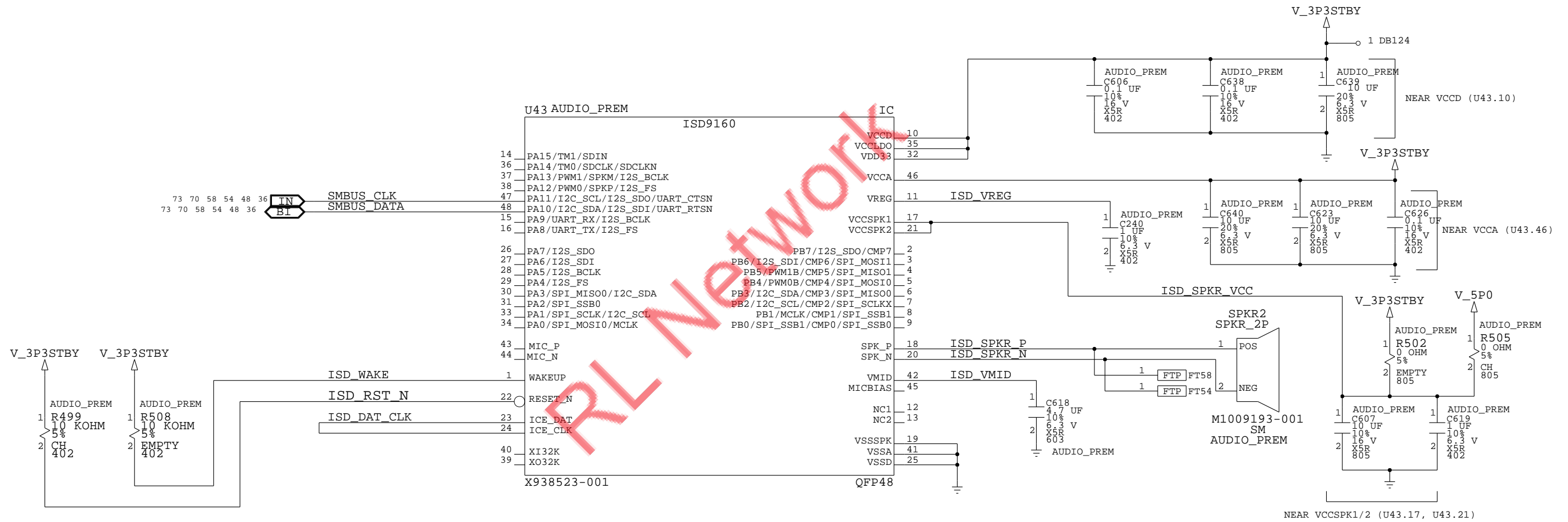


TO ADDRESS LONG TERM RELIABILITY CONCERNS
 PERMANENT PULL UP/DOWN RESISTORS HAVE BEEN ADDED
 EVEN THOUGH THIS PART HAS ITS OWN INTERNAL 100K EQUIVALENTS



PREMIUM SPEAKER (SE/LE)

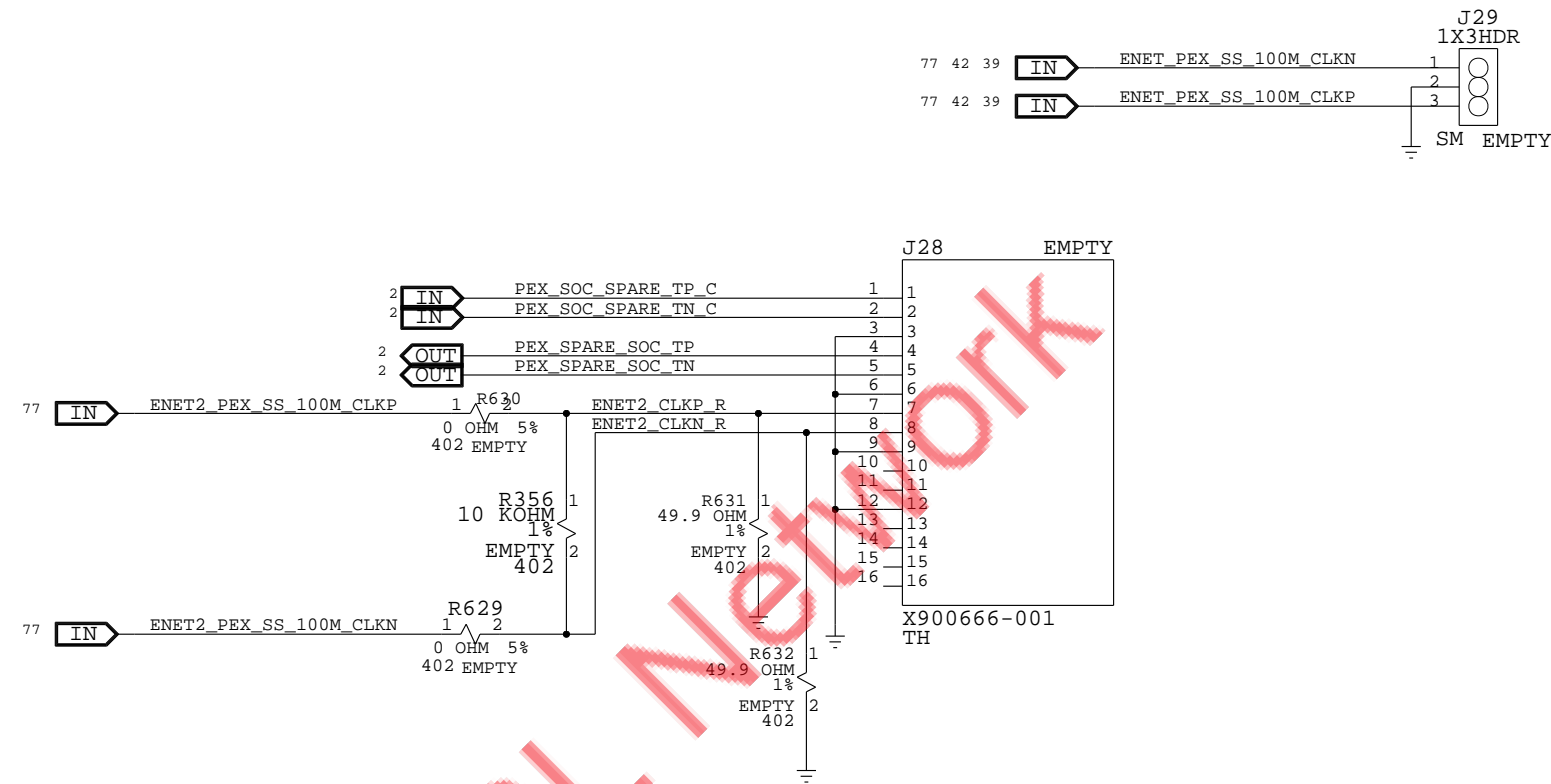
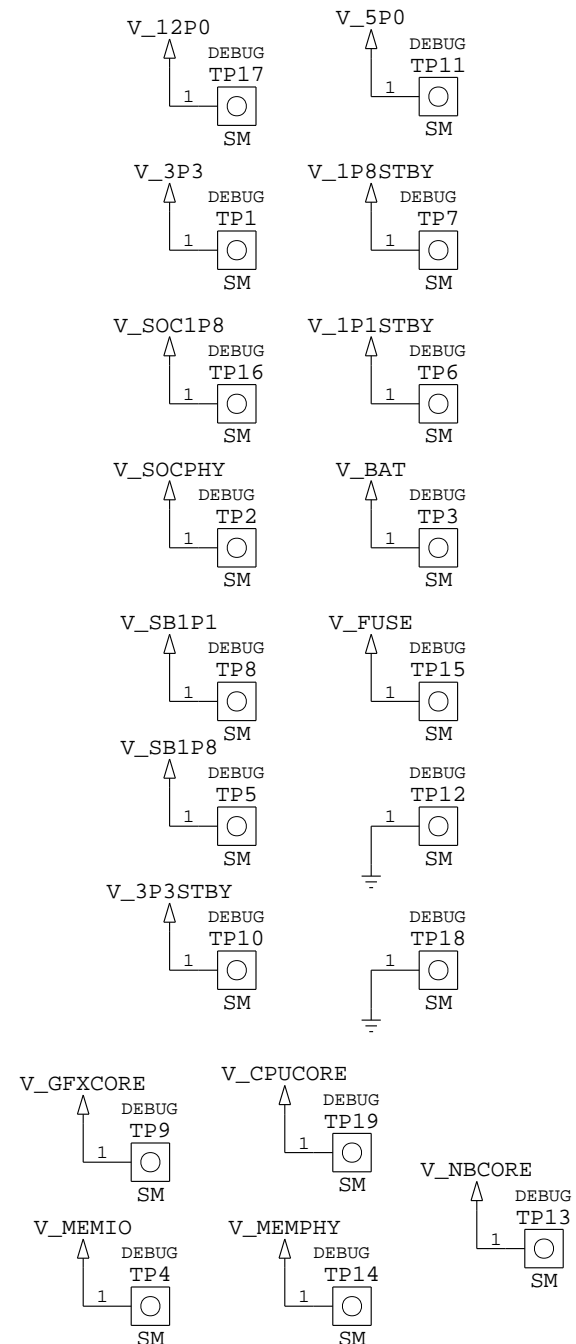
PREMIUM/SE/LE SKU ONLY



ISD9160FIMS05 - REMOVED CAP TOUCH FUNCTIONALITY

DEBUG: VR HEADERS, TEST POINTS, CONNECTORS

PCIE CONNECTORS



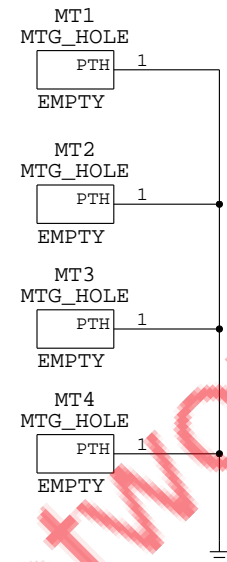
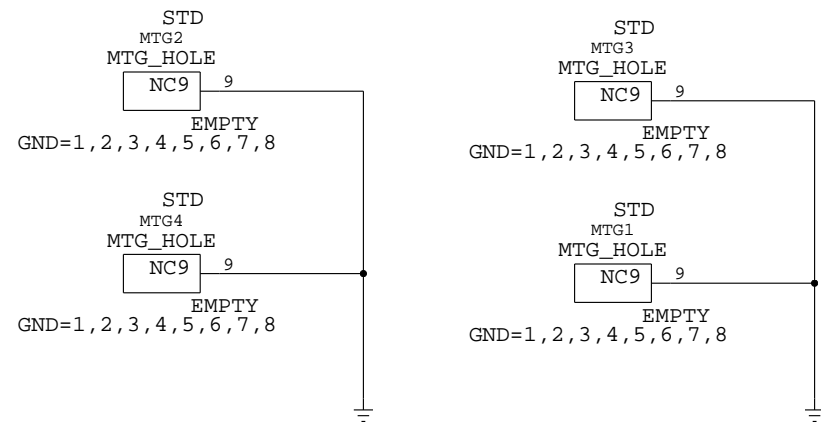
NOTES: TO ENABLE 100 MHZ REF CLOCK ON HEADER J28:

1. WHEN CLOCK BUFFER U35 IS INSTALLED: POPULATE R629 AND R630.
2. WITHOUT CLOCK BUFFER INSTALLED:
 - A. POPULATE R631 AND R632.
 - B. WIRE JUMPER ETHERNET 100 MHZ CLOCK FROM HEADER J29.1 AND J29.3 TO J28.8 AND J28.7 RESPECTIVELY.
3. SEE PAGES 2 AND 77 FOR ADDITIONAL PCIE SPARE LANE INFORMATION.

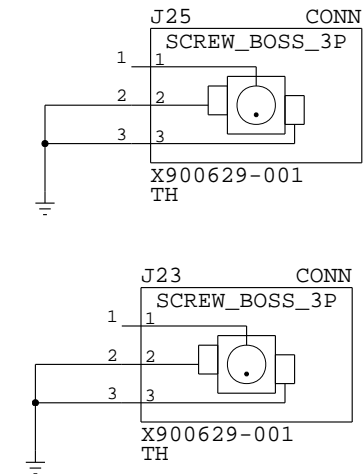
NOTE: THESE TEST POINTS ARE NOT TO BE USED FOR VOLTAGE REGULATOR QUALIFICATION TEST POINTS

LABELS AND MOUNTING

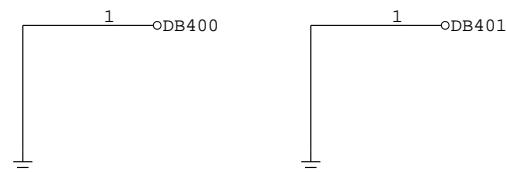
HEAT SINK MOUNTING HOLES



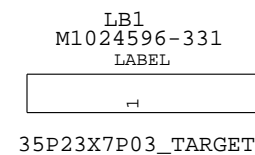
SCREW BOSS



GND PADS FOR HEATSINK ALIGNMENT PINS

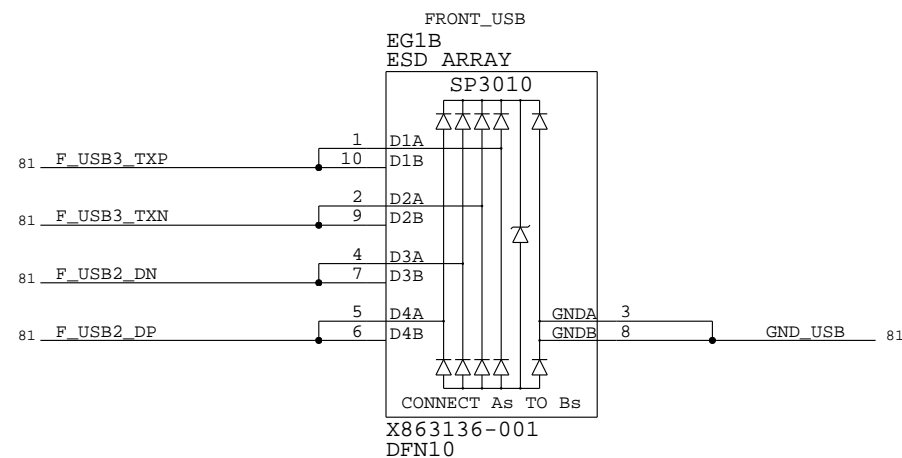
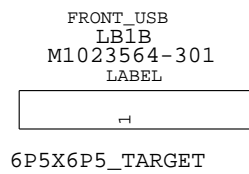
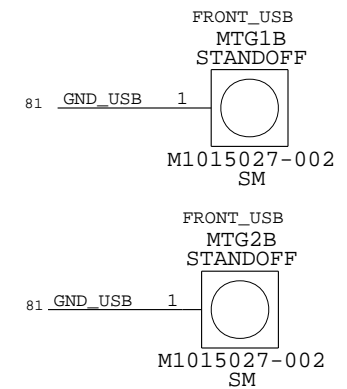
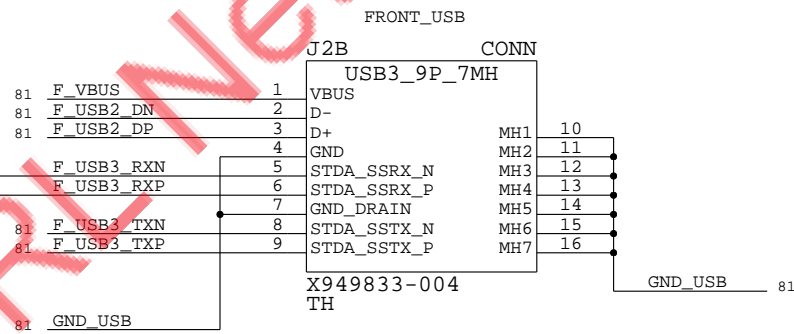
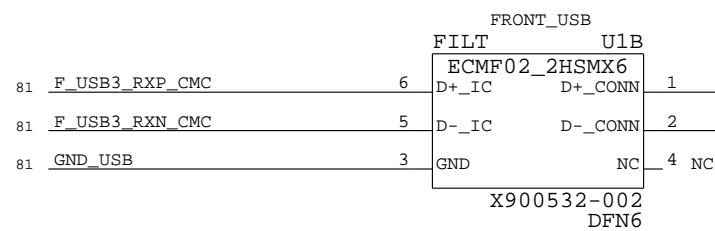
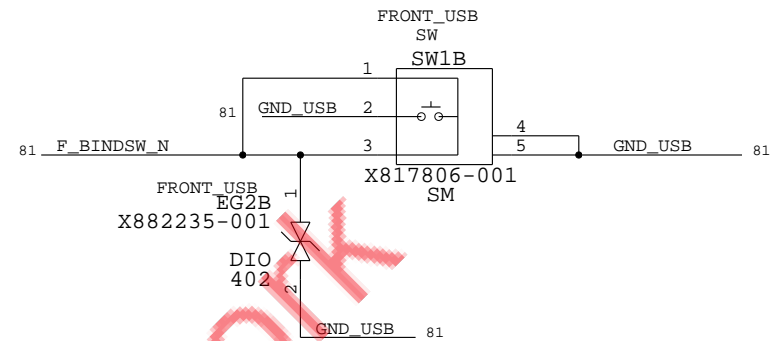
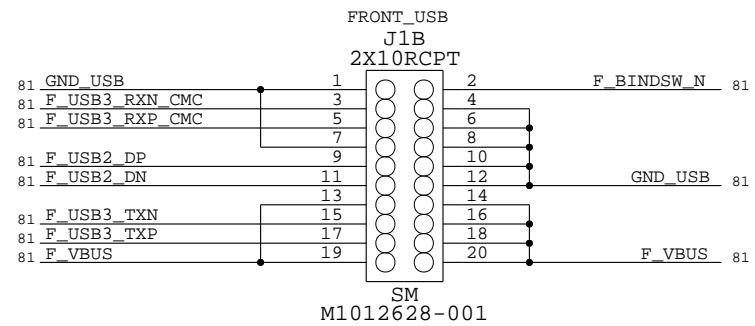


INTELLIGENT SERIAL NUMBER TARGET



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
NA	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,GT	PCB_GI
M1037358-002	FR4	PCB1	PCB,CACTUS,FAB G RETAIL,8 LAYERS,OSP	PCB_OSP

FRONT PANEL USB - NESTED PCB



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
M1033394-001	FR4	PCB1B	PCB,CACTUS,FAB E RETAIL,FRONT USB,8 LAYERS,GH	FRONT_USB

BOM DEFINITIONS

BOM	DEFINTION
AUDIO	INCLUDES COMPONENTS FOR THE STANDARD AUDIO SOLUTION
AUDIO_PREM	INCLUDES COMPONENTS FOR THE PREMIUM SE/LE SPEAKER SOLUTION
COMMON	ALL COMPONENTS WITH NO BOM PROPERTY
DEBUG	COMPONENTS REQUIRED FOR BRING UP & DEBUG
DEBUG_HDT	HDT-RELATED DEBUG COMPONENTS
DEBUG_SHUNT	COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL
EMMC_BASE	DUMMY PLACE HOLDER FOR EMMC DEVICE & RESISTORS. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
EMMC_HYNIX_16NM	HYNIX EMMC DEVICE
EMMC_SAMSUNG_14NM	SAMSUNG EMMC DEVICE
EMMC_TOSHIBA_15NM	TOSHIBA EMMC DEVICE
GDDR5_BASE	DUMMY PLACE HOLDER FOR GDDR5. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
GDDR5_HYNIX	HYNIX GDDR5 MEMORY
GDDR5_SAMSUNG	SAMSUNG GDDR5 MEMORY
FRONT_USB	COMPONENTS ON THE FRONT PANEL USB
KIC_BASE	DUMMY PLACE HOLDER FOR KIC. NEVER USE THIS IN THE RECIPE FILE. USE ONE OF THESE INSTEAD: KIC_DEV OR KIC_RETAIL
KIC_DEV	DEBUG VERSION OF KRAKEN
KIC_RETAIL	RETAIL VERSION OF KRAKEN
M2_ONLY	POPULATE TO SUPPORT AN M.2 INTERFACE
NO_M2	POPULATE WHEN THERE IS NO M2. INTERFACE
PCB_GI	FAB TYPE: GOLD
PCB_OSP	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK
PCB_OSP_BLACK	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE BLACK SOLDERMASK
RTC_RETAIL	RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS
RTC_XDK	RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS
SOC_BASE	DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE. SELECT ONE OF THESE INSTEAD: EMMC_HYNIX_16NM, EMMC TOSHIBA_15NM, EMMC SAMSUNG_14NM
SOC_EMPTY	DOES NOT STUFF ANUBIS
SOC_INCLUDE	STUFFS ANUBIS
VR_FIXED	SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_MM
VR_MM	ALLOWS MOST VRS TO BE MARGINED FOR M&M BOARDS. EXCLUDES V_MEMIO. MUST BE USED IN CONJUNCTION WITH NOT VR_FIXED

