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Technical Guide

3DO Interactive Multiplayer

FZ-1

Panasonic®

CONTENTS

1. System Overview

The Real 3DO IM (Interactive Multiplayer) is based on the 3DO Interactive Multiplayer™ (IM) specification.

The REAL is a high performance video and audio entertainment and education system capable of realistic interactive video and CD quality audio presentations. The REAL represents the state of the art in a high performance low cost interactive video and audio system.

In addition, the REAL will play standard audio CDs at full 16-bit precision and bandwidth like audio stereo CD player. And also display and play Kodak Photo CD disc and Portfolio Photo CD disc (Photo with CD sound).

The REAL will produce NTSC (composite video), S-video and RF modulated composite video outputs to almost broadcast quality.

The REAL has the following high performance architecture :

- Two graphics animation processor (Cell Engine) that deliver 50 times the performance of typical personal computers and video game systems.
- Millions (2^{24}=16,777,216) of simultaneous colors for realistic picture quality.
- CD quality sound (16 bits stereo D/A converter with x8 over-sampling filter) with digital signal processing.
- 32-bit RISC processor for interactive processing and it works with 24 DMA (Direct Memory Access logic) to support high performance multitasking and real-time operating system.
- A CD-ROM drive supplies faster data access (double speed 300K Bytes/sec), transfer (4M Bytes/sec) and more than 500M Bytes data and program.
- Full Motion Video CD support with optional FMV cartridge (MPEG board).

1-1. Specifications

• Main Logic Board

Processor	CPU	ARM60 (32 bits RISC processor) Clock : 12.5 MHz
	DSP	Original 16 bits Digital Signal Processor (including in CLIO chip)
Memory	DRAM/VRAM	3 MB : Access time = 80 ns at fast page mode Serial access time = 20 ns 2MB = DRAM, main RAM 1MB = VRAM, dual port RAM Selectable as Main RAM or Frame Buffer
	ROM	1MB : Access time = 200 ns
	SRAM	32 KB : Battery backup memory
System IC	MADAM	3DO IM system control IC (Address Engine) : Mainly includes DMA, CPU control logic, BUS sharing logic and Cell engine System clock = 25.000 MHz (=1/2 of Crystal)
	CLIO	3DO IM system control IC (Data Engine) : Mainly includes pixel decoding logic, CLUT and video interface logic Video system clock = 24.5454 MHz
	Digital Color Encoder	BT9101 : This chip has Gamma correction logic, NTSC color encoder, three 8 bits video D/A converters and 3 Video amplifiers.
	Audio DAC	16 bits stereo D/A converter : Clock = 16.9344 MHz
I/O	Audio output	Stereo 16 bits PCM, sampling frequency = 44.1 KHz RCA pin jack connector x2 (Left/Right)
	Composite Video output	NTSC (RS170A standard) RCA pin jack connector x1
	S-Video output	NTSC mini DIM 4-pin connector x1
	RF modulated Video output	NTSC, channel 3 or 4 (mechanical switch selectable) RCA pin jack connector x1
	Controller Port	Low speed I/O bus for Controller, 3D glasses and etc. D-sub 9-pin connector x1
	Expansion Port	High speed I/O bus for Extension CD-ROM drive, MODEM and etc. 30-pin connector x1
	FMV Port	Connector for Full Motion Video cartridge 68-pin connector x1

•CD-ROM Drive Unit

Disc Format	Capable of reading CDs in the following standard formats: CD-DA (Audio Red Book) CD-ROM (Yellow Book) Mode 1 Mode 2 (ISO 9660) CD-ROM Mode 2 / XA Form 1 Form 2 CD-WO (Orange Book) Regular CD-WO Hybrid CD-WO (CD-Bridge, Photo-CD)	
Loading System	Tray auto loading and eject	
Data Capacity	540 MB (in case of 60 minutes CD disc)	
Transfer Rate	Audio	172.2/344.4K bytes/sec
	Mode 1	150/300K bytes/sec
	Mode 2	171.1/342.2K bytes/sec
	Mode 2 /XA form 1	150/300K bytes/sec
	Mode 2 /XA form 2	170.2/340.4K bytes/sec
Burst Transfer Rate	4M bytes/sec	
Buffer Memory	32K bytes	
Random Access Time	Typ. 350 ms (at double speed)	
Full Access Time	Typ. 750 ms (at double speed)	
Power	+9 V	Typ. 0.6 A Max. 1.5 A
	+5 V	Typ. 0.2 A Max. 0.8 A
Disc size	8 cm or 12 cm	
LED	Access indicator	
Switch	Open/Close button on main board	

•Power Supply Circuit (on Main Logic Board)

Power	Output Voltage	Max. Current	Comment
+5 V	+5.1 V +- 5%	1.0 A	Power for logic (System and CD-ROM)
+9 V	+9 V +- 5%	1.5 A	Power for CD-ROM motors and audio)
Backup	Battery : +3 V		CR2354-1GUF, 560 mAh Standby current : less than 2.5 uA Power down detect voltage : 4.2 V

•Controller (Control Pad)

Interface		3DO IM Control port specification Serial interface Controllers are physically daisy chained.
Button	Direction Pad	Left, Right Up, Down
	Button	A, B, C, X, P
	Shift Button	Right, Left
Cable	Length	3.5 m
	Signals	9 signals and 1 shield (GND)
	Connector	9-pin D-Sub male connector
Connector		9-pin D-Sub female connector This connector is used to connect more than one Controller
Headphone Jack		Mini stereo headphone jack (ø3.0)
Volume		Sound volume control for headphones

•Video Section

Video Output Level	1 V +- 20 %
Sync Level	0.286 V +-20%
Burst Level	0.286 V +0%/-40%
Signal to Noise Ratio Luminance (100% White)	> 60 dB
Signal to Noise Ratio Chroma AM (Red)	> 55 dB
Signal to Noise Ratio Chroma PM (Red)	> 55 dB
S-Video Output Level	1 V +-20%

TEST DOSC : KENWOOD SUBCODE (R-W) TEST DISK

•Digital Audio Section

Digital Audio Output Level	1.4 Vrms
Total Harmonic Distortion (1 kHz 0 dB)	< 0.03%
Signal to Noise Ratio (A-Weighted)	> 80 dB
Dynamic Range	> 80 dB
Frequency Response (20Hz refered to 1kHz)	+ 0 dB, - 0.5 dB
Frequency Response (20kHz refered to 1kHz)	+ 0 dB, - 1.8 dB

TEST DOSC : EIAJ DISK

•Physical Specification

Dimension	Width	11.2 inch (284 mm)
	Depth	10.6 inch (268 mm)
	Height	3.5 inch (88 mm)
Weight		6.6 lbs (3 Kg)
Temperature	Operating	10 to 35 °C (50°F to 95°F)
	Non operating	-20 to 60 °C (-4°F to 140°F) (When packed for shipment)

2. Block Diagrams

2-1. Power Supply Circuit Diagram

In Fig.2-1, a block diagram of the FZ-1 power supply circuit is shown.

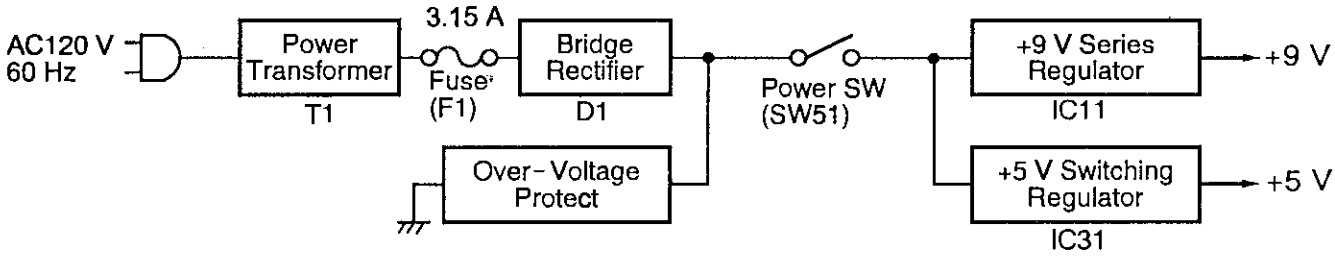


Fig. 2-1

From the AC line, DC power is created by the transformer and the rectifier circuit, passes through the +9 V series regulator and the +5 V Switching regulator, and is then supplied to the system.

+9 V is the power supply which is provided to the CD-ROM, Fan Motor and Audio Amplifiers.
+5 V is the power supply which is provided to the system board and CD-ROM.
Turning +5 V and +9 V on and off is controlled via SW51 (Power Switch on front panel of cabinet).

Rectifier circuit output is created at the point when the power cord is plugged into an AC outlet.
Rectifier circuit output voltage varies according to the state of the load placed on it.
Typical output characteristics are shown in Fig. 2-2.
The voltage at the rectifier circuit output is normally about 14.5 V when the power is on, and about 18 V when the power is off.

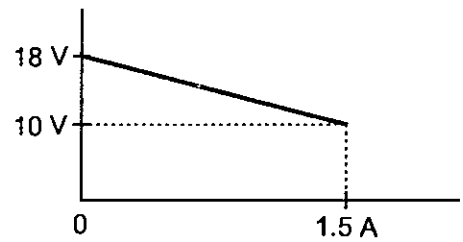


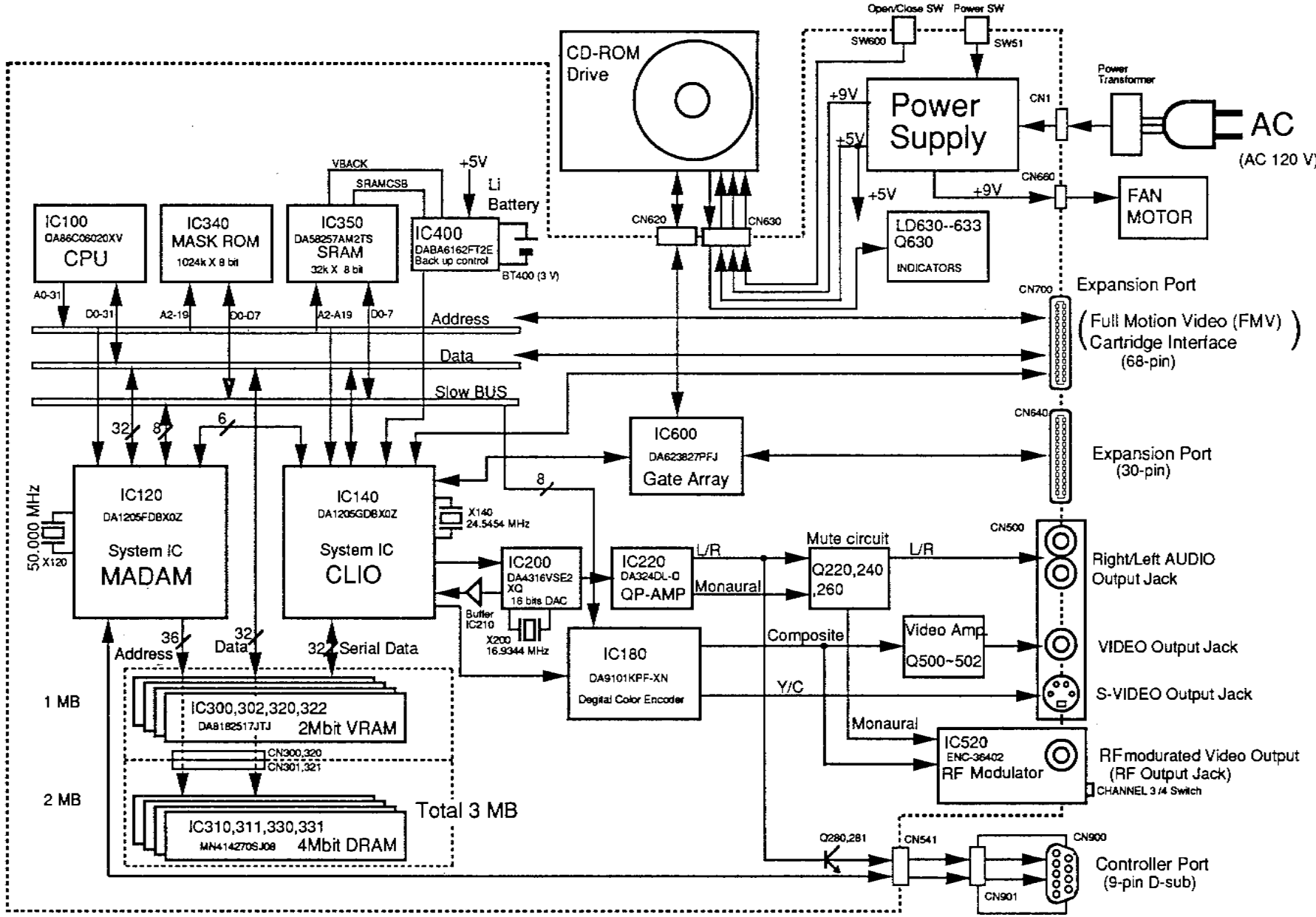
Fig. 2-2

Input AC 120V / 60Hz

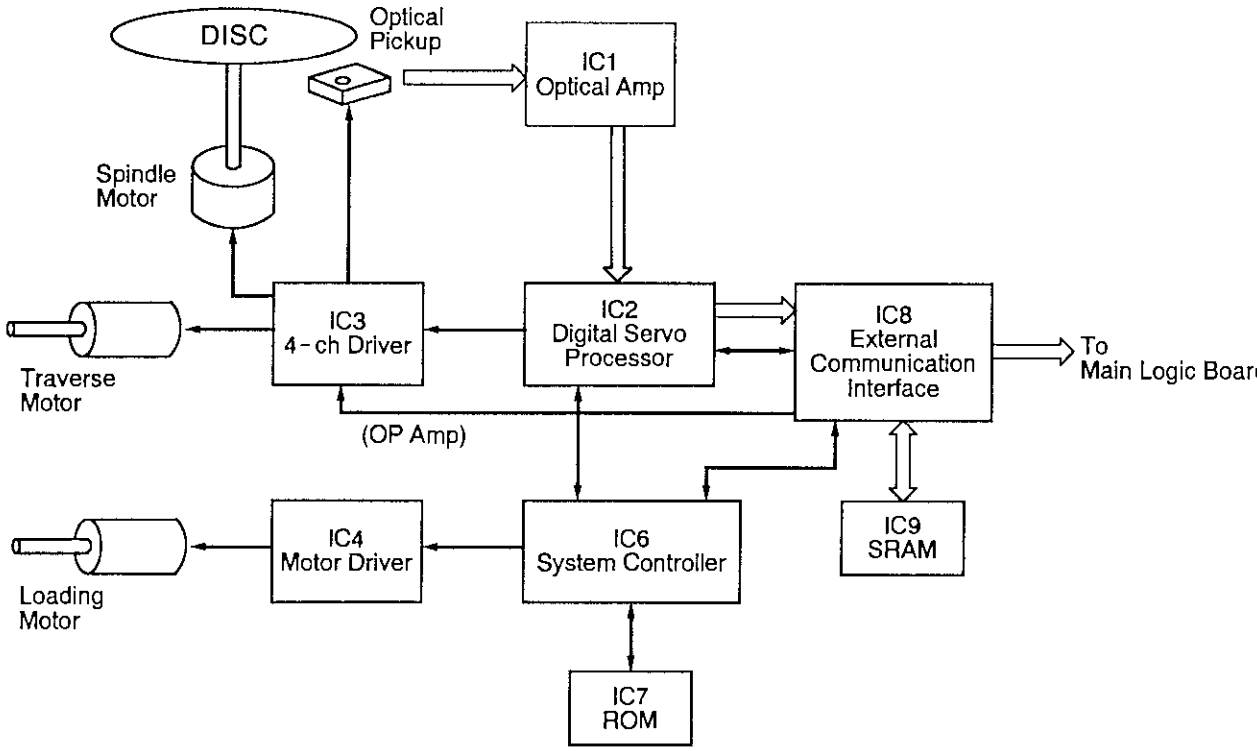
Power Name	Output Voltage (V)	Max. Current (A)
+9 V	+9 V ±5%	1.0 A
+5 V	+5.1 V ±5%	1.5 A

Output Configuration

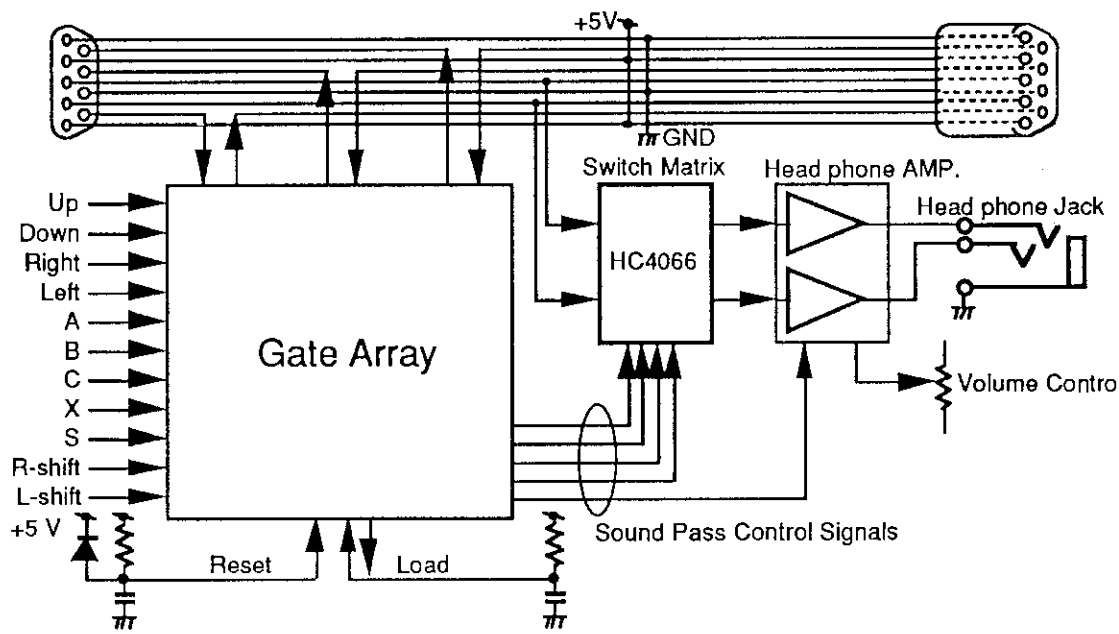
2-2. Main Logic Block Diagram



2-3. CD-ROM Drive Block Diagram



2-4. Controller Block Diagram



3. Operation

3-1. Main Logic

3-1-1. Memory

FZ-1 REAL system has 3M bytes RAM and 1M byte ROM and 32K bytes battery backup SRAM.

Memory array except ROM and NVRAM (battery backup SRAM) is 32 bits wide and 3M bytes in size. Memory consists of DRAM and VRAM (called Video RAM or Dual port DRAM). In 3DO IM system, there is no clear line between DRAM and VRAM. System can use both RAM as main RAM (for Program and data). The only difference is that System cannot use DRAM as Frame Buffer.

In our system, ARM60 CPU accesses memory as Big Endian, so the data bits of CPU are wired to the byte sections of the memory as follows :

Byte 0 is wired to bits 31 -> 24
Byte 1 is wired to bits 23 -> 16
Byte 2 is wired to bits 15 -> 8
Byte 3 is wired to bits 7 -> 0

32 bits wide VRAM is physically split two 16-bit wide memories. These 2 bank memories are controlled by MADAM with two separate address and control bus. The upper 16 bits (31 -> 16) are called the Left half and the other are called the Right half. As a Frame buffer, Left half has even line data and Right half has odd line data. Each line data are accessed individually by CLIO to do interpolation.

3-1-2. CPU and System ASICs (MADAM and CLIO)

Crystal oscillator for system clock is 50.000 MHz. This clock is divided by 2 in MADAM chip and 25.000 MHz clock is supplied to system including MADAM itself as system clock.

CPU is 32-bit RISC processor ARM60. ARM60 is running at 12.5 MHz and has 32 bits Data Bus, 32 bits Address Bus (4G Bytes) and control signals. ARM60 is designed to use DRAM fast page access mode, so during continuous DRAM read/write within one page, it takes only 80 ns per 1 access.

CPU and System ICs (MADAM and CLIO) share system devices (Memory, Hardware, Expansion bus devices and Control bus devices). The sharing is controlled by System IC and is not normal method but little forcible method. To get Bus, the System IC stops (stretches) the CPU clock (MCLK), switch Memory address by internal logic and forces Data Bus to High Impedance by DBE signal of CPU. So, it takes no time to change bus control.

3-1-3. Video system

The video sync timing and level of REAL system is based on the RS170A industry standard for television in several countries including USA.

The color burst frequency is 3.579545 MHz and video pixel clock frequency is 12.2727 MHz (= 3.579545 MHz x 2 / 455 x 780). 780 means that there are 780 pixels in the complete horizontal time. This video clock frequency is selected to get real square pixels. This clock is made by 24.5454 MHz Crystal connected with CLIO.

Video timing signals, HSYNC and VSYNC, are driven by Digital Color Encoder named BT9101 (IC180) and supplied into CLIO. This sync signal timing is based on RS170A.

CLIO makes detailed timing for memory control and send video DMA request to MADAM.

MADAM controls Serial port of VRAM using the following signals:

For Left half

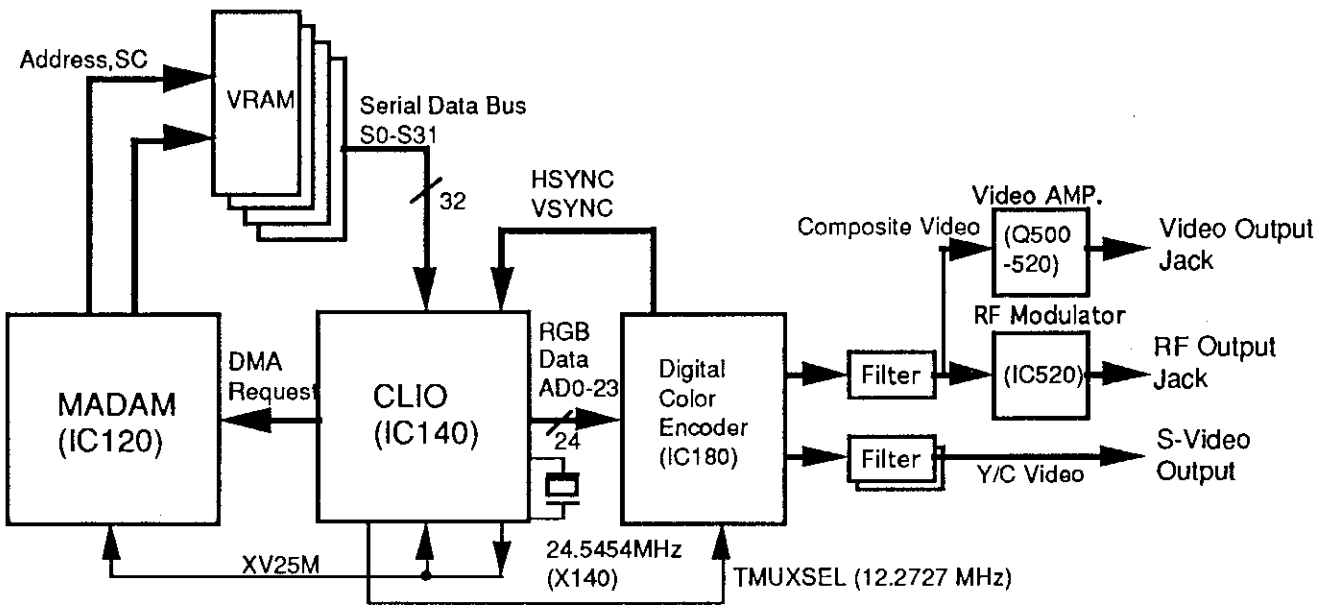
LA0-8, LRAS0B, LRAS2B, LCASB, LSC, LSOE0B, LSOE1B, LDTOEB, LDSF, LWELB, LWEUB, LQSF

For Right half

RA0-8, RRAS0B, RRAS2B, RCASB, RSC, RSOE0B, RSOE1B, RDTOEB, RDSF, RWELB, RWEUB, RQSF

CLIO read the pixel data from VRAM serial port (S0-S31), do interpolation, convert with Color Look Up Table and send result data into Digital Color Encoder. The data sent by CLIO are three 8 bit data (RGB888) per pixel.

Digital Color Encoder makes NTSC composite and Y/C separated video analog signal. Y/C separated video signal are sent directly to S-Video connector through LC low pass filter. Composite video signal is sent to RF modulator and Composite video connector through video amplifier.



Video System Block Diagram

3-1-4. Slow Bus (ROM and SRAM Bus)

3DO IM system has the Slow Bus for accessing to ROM, SRAM and other slow access devices.

ROM is one of the slow bus devices. This access is slow (about 320 ns per byte, 14,000 ns per word). ROM is located in a 1 Megabyte address range. Writes to this area have no effect. ROM is accessed by only CPU through System IC (MADAM) with an 8-bit to 32-bit data width converter. When CPU accesses to ROM, the ROM controller in System IC will actually do 4 read cycles from the bus and will capture 4 bytes of data from ROM. To access these 4 bytes of ROM data, System IC uses PDRD- and PDWR- signals as Address 0 and 1.

At release from reset, the ROM appears in the 000xxxxx range and CPU will start from ROM. The Data on ROM is copied to RAM and execute it there. Writing to any address in this range changes the assignment from ROM to RAM.

SRAM area is assigned in the 03140000 to 0317FFFF range, but only the lower byte (8 bits) of the word (32 bits) is meaningful, writes to upper 24 bits has no mean and reads from upper 24 bits is read as "0".

SRAM is backed up by Lithium battery. The BA6162F (IC400) controls SRAM battery backup. When the power is falling down, at Vcc = 4.2 volt, backup control IC switches Vcc of SRAM from 5V to battery and drives reset line to low (active).

Signal	Active	Direction	Comment
PD0	High	I/O	Data bus for Slow Bus 2^0
PD1	High	I/O	Data bus for Slow Bus 2^1
PD2	High	I/O	Data bus for Slow Bus 2^2
PD3	High	I/O	Data bus for Slow Bus 2^3
PD4	High	I/O	Data bus for Slow Bus 2^4
PD5	High	I/O	Data bus for Slow Bus 2^5
PD6	High	I/O	Data bus for Slow Bus 2^6
PD7	High	I/O	Data bus for Slow Bus 2^7
PDWR-	Low	Out	Write strobe for slow bus devices and Address 1 for ROM
PDRD-	Low	Out	Read strobe for slow bus devices and Address 0 for ROM
ROMCS-	Low	Out	ROM chip select strobe
SRAMR-	Low	Out	SRAM Read strobe
SRAMW-	Low	Out	SRAM Write strobe
PDCS0-	Low	Out	Chip select strobe for Slow Bus device area #0
PDCS2-	Low	Out	Chip select strobe for Slow Bus device area #2
PDCS3-	Low	Out	Chip select strobe for Slow Bus device area #3

Slow Bus Interface Signals

3-1-5. Expansion Port and CD-ROM Interface

Expansion Bus driven by CLIO chip is connected to CD-ROM Interface Gate Array (called OSA). The OSA is used as CD-ROM drive interface and Expansion port buffer. Expansion port signals are almost the same signals with Expansion Bus, but CD-ROM drive signals are original.

See Expansion Bus Specification section of Appendix A.

The STB- signal controls the timing of all information transfer between the 3DO IM System and the expansion devices. The 3DO IM System uses the STB- signal in conjunction with three control signals (SEL-, CMD-, and WR-) to control an expansion device. Eight possible Expansion Port transactions are possible with the encoding of the SEL-, CMD-, and WR- signals. The control signals are valid before, during, and after the assertion of the STB- signal. The control signals, however, are only guaranteed to be valid around the assertion of the STB- signal as defined in the Electrical Characteristics section of this document.

IDIN and IDOUT signals are used to determine each Expansion device's address during start up sequence. At normal states, these signals stay to High.

3-1-6. Controller Bus

Controller Bus is driven by MADAM. There is one 9-pin D-sub male connector in front of REAL system.

The Devices on the Controller Bus are communication with System using 1 clock, 1 serial data input and 1 serial data output lines. First device is connected with connector in front of the system and next devices are connected with previous devices using daisy chain connection.

In the 9 wires, there are two sound signals (L/R) and 1 analog Ground. These signal are connected to an amplifier in Controller Pad. User can hear the stereo Game and CD sounds using headphone connecting into headphone jack of Controller Pad.

See Controller Bus Specification section of Appendix A.

3-1-7. FMV Cartridge Interface

FMV (Full Motion Video) cartridge is optional device, which decodes FMV data on CD-ROM disc.

See FMV Cartridge Connector section of Appendix A.

3-1-8. Audio Circuit

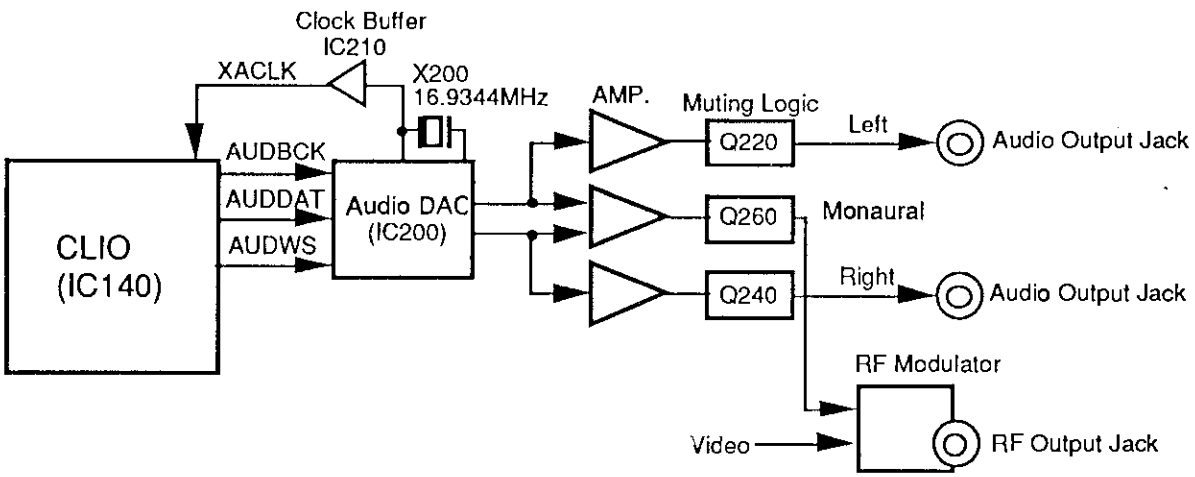
There is one DSP (Digital Signal Processor) in CLIO chip. It mixes more than 8 channels sound data read from CD disc or made by game program and perform some effects on each sound. For example, echo, emphasis, 3D sound effect and other filtering. These function are selectable because the DSP has RAM program area and also RAM data area.

These digital data are read from memory with DMA channel. DSP has FIFOs, so DMA are done efficiently.

Output Left and Right digital sound data from CLIO (DSP) go into 16-bit stereo D/A converter (IC200, AK4316). Converted sound data output to 2 types of buffer amplifiers. One is normal buffer with low pass filter and the other is mixing buffer. The former sound go to Left/Right sound out put connector and Controller Port though simple transistor buffer. The other goes into RF modulator as monaural sound and it is mixed with video signal.

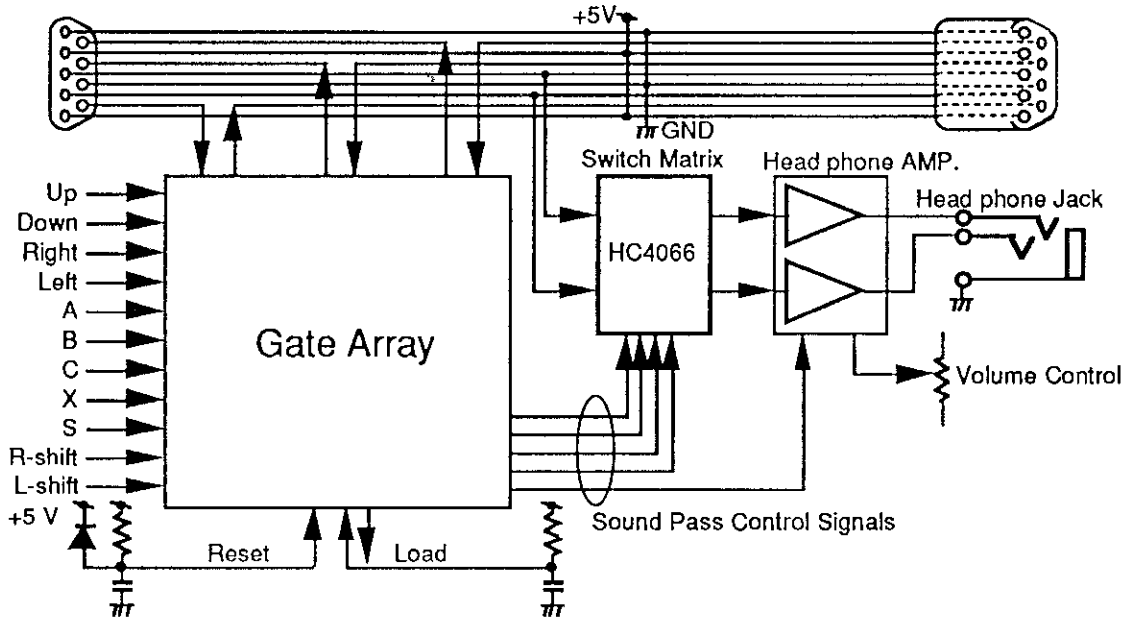
At the output of the buffer, there are Muting logic. It's made of transistors. These transistors mute sound at power on and off states.

The communication between CLIO and DAC is performed with XACLK, AUDWS, AUDBCK and AUDDAT. AUDDAT signal is a stereo audio sound packed into one serial digital data. AUDBCK is a clock for AUDDAT serial data. AUDWS indicates Left or Right word packet. XACLK comes from 16.9344 MHz crystal through clock buffer. 16.9344 MHz is 44.1 KHz x 384. This clock is used for making other signals in CLIO and over sample filtering in DAC.



Audio System

3-2. Controller (Control Pad)

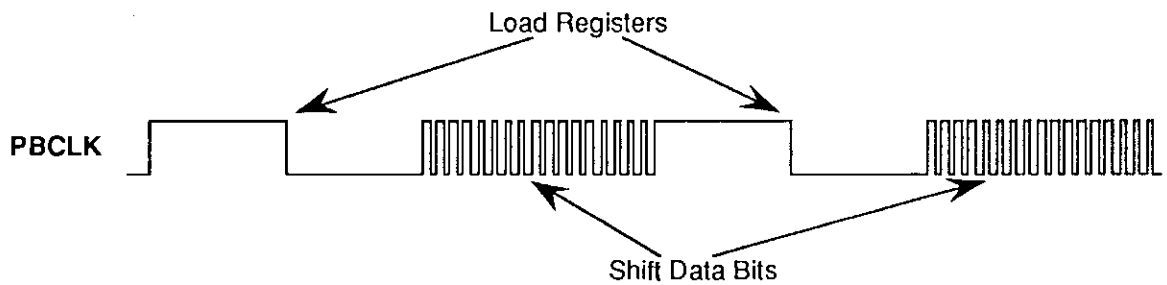


Controller Block Diagram

Controller Bus has three signals for serial communication. One is a serial data signal from System (PBDOUT), one is a serial data signal sent to System (PBDIN) and the last is serial clock (PBDCLK). This clock wave form is below.

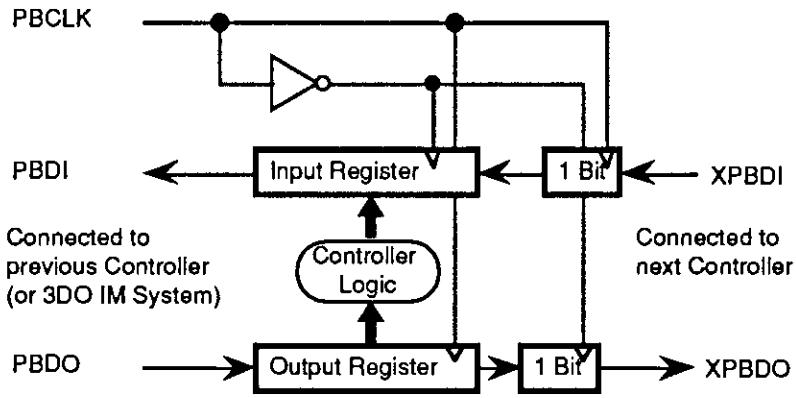
Fast clock rate is about 12.7 us and slow clock rate is about 1000 us. This clock output as Load signal to CR logic through open drain inverter and input. During clock is high at slow rate section, Load output becomes High impedance and capacitor is charged by resistor. The high level period is setup enough long for Load input to become high. By the high of Load input, the Output Shift Register latches switch data and the Input shift register changes its output.

At fast clock section, Load input never goes to high because high period is too short.



Controller Bus shift clock

Controller has 5 buttons, 2 shift buttons and 1 direction pad. They have conducive rubber switch mechanism and are connected to Gate Array (called KYO). The signal came from switch are inputted into shift register and output to system in serial with ID data. And also the signal came from next controller devices is inputted into serial input of shift register and send to system. Output data is shifted out at falling edge of PBCLK and input data is shifted in at rising edge.



Shift Register In Gate Array

Input data driven by System is shifted in into input shift register at rising edge of PBCLK. There are 2 bits shift register in the KYO. The output data of this shift register is shifted out to next controller devices at falling edge of PBCLK.

3-3. Power Logic

3-3-1. Rectifier Circuit

The rectifier circuit is shown in Fig. 3-1.
Once stepped down by the transformer, the AC output is full-wave rectified by bridge diodes and smoothed by capacitor C1, creating a DC power supply.

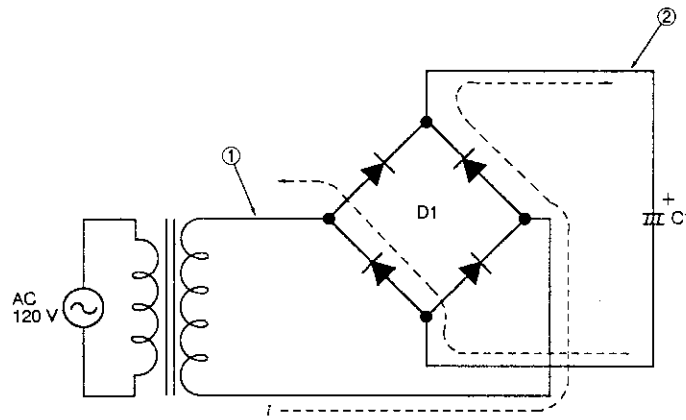
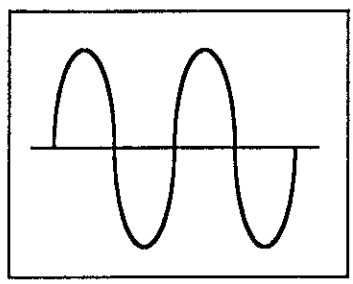
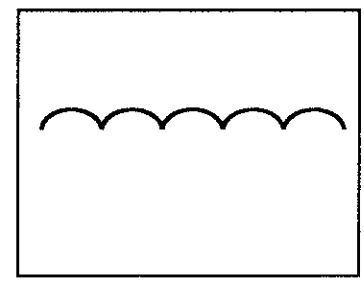


Fig. 3-1

Waveform at point ①



Waveform at point ②



The voltage at point ② is about 14.5 V when the power is on, and about 18 V when the power is off.

3-3-2. +9 V Series Regulator

+9 V is created by the IC11 (SI-3090CA) 5-terminal type IC regulator.
An internal equivalent circuit for IC11 (SI-3090CA) is shown in Fig. 3-2.

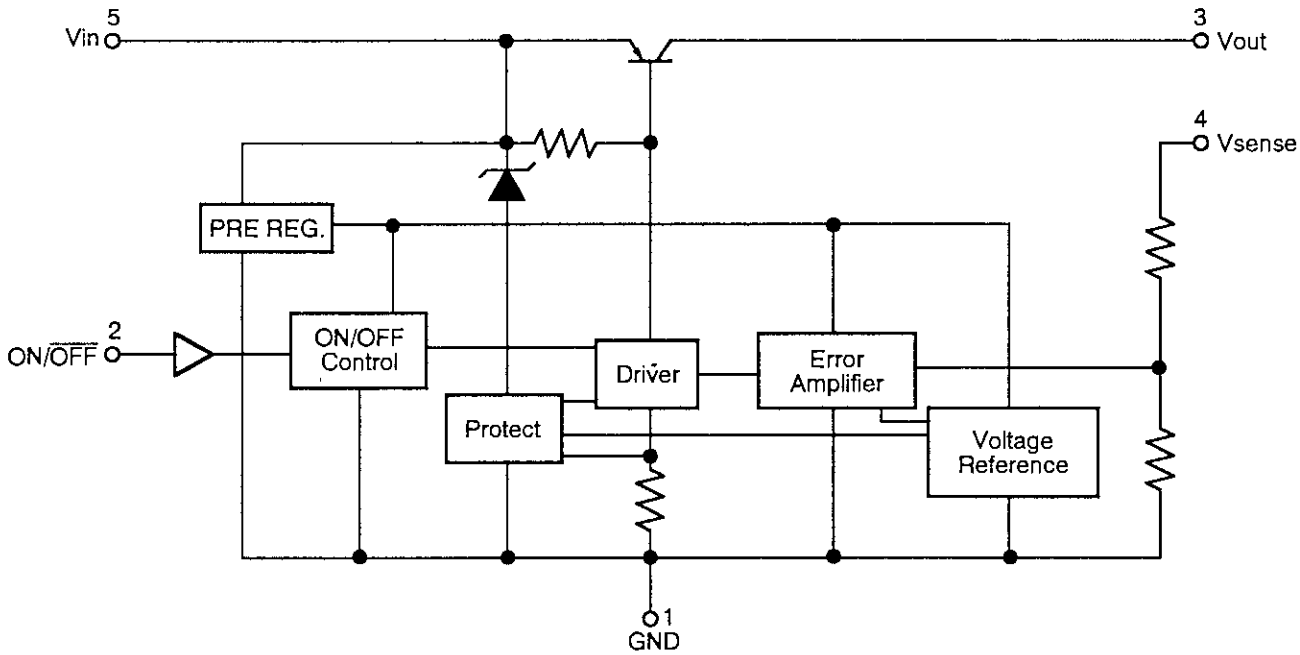


Fig. 3-2

The output on/off control terminal (pin 2) is LS-TTL compatible; 2.0 V and above causes the regulator to switch on and output +9 V.
Input pull-up is performed within the IC; when input is open, output goes on.
The on/off control terminal (pin 2) is controlled by SW51(Power Switch); when Power switch is off, it is connected to ground through a diode (see Fig. 3-3).

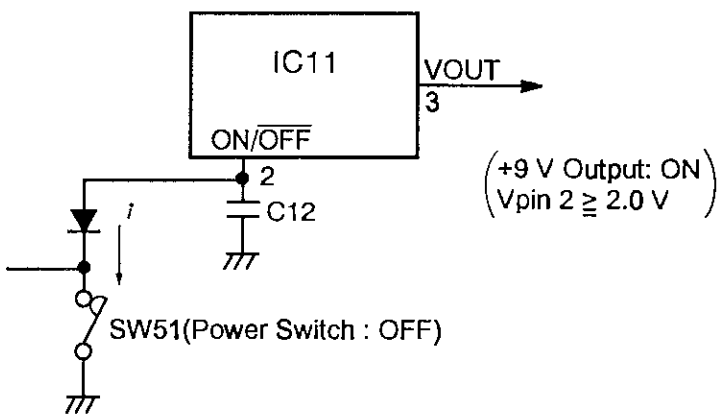


Fig. 3-3

When the power switch is pressed to turn on, SW51 becomes open, the potential at pin 2 of IC11 is increased by the pull-up resistor in the IC, and +9 V is output.
When the power is on, the voltage at pin 2 is about 2.6 V.

3-3-3. +5V Switching Regulator

+5 V is created by DC/DC conberter IC31 (L4960, built-in switching transistor type), a power switching regulator IC.

An internal equivalent circuit for IC31 (L4960) is shown in Fig. 3-4.

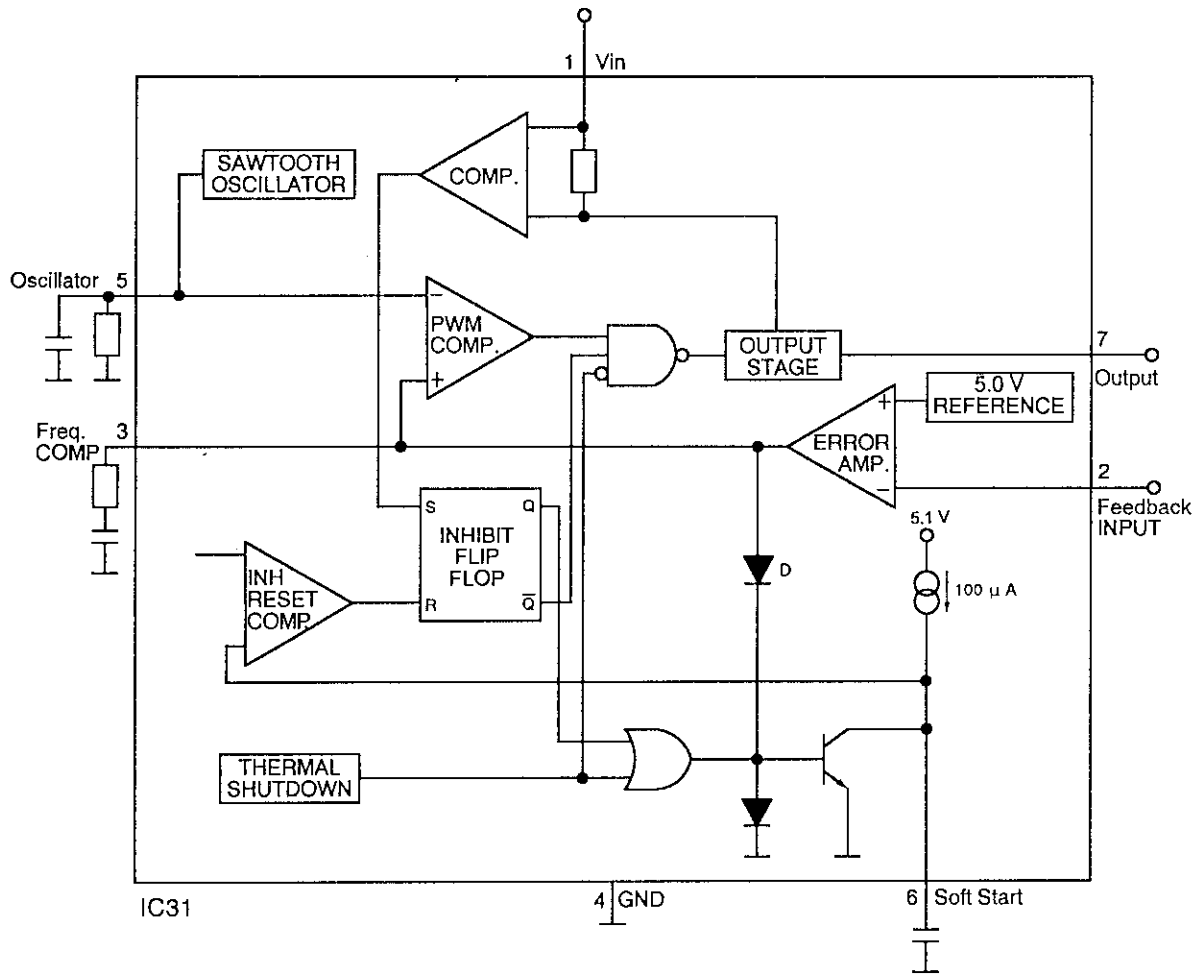


Fig. 3-4

Pin No.	Pin Name	Function
1	Vin	Power supply input terminal
2	Feedback Input	Terminal for control loop feedback
3	Frequency Compensation	Terminal for setting control loop gain
4	Ground	
5	Oscillator	Terminal for setting switching frequency
6	Soft Start	Terminal for setting the soft start time constant When set to GND level, switching halts (output goes off).
7	Output	Switching transistor output

Since there is no output on/off control pin on the IC itself, output on/off control is performed by controlling the soft start pin(Pin 6).

On IC31 (L4960), switching can be halted by setting the soft start pin to GND level.

The soft start pin is controlled by SW51(Power Switch), and is connected to ground through R51 (1 KΩ) when off. (see Fig. 3-5)

When the power switch is pressed, SW51 becomes open, the potential at pin 6 is increased by the current source in the IC, and switching begins.

When the power is on and in steady state, the voltage at pin 6 is about 5V.

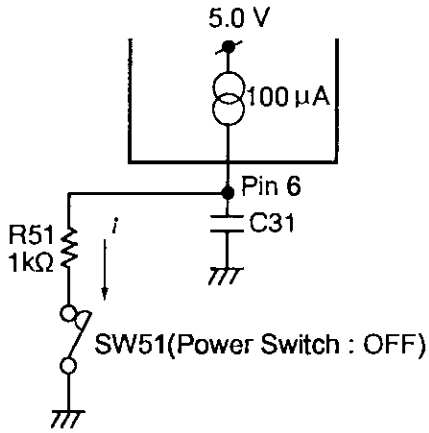


Fig. 3-5

Switching output from IC31 is smoothed by the filter comprised of L31 and C35 (see Fig. 3-6).

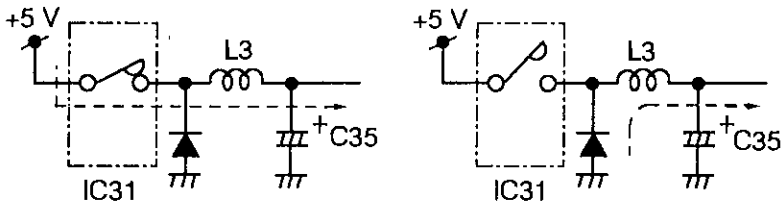
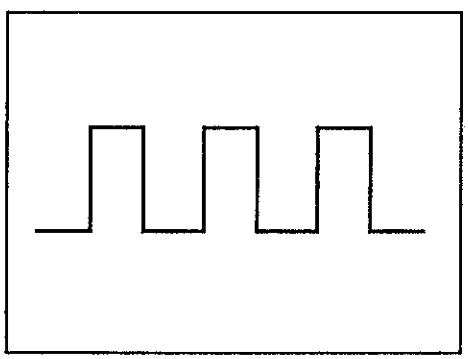
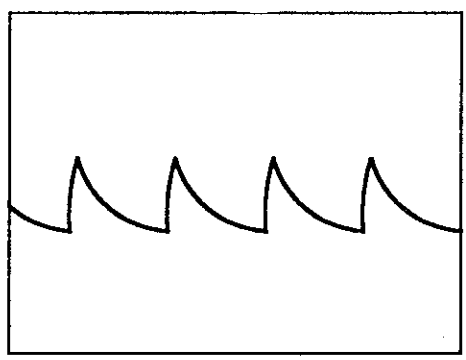


Fig. 3-6

Wavefrom at Pin 7 (Output) of IC31



Wavefrom at Pin 5 (Oscillator) of IC31



3-3-4. Over-Voltage Protection

The over-voltage detection circuit is comprised of Zener diodes(D3 D12 and D33) and a thyristor(D2).
The detection points are +9 V and +5 V, the voltage after transformer secondary-side rectification (see Fig. 3-7).

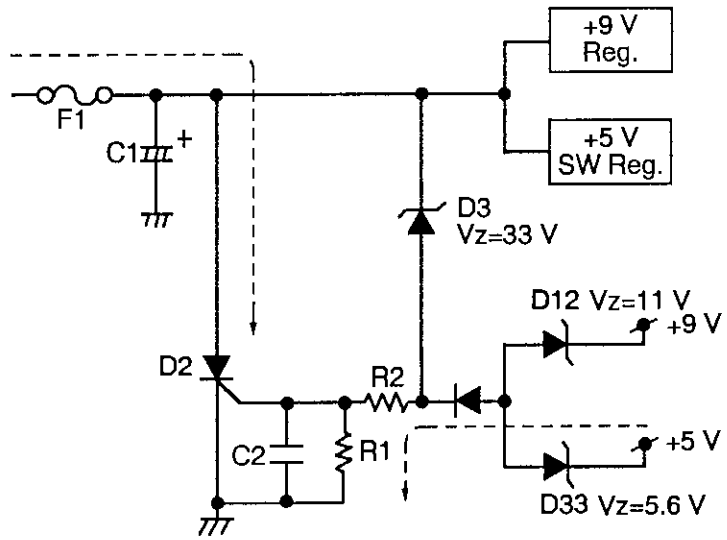


Fig. 3-7

If over-voltage occurs at one of the detection points, the Zener diode begins to conduct, increasing the gate voltage of the thyristor.
When the gate voltage reaches 0.5 V, the thyristor goes on, cutting F1 and causing the power to turn off.

Detection Point	Operating Voltage of Over-Voltage Protection
Secondary side of Power Transformer	34.0 V min.
+5 V	6.8 V min.
+9 V	11.8 V min.

3-4. CD-ROM Drive Circuit

3-4-1. Optical System and Servo Unit

Optical Pick-Up : 3-beam system is employed

Both the spindle motor (for rotating the disc) and traverse motor (for moving the entire pick-up) are driven under IC3 control. At the same time, IC3 controls the focus servo (for correcting deflection in the focal point caused by surface deviation), which is employed to correct the position of the optical pick-up lens, as well as the tracking servo (for correcting deviation in the tracking pitch caused by off-centering).
IC3 controls 4 channel servos : the spindle servo, traverse servo, focus servo and tracking servo.

3-4-2. Signal Unit

Inside the optical pick-up : disc is read by the laser beam and the optical data is sent to the photodetector (photodiode).
The optical data voltage (a very faint voltage of 1 μV to 2 μV) supplied to the photodetector is amplified to 1-3 V by IC1 (optical amplifier).
IC2 (DSP : Digital Servo Processor) processes the signal which is output from IC1 (optical amplifier) by removing noise, adjusting its phase and providing EFM demodulation.
The processed signal is passed to IC8 which provides frame synchronization and error correction and it stores the signal in the buffer memory of IC9.
The stored data is called by IC8 in accordance with the system clock and passed to the main logik circuit.

3-4-3. Function Unit

The loading motor is controlled and the tray opened and closed by IC4.
The IC6 control microcomputer and IC7 external ROM receive the signal from the main logik circuit and control the CD-ROM Drive.
IC7 external ROM : At present, this is an EPROM which contains its own 3DO program.

4. Appendix A

4-1. Expansion Bus Specification

4-1-1. Connector

The connector used for the 3DO IM Expansion Port is the Hosiden CMS 1230-010010 or equivalent. The socket is located on the 3DO IM System unit. The connector pinout is shown below. Note that the cable must be shielded. The connector located on the cable end is a Hosiden CMP1230 or equivalent.

Pin Number	Signal
1	GND
2	ADB[0]
3	ADB[1]
4	GND
5	ADB[2]
6	ADB[3]
7	GND
8	ADB[4]
9	ADB[5]
10	GND
11	ADB[6]
12	ADB[7]
13	GND
14	INT-
15	POWER

Pin Number	Signal
16	GND
17	STB-
18	CMD-
19	GND
20	RDY-
21	SEL-
22	GND
23	WR-
24	IDIN
25	GND
26	IDOUT
27	RESET-
28	GND
29	Reserved
30	Reserved
Shield	Chassis GND

3DO IM Expansion Port External Connector Pinout

4-1-2. Signals

Signal Name	I/O (relative to Expansion Device)	Description
STB-	I	Strobe signal. Used to indicate all address, data, and command transfers on the 3DO IM Expansion Port.
ADB[7:0]	I/O	Bi-directional Address and Data Bus (Tri-state outputs).
WR-	I	Write signal. Indicates command, data, or address information will be transferred from the 3DO IM System to the expansion device. Used in conjunction with the SEL- and CMD- signals to determine the transaction type.
CMD-	I	Command signal. Used in conjunction with the SEL- and WR signals to determine the transaction type.
SEL-	I	Selection signal. Used in conjunction with the CMD- and WR- signals to determine the transaction type.
RDY-	O	Ready signal. Indicates the expansion device has placed data onto the ADB bus. Also used to indicate media access (door open/close events) (Tri-state output).
INT-	O	Interrupt signal. Indicates drive has data or status information ready for transfer. (Open collector output)
RESET-	I	Power On Reset signal driven by the 3DO IM System.
IDIN	I	Input from previous expansion device. Used for device address assignment.
IDOUT	O	Output to next expansion device. Used for device address assignment.
POWER	I	Input to turn on expansion device. Provides 40 mA of 4.5 to 5.5 V per expansion connector. This signal is intended to control a power relay in an expansion device.

3DO IM Expansion Port Signals

4-2. CD-ROM Interface Gate Array (OSA) Specification

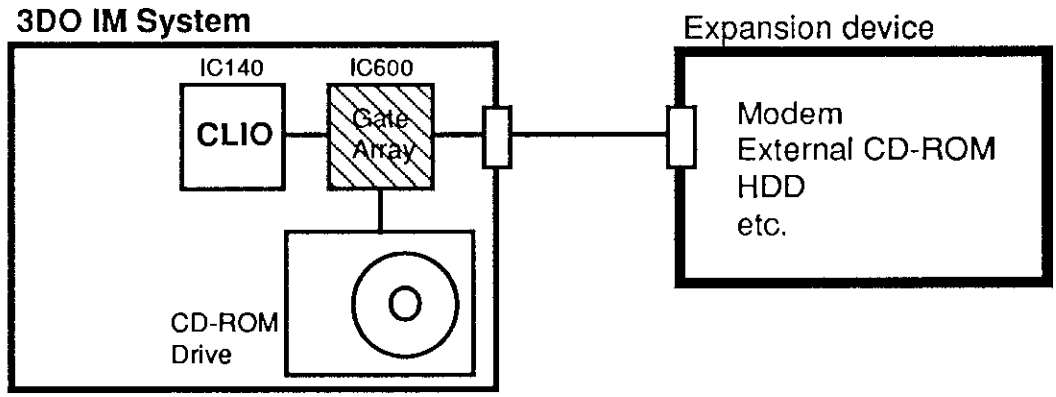
4-2-1. Introduction

This specification is for the 3DO IM System CD-ROM Interface Gate Array (IC600 called "OSA") with Expansion port.

This Gate Array is working as buffer among the CLIO Expansion bus, the Expansion port and the internal CD-ROM drive. The OSA has selection circuit for CD-ROM drive according to the 3DO IM expansion bus specification.

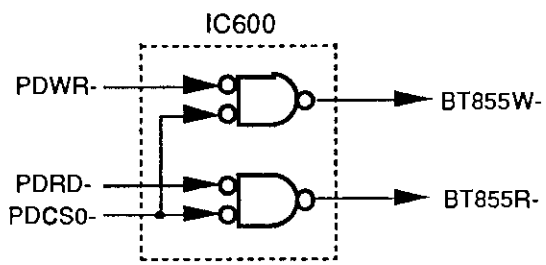
4-2-2. Connection

When the OSA is used as an expansion bus buffer and interface with an internal CD-ROM drive, the bus connections is shown below.

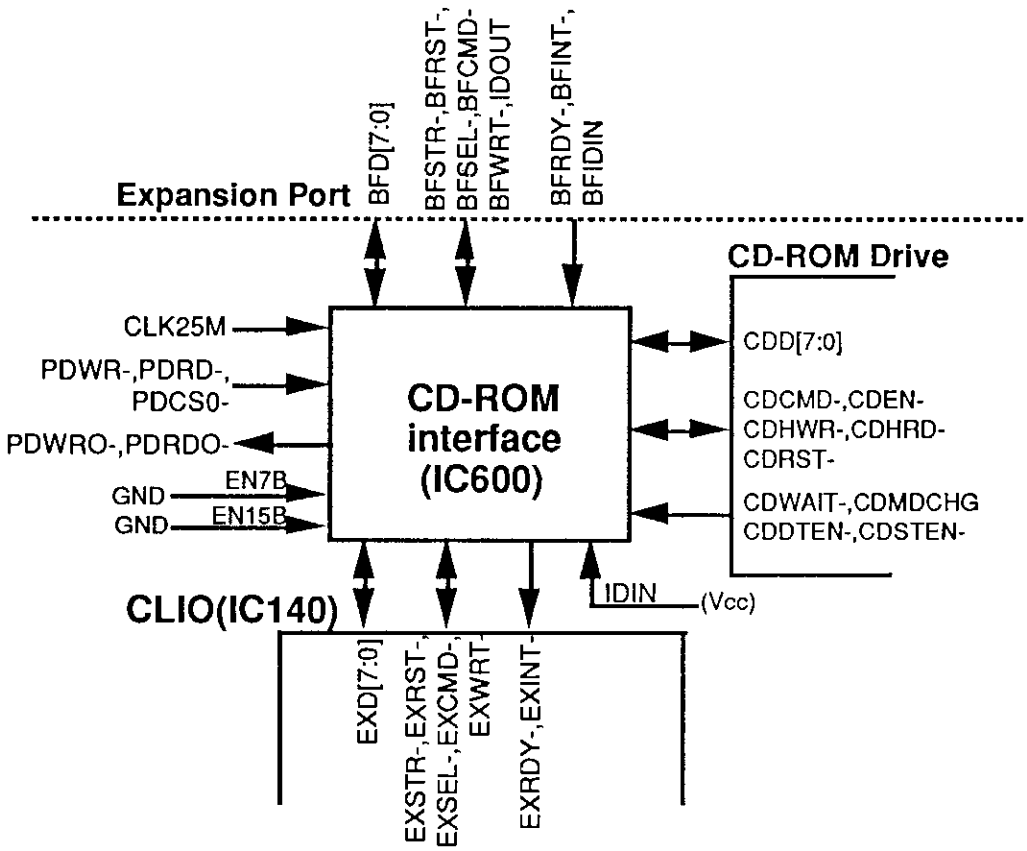


System with Internal CD-ROM Drive and Bus Buffer

And the OSA is also used to decode the Slow Bus signals. BT855W- and BT855R- are used to control Digital Color Encoder (IC180). These signals are decoded from PDWR-, PDRD- and PDCS0- signals.



Slow Bus Interface



Connection to CD-ROM Drive and Expansion Bus

BFCMD- and CDCMD- signals are used to set up the Gate Array (IC600) working mode. When this Gate Aray is used for both the CD-ROM Interface Gate Array and the Expansion bus buffer, during EXRST- signal is Low, BFCMD- and CDCMD- signals must be left High by connected with internal or external pull up resister. The BFCMD- and CDCMD- pin have internal pull-up resisters, so we have no need of connecting any external resister.

EXD[7:0], EXSTR-, EXRST-, EXSEL-, EXCMD-, EXWRT-, EXRDY- and EXINT- signals are connected to or from the CLIO chip (IC140).

CDD[7:0], CDCMD-, CDEN-, CDHWR-, CDHRD-, CDRST-, CDMDCHG, CDWAIT-, CDDTEN- and CDSTEN- signals are connected to or from CD-ROM drive

BFD[7:0], BFSTR-, BFRST-, BFSEL-, BFCMD-, BFWRT-, BFRDY- and BFINT- signals are connected to or from the Expansion BUS Connector when this Gate Array is used as external bus buffer, and to or from internal expansion devices when it's used as internal expansion bus buffer.

IDIN signal is connected to Vcc when this Gate Array used for internal 1st CD-ROM drive interface. At this setting, CD-ROM drive connected to CDxx Bus is assigned as device 0.

When used in one internal device system, IDOUT is connected to 'IDIN' of the first expansion device's connected Expansion Bus, 'IDOUT' of the first device is connected to 'IDIN' of second device, and 'IDOUT" of the last device is connected into BFIDIN signal. IDIN and IDOUT signal are used to determine the address of each devices. BFIDIN signal is used to detect connecting over 15 devices and connecting a new device after determine each device address.

When used in multi- internal device system, IDOUT is connected to IDIN of 2nd interface Gate Array, and BFIDIN is connected with IDOUT of last internal device.

EN15B signal should be pulled down or connected with GND. This setting is needed to activate device 15 function. The device 15 detects the violation that user turns on expansion device after address assignment sequence or user connects over 15 devices on expansion bus.

EN7B signal should be connected with GND. EN7B will be used timing control by system.

4-3. CD-ROM Drive Specification

4-3-1. Introduction

This specification is for the 3DO IM System internal and external CD-ROM drives. The CD-ROM drive attaches to either the internal or external portion of the 3DO IM Expansion Port. Minor differences in the two drives exist and are highlighted in the text.

The important characteristics of the CD-ROM drive are:

- **No** direct audio conversion capability is available
- Single and double speed playback modes are supported
- Capable of reading CD's in the following standard formats:

  CD-DA (Audio Red Book)
  CD-ROM (Yellow Book)
  Mode 1
  Mode 2
  (ISO 9660)
  CD-ROM Mode 2 / XA
  Form 1
  Form 2
  CD-WO (Orange Book)
  Regular CD-WO
  Hybrid CD-WO (CD-Bridge, Photo-CD)

- FIFO based data interface to 3DO IM System
- 32K Bytes Buffer Memory
- 4.0 Mbytes/sec burst transfer rate from buffer to 3DO IM System
- Supports transfer of audio information and sub-code information over digital 3DO IM Expansion Port.
- Supports both 8 cm and 12 cm discs

4-3-2. Connectors

CD-ROM drive uses two sets of Connectors and Flat cables.

Pin Number	Pin Name	Comment
1	LED	Access LED
2	EJECT	Open/Close switch input
3	+5V	
4	+5V	
5	GND	
6	GND	
7	GND	
8	GND	
9	GND	
10	+9V	
11	+9V	
12	+9V	

CD-ROM Interface Connector for Power

Pin Number	Pin Name	Comment
1	CDRST-	RESET signal for CD-ROM drive
2	CDMDCHG	Media Change signal
3	GND	
4	CDCMD-	Data/Command-
5	GND	
6	CDSTEN-	Status Valid signal
7	GND	
8	CDDTEN-	Data Chunk Valid signal
9	GND	
10	CDWAIT-	Wait signal
11	GND	
12	CDHRD-	Read strobe
13	GND	
14	CDHWR-	Write strobe
15	GND	
16	CDEN-	Enable CD-ROM access
17	GND	
18	CDD7	Data Bus 2^7
19	GND	
20	CDD6	Data Bus 2^6
21	GND	
22	CDD5	Data Bus 2^5
23	CDD4	Data Bus 2^4
24	GND	
25	CDD3	Data Bus 2^3
26	CDD2	Data Bus 2^2
27	GND	
28	CDD1	Data Bus 2^2
29	GND	
30	CDD0	Data Bus 2^1

CD-ROM Interface Connector for Signals

4-3-3. Commands

All commands sent to the CD-ROM drive are 7 bytes in length except the Abort command. A summary of the commands and their corresponding Operation Code is shown below. The Operation Code is the first byte of the command.

Drive Commands	Operation Code	Bytes In Data FIFO	Bytes In Status FIFO
Seek	01H	0	2
Spin Up	02H	0	2
Spin Down	03H	0	2
Diagnostics	04H	0	2
Drawer Open	06H	0	2
No Operation	05H	0	2
Drawer Close	07H	0	2
Abort	08H	0	2
Mode Set	09H	0	2
Reset	0AH	0	0
Flush	0BH	0	2
Read Data	10H	Variable	2
Data Path Check	80H	0	4
Read Error	82H	0	10
Read Identification	83H	0	12
Mode Sense	84H	0	7
Read Capacity	85H	0	7
Read Header	86H	0	6
Read Sub Q	87H	0	12
Read UPC	88H	0	10
Read ISRC	89H	0	12
Read Disc code	8AH	0	12
Read Disc Information	8BH	0	8
Read TOC	8CH	0	10
Read Session Information	8DH	0	8

Drive Commands and Operation Codes

All commands except the Reset Command return a Status Byte in the Status Return FIFO. The Status Byte describes the success or failure of the command. It is the last byte placed into the Status Return FIFO. All commands except the Read Sub Q command and the Reset Command also return a Command Tag Byte in the Status Return FIFO. The Command Tag byte is the first byte placed in the Status Return FIFO and corresponds to the Operation Code of the command.

4-4. Controller Bus Specification

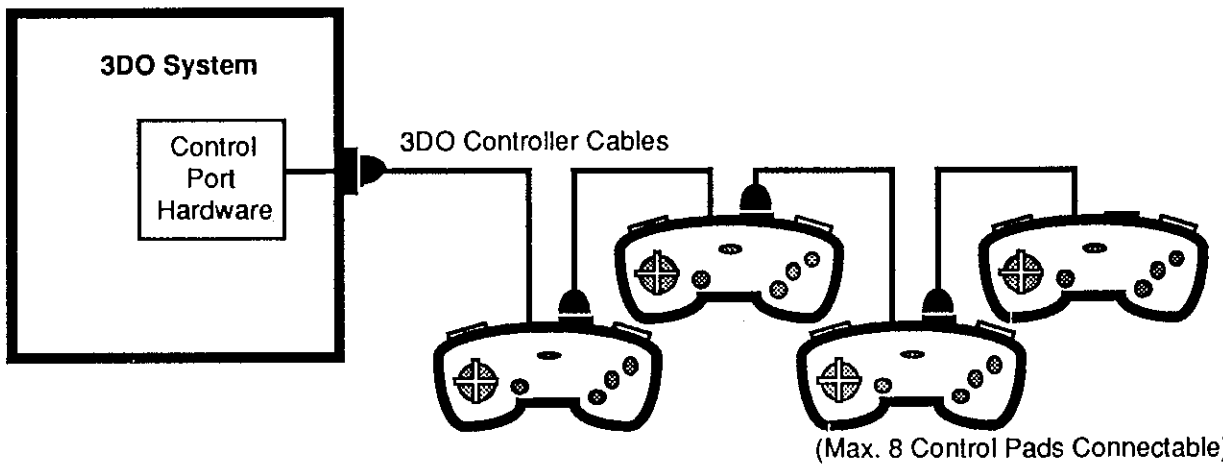
4-4-1. Introduction

This specification is for the 3DO IM Control Port and the 3DO IM Controllers. The 3DO IM Control Port and its protocol are intended to provide an inexpensive and simple method for connecting peripherals, (called 3DO IM Controllers, or just Controllers in this document) to the 3DO IM System. Controllers are generally mechanisms such as control pads, 3-D glasses, mouse, keyboards, and other user-centric devices. Users can have multiple copies of the same device (example: 4 control pads) or combinations of different types of devices connected to the Control Port.

3DO IM Controllers are connected to the 3DO IM System at the 3DO IM Port. Only the first Controller is connected directly to the Control Port. Any additional Controllers are attached in a daisy-chained manner.

4-4-2. Physical Specification

The 3DO IM System has a single socket connector on the system unit. Each 3DO IM Controller has a cable which connects to a socket and each Controller also has a single socket connector for an additional device to be connected. The basic cabling method is shown below:



Control Port Cabling

The devices are physically daisy chained together. All 3DO IM Controllers must have both the cable with plug and the socket.

4-4-3. Connector

The Control Port connects a 9-wire cable to the system unit. The System includes at least one socket connector (9-pin D-sub male connector or equivalent) on the system unit. Each Controller includes a cable with a plug (9-pin D-Sub female connector or equivalent) and a socket connector. The connector pinout is shown below:

Pin Number	Signal
1	PBRAG
2	PBVCC
3	PBRA
4	PBLA
5	PBVCC +5V
6	PBDO -- Data from System
7	PBCLK
8	PBLAG
9	PBDI -- Data in to System

Control Port Connector Pinout

4-4-4. Signals

The Control Port consists of the signals listed in the table below:

Signal Name	I/O (relative to Controller)	I/O (relative to Control Port)	Description
PBCLK	I	O	Clock signal. Indicates each cycle at the Control Port and register transfer times.
PBLA	I	O	High impedance audio signal for Left Channel
PBLAG	I	O	Audio Ground for Left Channel
PBRA	I	O	High impedance audio signal for Right Channel
PBRAG	I	O	Audio Ground for Right Channel
PBDI	O	I	Data input to System from Controller(s)
PBDO	I	O	Data output from System to Controller(s)

Control Port Signals

4-5. FMV Cartridge Connector

Pin Number	Signal
1	A2
2	A3
3	GND
4	A4
5	A5
6	A14
7	NC
8	A15
9	UNCREQW
10	UNCREQR
11	GND
12	UNCACKW
13	UNCACKR
14	D31
15	D30
16	D29
17	D28
18	D27
19	GND
20	D26
21	D25
22	D24
23	NC
24	D23
25	D22
26	D21
27	GND
28	D20
29	D19
30	D18
31	D17
32	D16
33	D15
34	D14
35	GND

Pin Number	Signal
36	D13
37	D12
38	D11
39	NC
40	D10
41	D9
42	D8
43	GND
44	D7
45	D6
46	D5
47	D4
48	D3
49	D2
50	D1
51	GND
52	D0
53	EXTREQW
54	EXTREQR
55	GND
56	EXTACKW
57	EXTACKR
58	CLC0
59	GND
60	CLC1
61	CLC2
62	RESET-
63	GND
64	CREADY-
65	UNCINT-
66	POWER
67	NC
68	X25M
Shield	GND

FMV Cartridge Connector

Signal Name	Active	I/O	Description
A[5:0]	High	Out	Address input
D[31:0]	High	I/O	Bi-directional data bus
CLC[2:0]	High	Out	Control code
RESET-	Low	Out	System reset output
UNCREQW	High	In	Video DMA Write request
UNCREQR	High	In	Video DMA Read request
UNCACKW	High	Out	Video DMA Write Acknowledge
UNCACKR	High	Out	Video DMA Read Acknowledge
EXTREQW	High	In	Audio DMA Write request
EXTREQR	High	In	Audio DMA Read request
EXTACKW	High	Out	Audio DMA Write Acknowledge
EXTACKR	High	Out	Audio DMA Read Acknowledge
CREADY-	Low	In	Acknowledge for CLC[0:2]
X25M	High	Out	25 MHz clock
UNCINT-	Low	In	Interrupt request

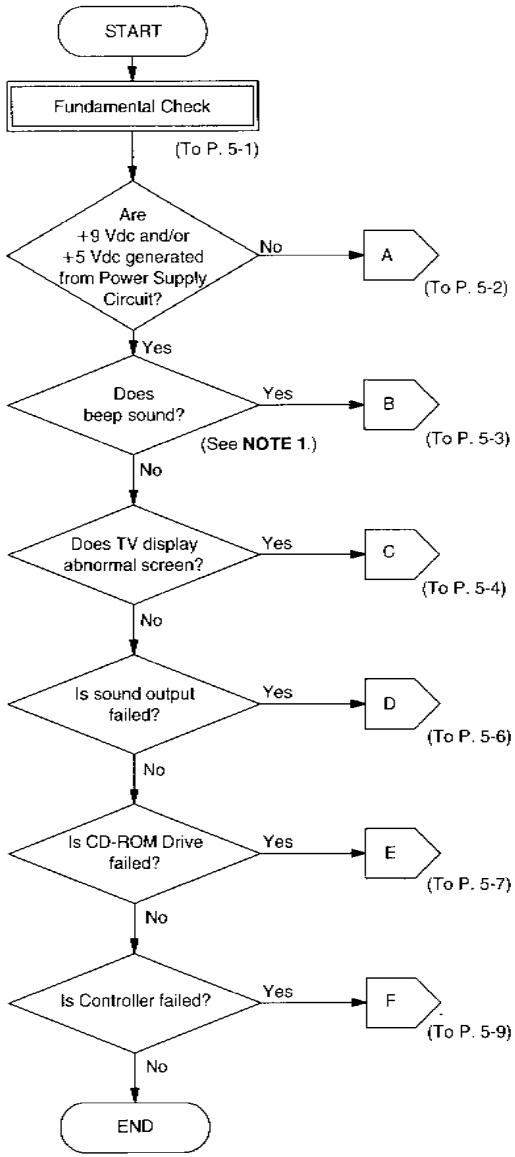
FMV Cartridge Signals

5. Troubleshooting

5-1. Flow Chart

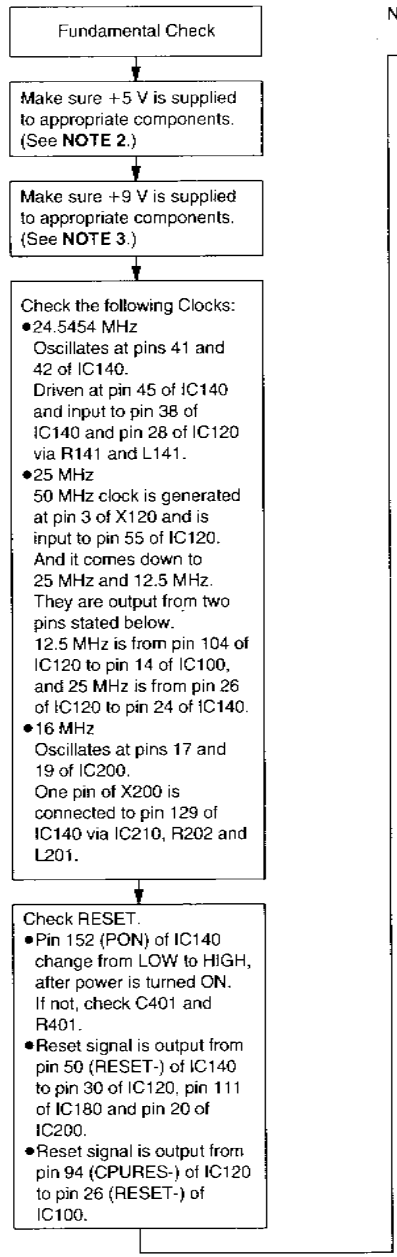
5-1-1. Main Flowchart

Note: Placing any disc into its tray is not required in the following main flowchart.

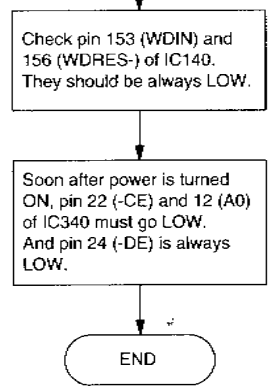


NOTE 1: Beep may be heard when power switch is turned ON, if system has problem.
Thus, sound level should be set to appropriate level with volume control of TV.

5-1-2. Fundamental Check



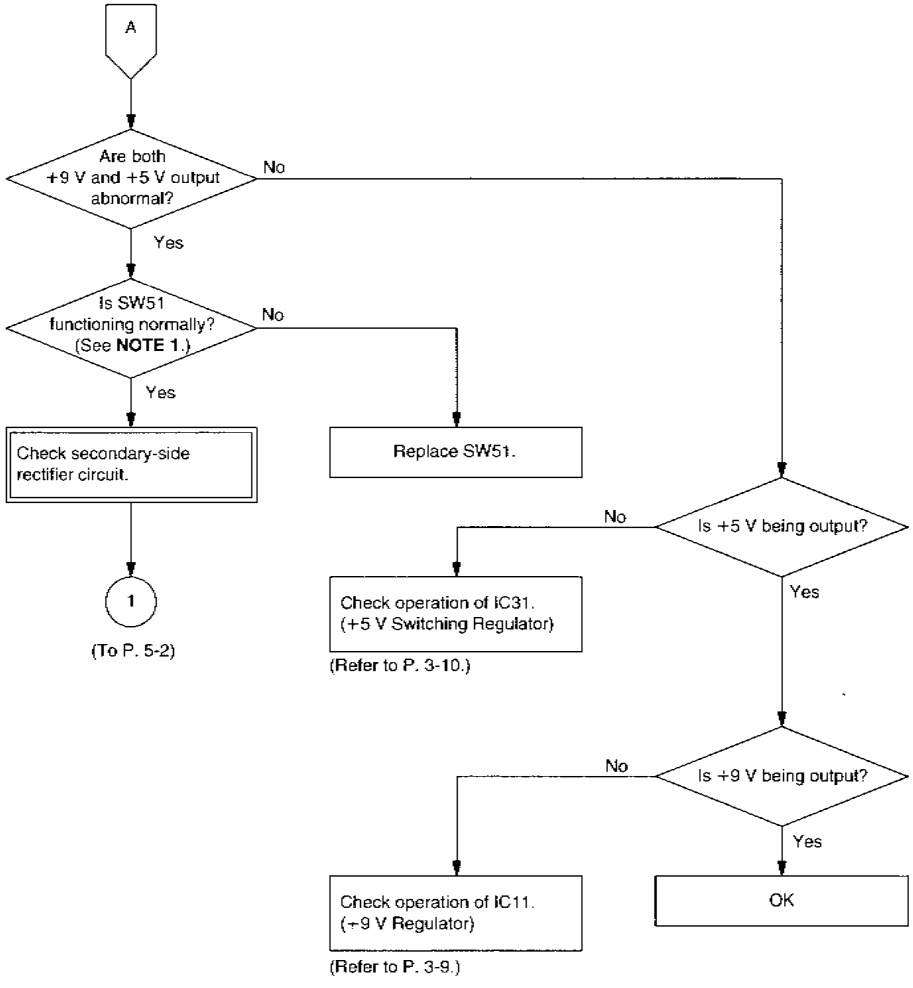
Note: Fundamental check can be done without placing any disc into its tray.

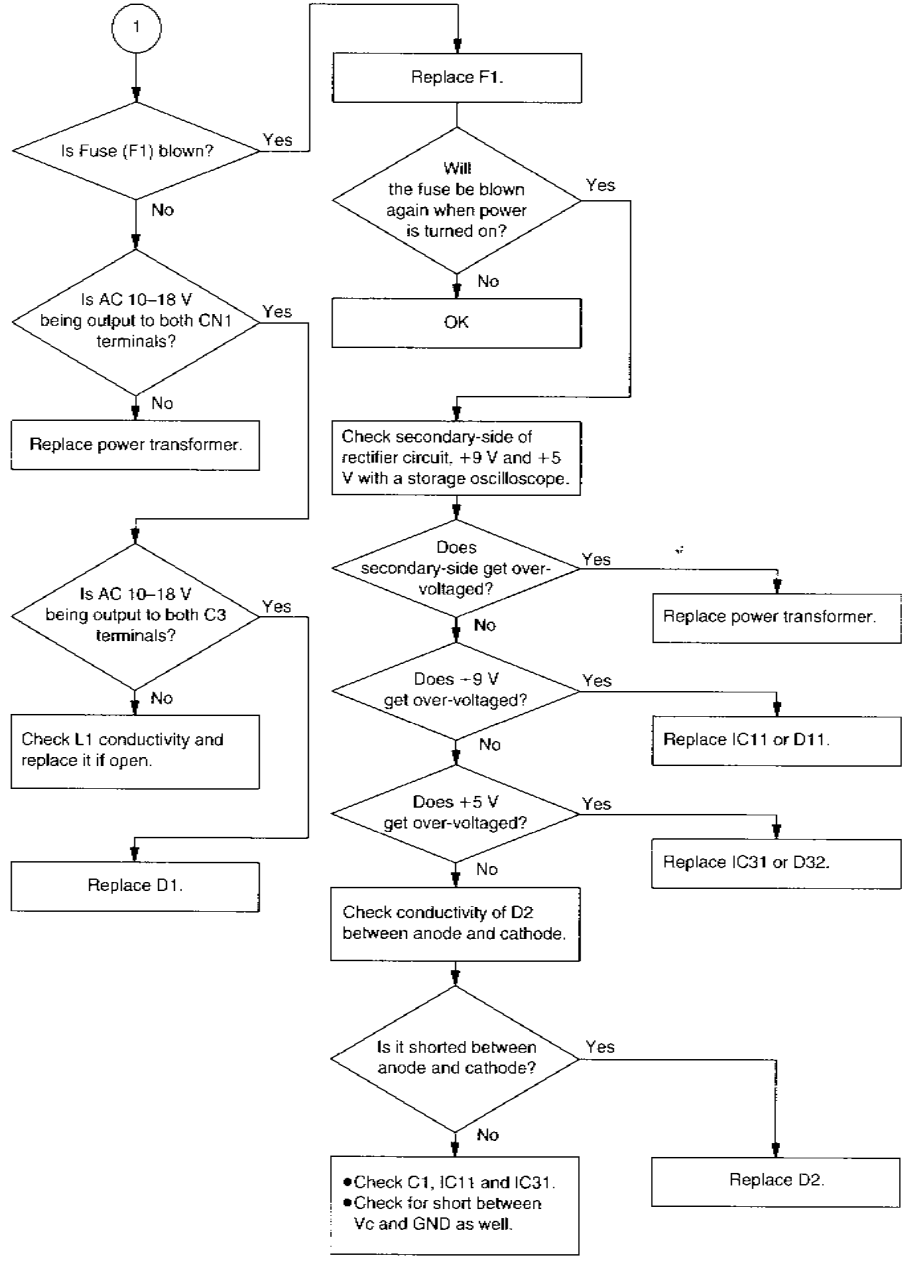


NOTE 2: IC100, IC340 and etc., for other components refer to schematic diagram.

NOTE 3: IC220, IC201 and etc., for other components refer to schematic diagram.

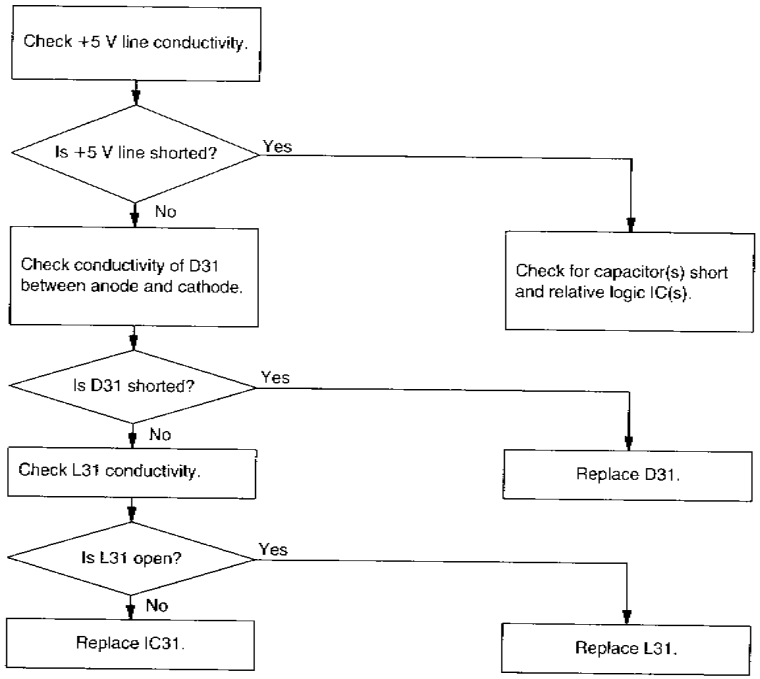
5-1-3. Power Logic Check



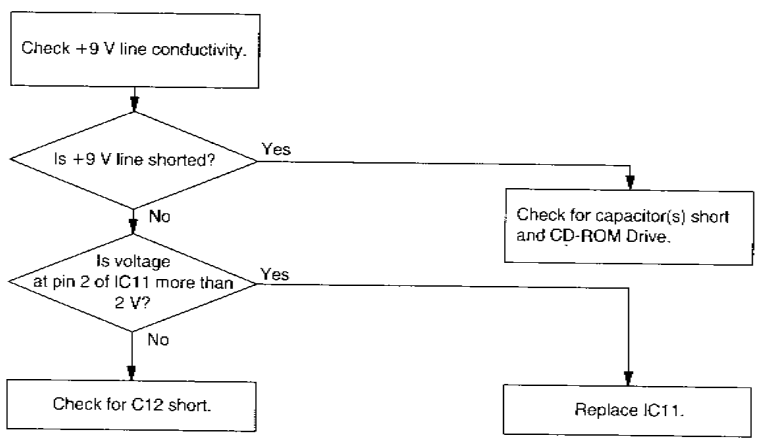


NOTE 1: With power on: Power Switch (SW51) should be shorted between pins 2 and 3.
With power off: Power Switch (SW51) should be shorted between pins 1 and 2.

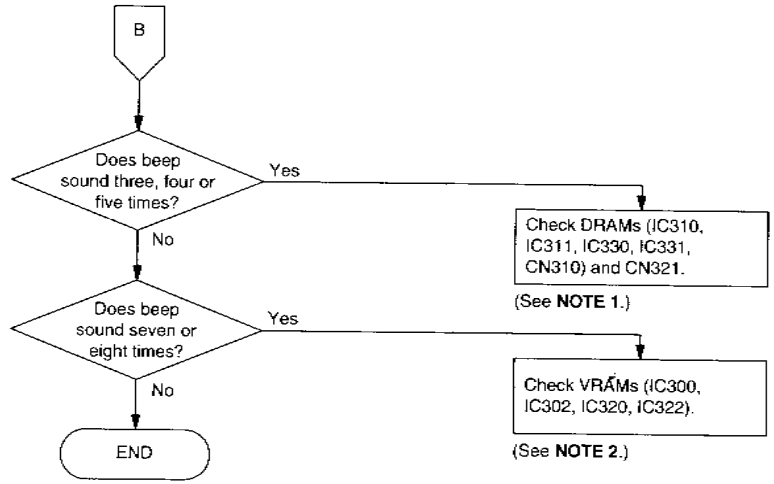
+5 V Switching Regulator



+9 V Series Regulator



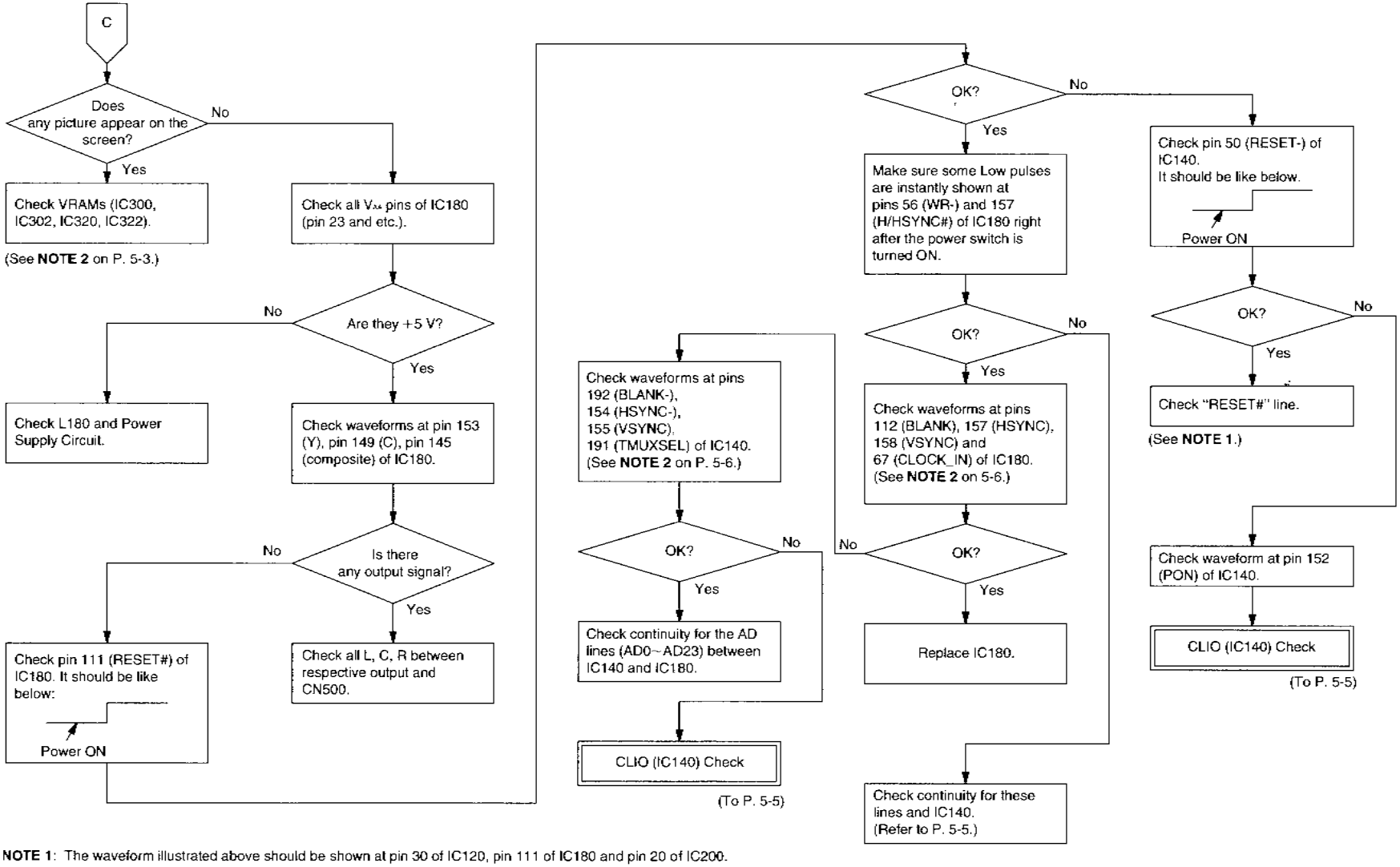
5-1-4. DRAM/VRAM Check



NOTE 1: Check V_{cc} and V_{ss}, and all signals at address, data and control pins whether these signals are input or output from/to DRAM's.
Signals on address and data lines should not be fixed at High, Low or middle level.

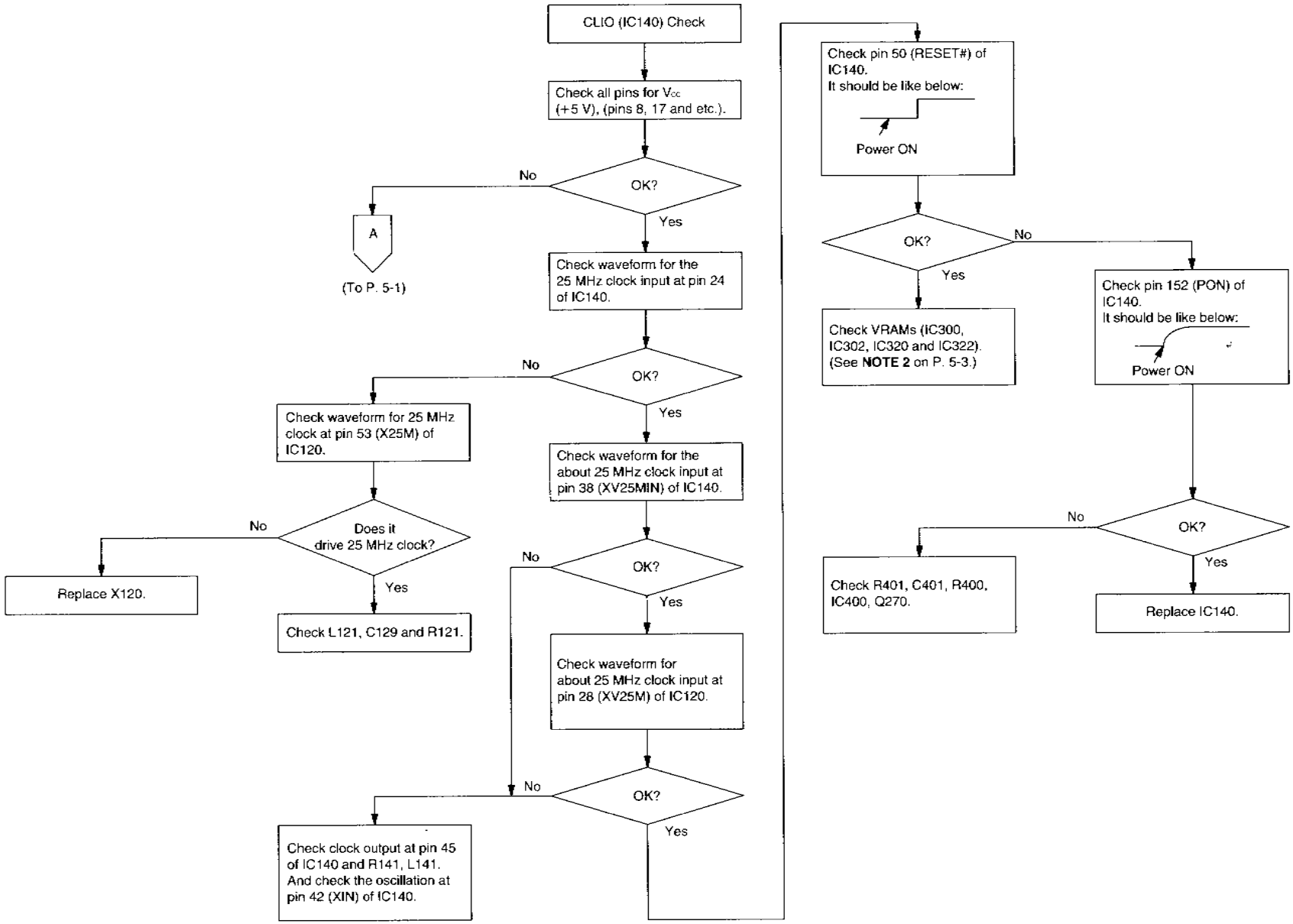
NOTE 2: Check V_{cc} and V_{ss}, and all signals at address, data and control pins whether these signals are input or output from/to VRAM's.
Signals on address and data lines should not be fixed at High, Low or middle level.

5-1-5. Video Check

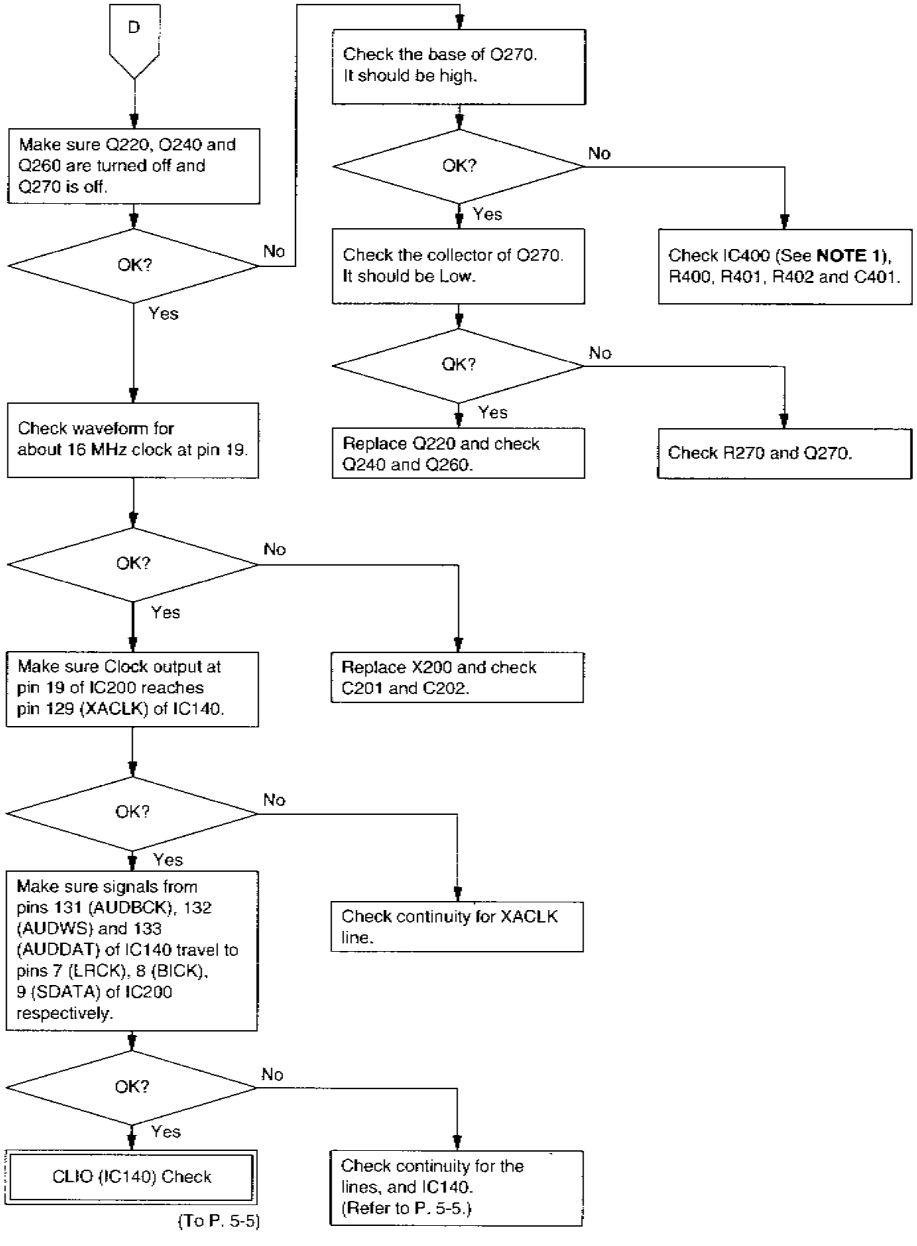


NOTE 1: The waveform illustrated above should be shown at pin 30 of IC120, pin 111 of IC180 and pin 20 of IC200.

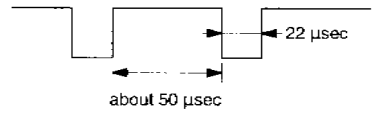
5-1-6. CLIO Check (IC140)



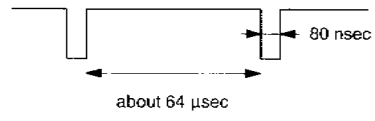
5-1-7. Audio Check



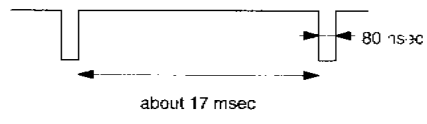
NOTE 1: Make sure pin 2 of IC400 is not shorted.
NOTE 2: •Pin 112 (BLANK) of IC180 and pin 192 (BLANK-) of IC140



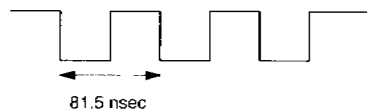
•Pin 157 (HSYNC) of IC180 and pin 154 (HSYNC-) of IC140



•Pin 158 (VSYNC) of IC180 and pin 155 (VSYNC) of C140

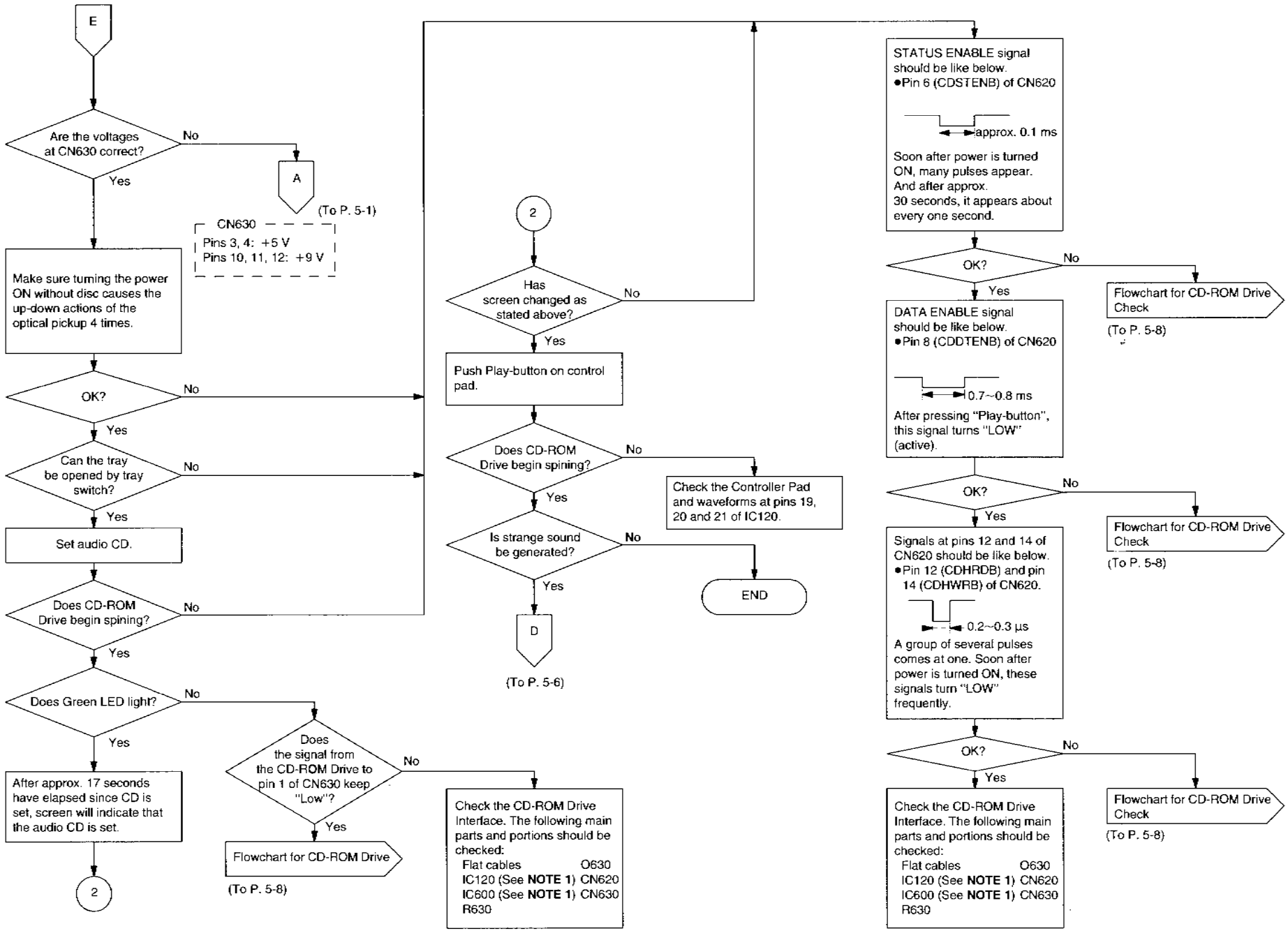


•Pin 67 (CLOCK_IN) of IC180 and pin 191 (TMUXSE_) of IC140



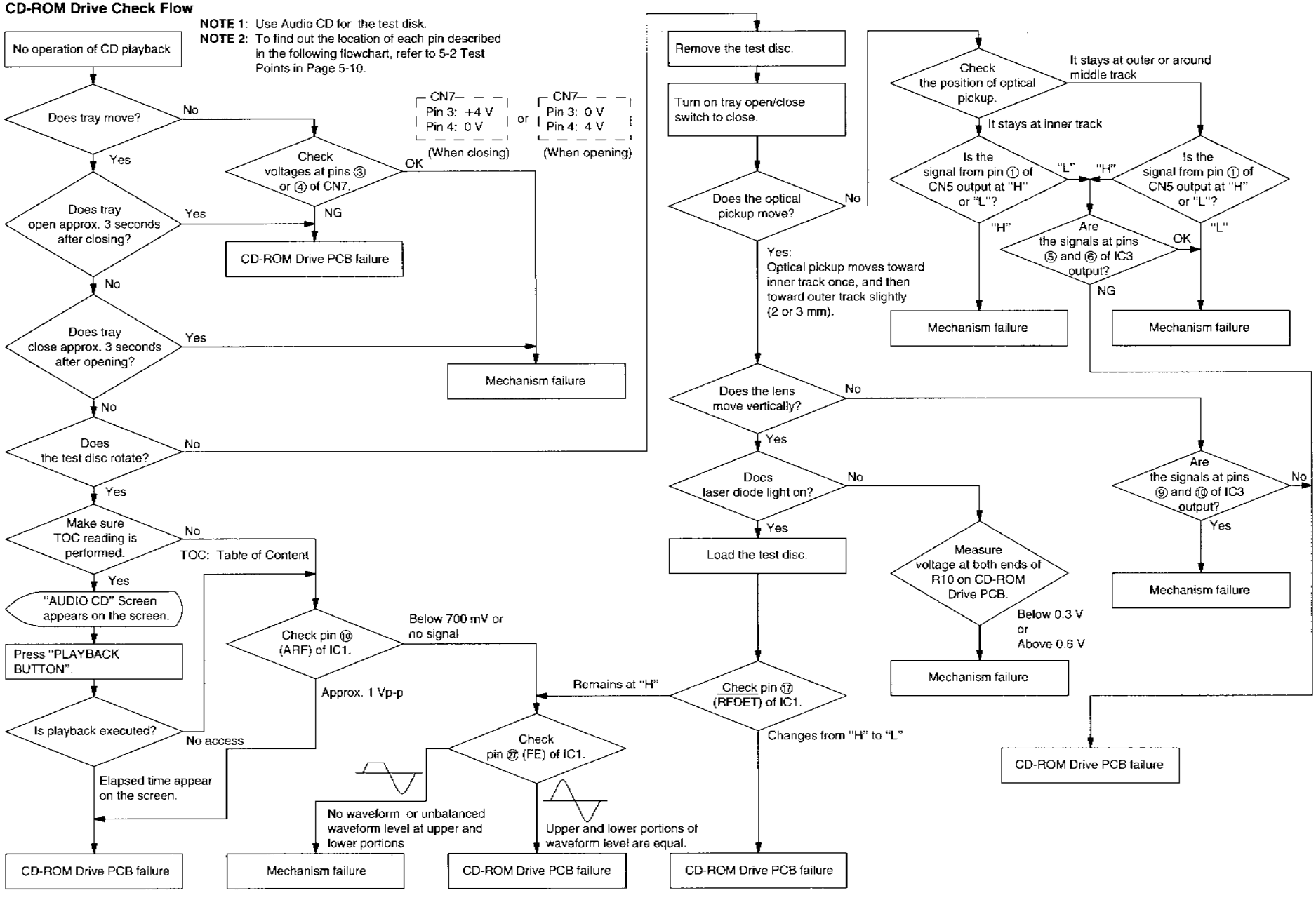
5-1-8. CD-ROM Drive Check

NOTE 1: Perform fundamental check again and check waveforms at pins related to CD-ROM Drive interface.

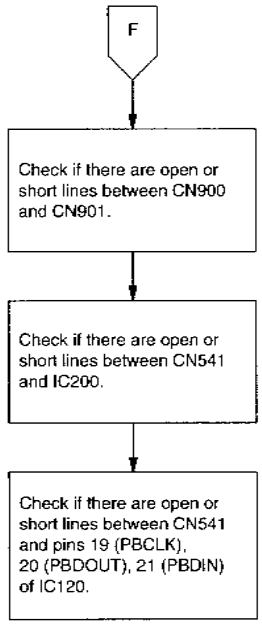


CD-ROM Drive Check Flow

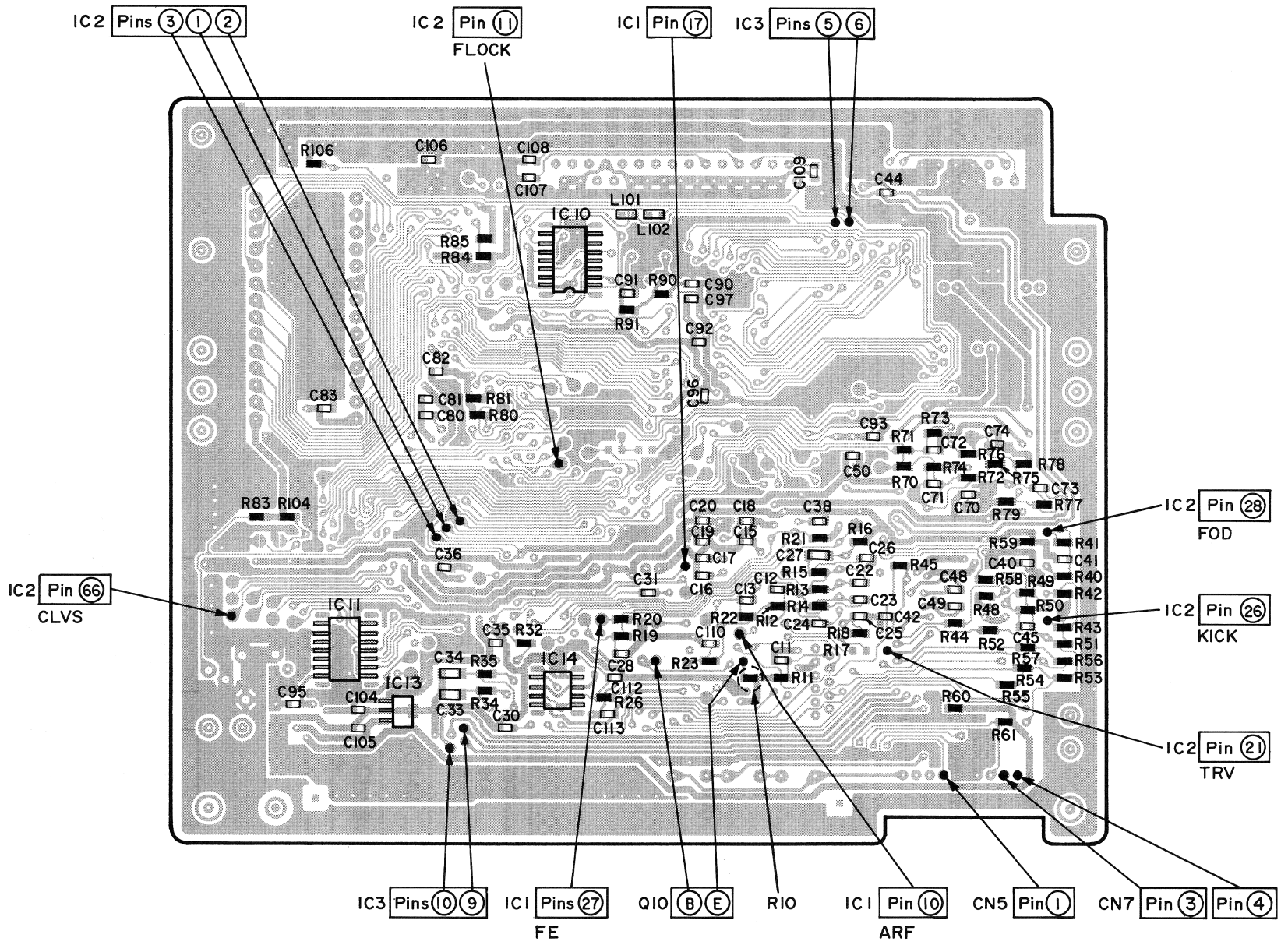
NOTE 1: Use Audio CD for the test disk.
NOTE 2: To find out the location of each pin described in the following flowchart, refer to 5-2 Test Points in Page 5-10.



5-1-9. Controller Check



5-2. Test Points



Bottom view of CD-ROM DRIVE PCB

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