SCHEMATIC REV	PBA NUMBER	REV	BOM RELEASE DATE
9.0	A32848-900	01	08/30/01

DVT

REV 9.0

FAB K

STANDARD BOM: MICRON DDR

SEE PAGE 13 FOR SAMSUNG ALT

NOTES:

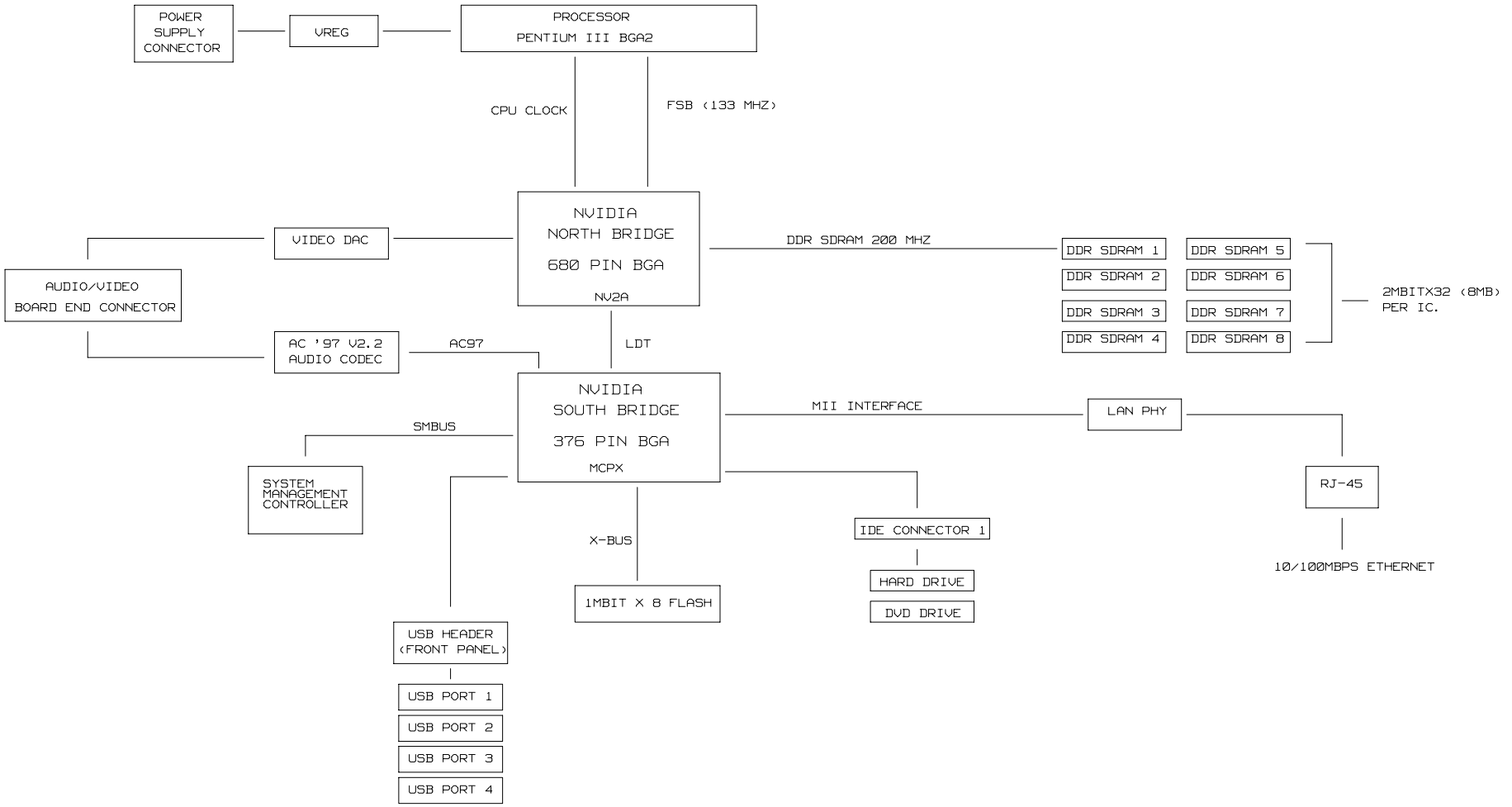
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

[PAGE_TITLE=COVER PAGE]

DRAWING
DVTFABK.SCH.1.1
Thu Aug 30 08:43:02 2001

BOM RELEASE DATE	xx/xx/xx	PB NUMBER A38727-009	
SIGNATURE	DATE	intel	3065 BOWERS AVE SANTA CLARA, CA 95051
DRN BY			
CHK BY xxxxxx	xx/xx/xx	TITLE SCH, PBA, DVT	
ENGR APVD			
APVD			
APVD			

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	1\55	9.0

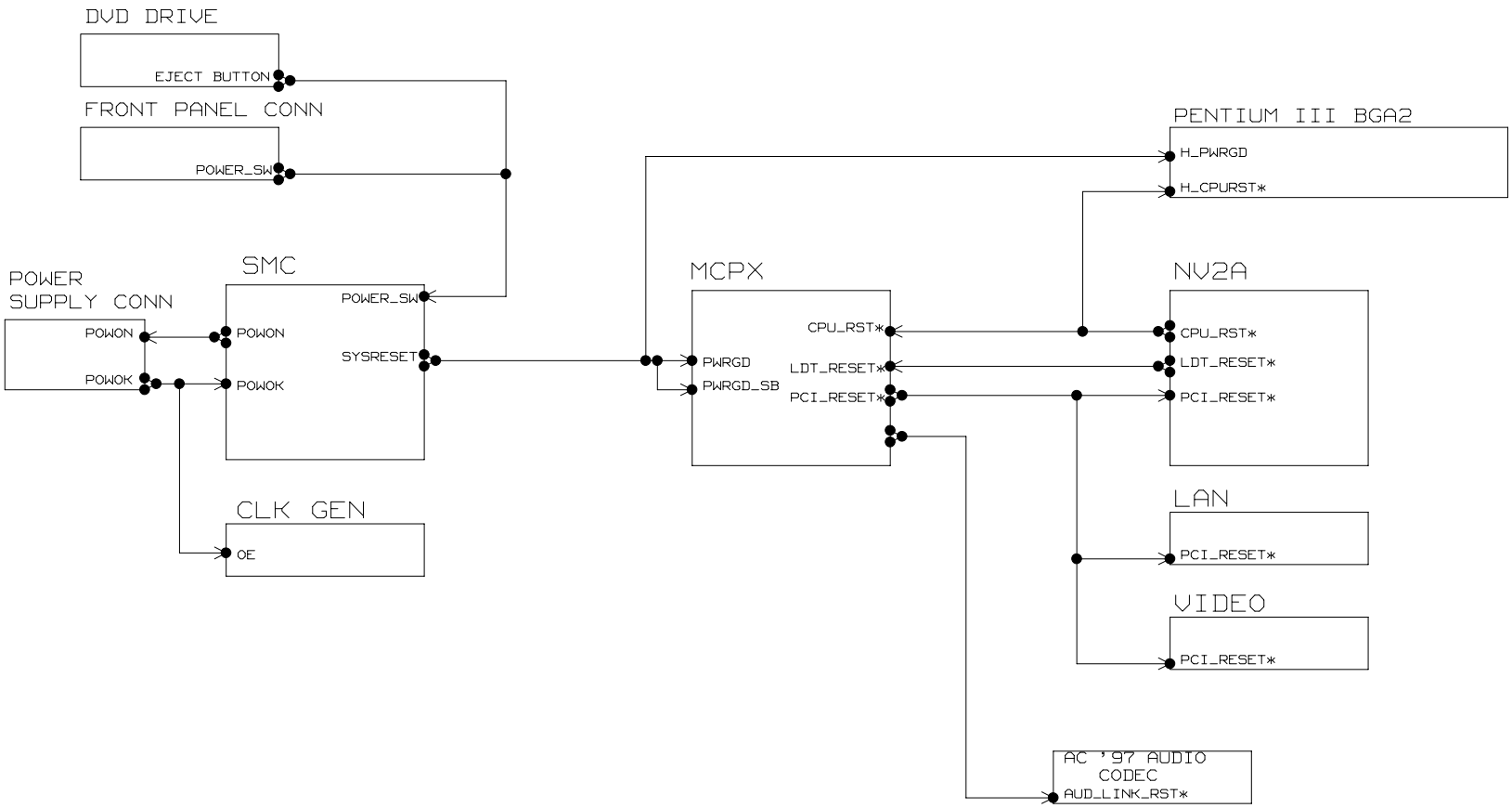


[PAGE_TITLE=BLOCK DIAGRAM]

DRAWING
DVTFABK.SCH.1.2
Thu Aug 30 08:40:17 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	2	9.0

RESET & POWER-ON MAP



[PAGE_TITLE=RESET MAP]

DRAWING
DVTFABK.SCH.1.3
Thu Aug 30 08:40:21 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	3	9.0

PCI DEVICE MAP

DEVICE	PCI BUS #	DEVICE #	FUNCTION	DEVICE ID	COMMENTS
NV2A					
HOST BRIDGE	00	00	00	02A8	IT IS DIFFERENT FUNCTIONALLY FROM CRUSH12
AGP BRIDGE	00	30	00	01B7	SECONDARY BRIDGE #=1 IN STD ENUMERATION
NV2A	02	00	00	02A0	
MCPX					
APU	00	05	00	01B0	
AUDIO CODEC	00	06	00	01B1	
USB1.1 OHCI A	00	02	00	01C2	
USB1.1 OHCI B	00	03	00	01C2	
MAC	00	04	00	01C3	
IDE	00	09	00	01BC	
SMBUS2	00	01	01	01B4	
SUBTRACTIVE	00	01	00	01B2	INCLUDES LEGACY AND LPC (BIOS)

GPIO USAGE TABLE

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
MCPX	GPIO0	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO1	OUT	VCC3	H	H	TESTPOINT (NOT USED)
MCPX	GPIO14	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO15	OUT	VCC3	Z	Z	FWENB
MCPX	GPIO16	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO19	OUT	VCC3	Z	Z	LVLCNT1
MCPX	GPIO20	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO21	IN	VCC3	H	H	SMI* INPUT FROM SMC
MCPX	GPIO22	OUT	VCC3	Z	Z	LVLCNT0
MCPX	GPIO24		VCC3	Z	Z	TESTPOINT (NOT USED)

SMBUS ADDRESS MAP

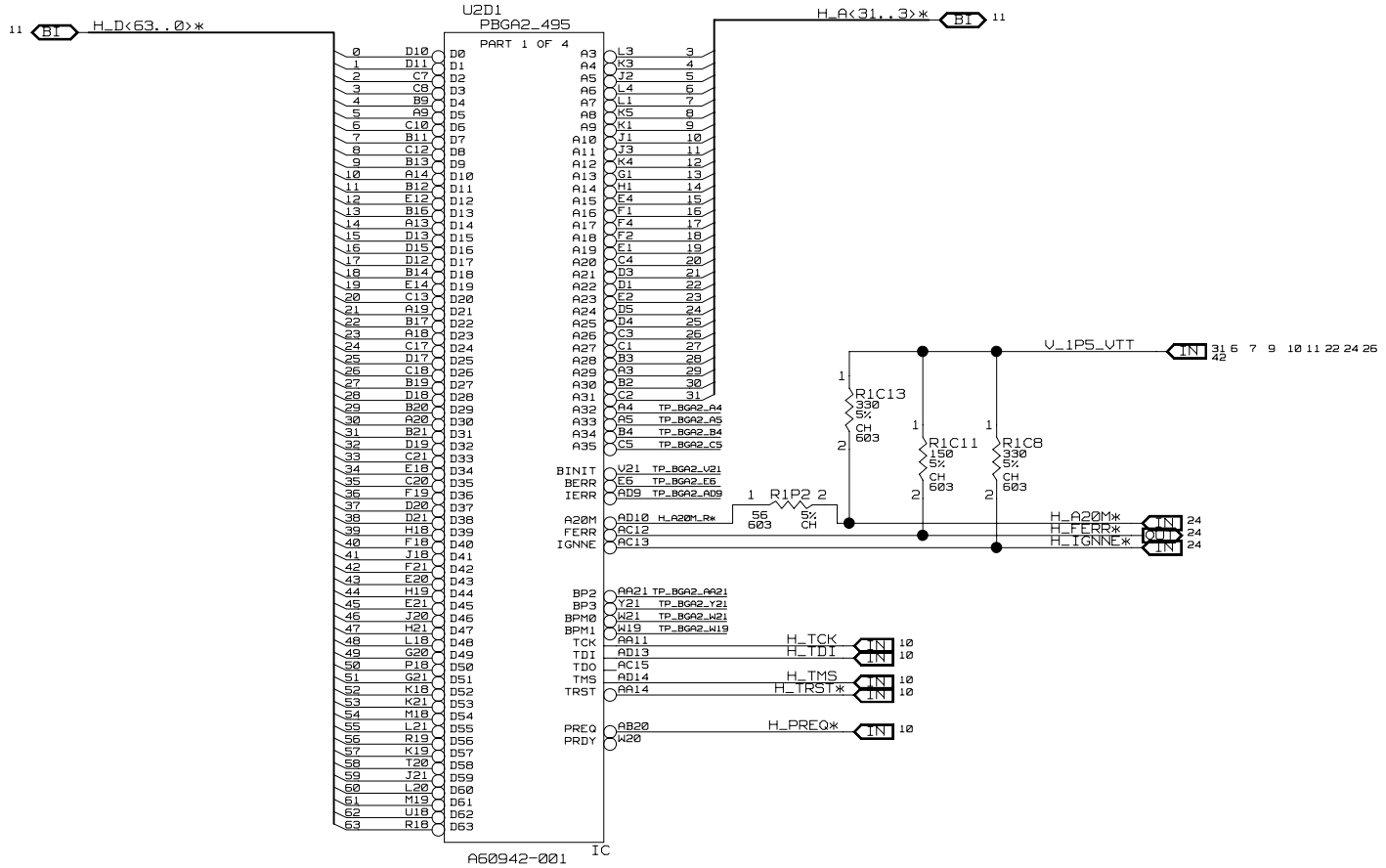
DEVICE	SMBUS #	ADDRESS	EVT	DVT	COMMENTS
CX25871	1	8A/8B		X	CONNECT ALTADDR (PIN 48) TO 3.3
CNR EEPROM	1	A8/A9	X	X	CONNECT CNR_SMB[2:0]=100 BINARY
MCP1 SMB1	1	10/11	X	X	SMBUS HOST (WRITE/READ)
SMC	1	20/21	X	X	(WRITE/READ)
TEMP(ADM1032)	1	98/99	X	X	(WRITE/READ)
DIMM0	0	A0/A1	X		M_A_CS[1..0]*
DIMM1	0	A2/A3	X		M_B_CS[1..0]*
DIMM2	0	A4/A5			M_B_CS[3..2]*
MCP1 SMB0	0	10/11	X		SMBUS HOST (WRITE/READ)

*NOTE: DEVICES ON SMBUS 0 DON'T EXIST ON DVT.

[PAGE_TITLE=GPIO/IDSEL TABLE]

DRAWING
DVTFABK.SCH.1.4
Thu Aug 30 08:40:24 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	4	9.0



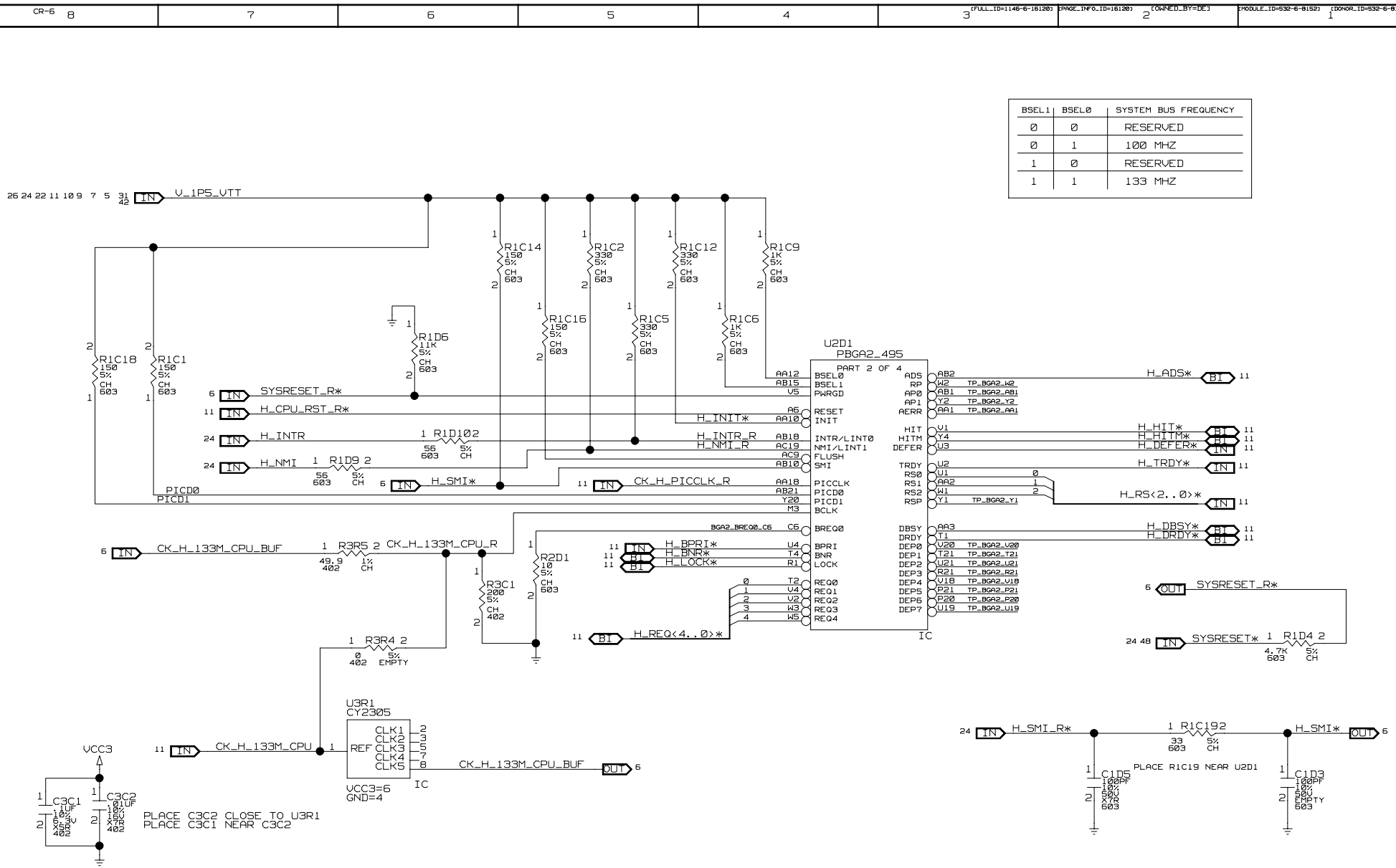
NC: A15, A16, A17, C14, D8, D14, D16, E15, G2, G5, G18, H3, H5, J5, M4, M5, P3, P4, AA5, AA19, AC3, AC20, AD15

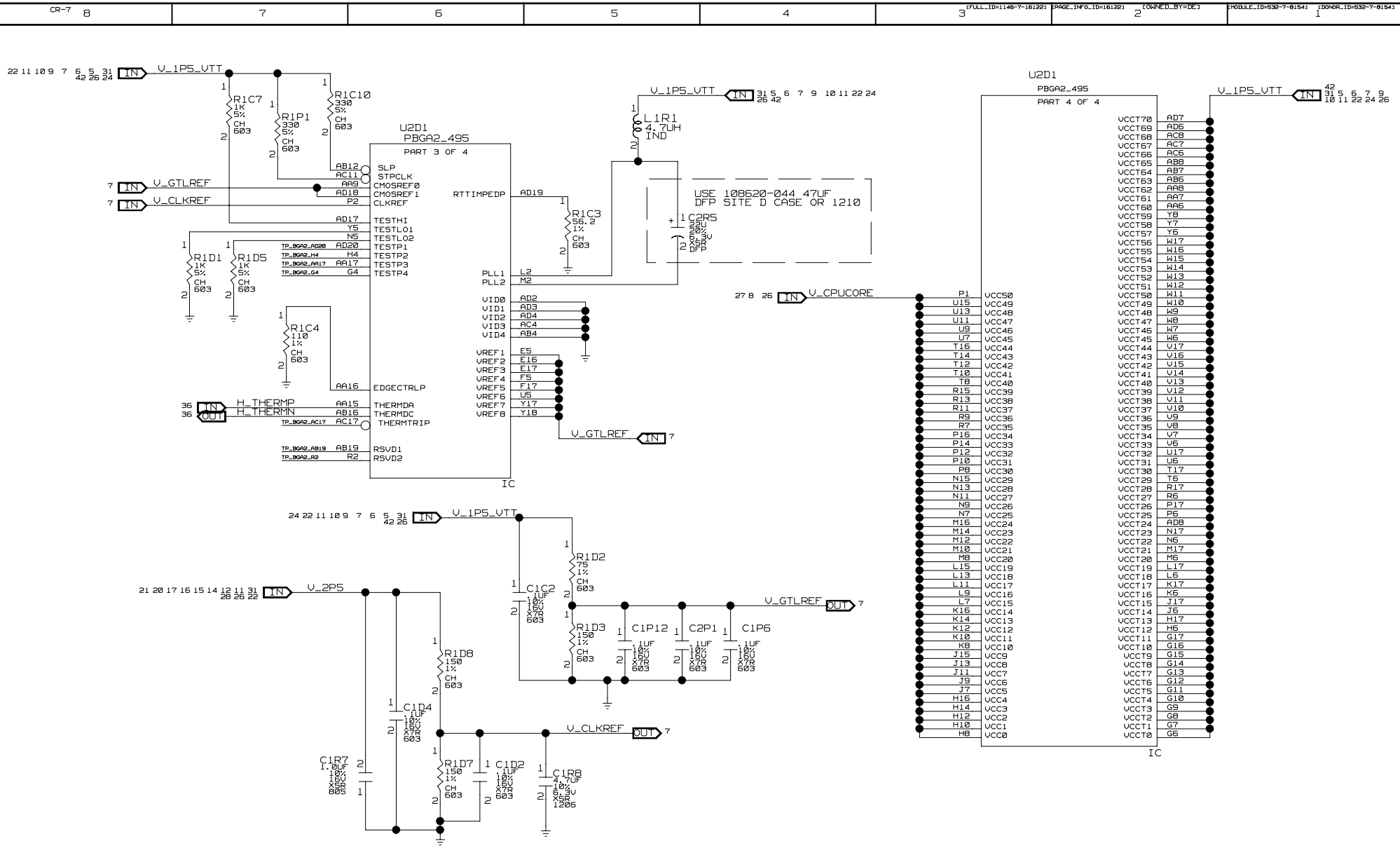
GND: A2, A7, A8, A12, A21, B1, B5, B6, B7, B8, B10, B15, B18, C9, C11, C15, C16, C19, D2, D6, D7, D9, E3, E7, E8, E9
GND: E10, E11, E13, E19, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F20, G3, G19, H2, H7, H9, H11, H13, H15
GND: H20, J4, J8, J10, J12, J14, J16, J19, K2, K7, K9, K11, K13, K15, K20, L5, L8, L10, L12, L14, L16, L19, M7, M9, M11
GND: M13, M15, M20, N2, N3, N4, N8, N10, N12, N14, N16, N18, N19, N20, P5, P7, P9, P11, P13, P15, P19, R3, R4, R5, R8, R10, R12, R14, R16, R20
GND: T3, T5, T7, T9, T11, T13, T15, T18, T19, U8, U10, U12, U14, U16, U20, V3, V19, W4, W18, Y3, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y19
GND: AA4, AA13, AA20, AB3, AB5, AB9, AB11, AB13, AB14, AB17, AC1, AC2, AC5, AC10, AC14, AC16, AC21, AD1, AD5, AD16, AD21, AC18

[PAGE_TITLE=PENTIUM III BGA2 PART 1 OF 4]

DRAWING
DVTFABK.SCH.1.5
Thu Aug 30 08:40:27 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	5	9.0


BSEL1 BSEL0 SYSTEM BUS FREQUENCY
0 0 RESERVED
0 1 100 MHZ
1 0 RESERVED
1 1 133 MHZ
V_1P5_VTT
R1C14 150 5% CH 603
R1C2 330 5% CH 603
R1C12 330 5% CH 603
R1C9 1K 5% CH 603
R1C16 150 5% CH 603
R1C5 330 5% CH 603
R1C6 1K 5% CH 603
R1C18 150 5% CH 603
R1C1 150 5% CH 603
R1D6 11K 5% CH 603
U2D1
PBGA2_495
PART 2 OF 4
SYSRESET_R*
H_CPU_RST_R*
H_INTR
H_NMI
H_SMI*
H_INIT*
H_INTR_R
H_NMI_R
PICD0
PICD1
CK_H_PICCLK_R
H_ADS*
H_HIT*
H_HITM*
H_DEFER*
H_TRDY*
H_RS<2..0>*
H_DBSY*
H_DRDY*
H_BPRI*
H_BNR*
H_LOCK*
H_REQ<4..0>*
IC
CK_H_133M_CPU_BUF
R3R5 49.9 402 1% CH
CK_H_133M_CPU_R
R2D1 10 5% CH 603
R3C1 200 5% CH 402
R3R4 0 402 EMPTY
SYSRESET_R*
SYSRESET*
R1D4 4.7K 603 5% CH
U3R1
CY2305
CK_H_133M_CPU
CK_H_133M_CPU_BUF
VCC3
C3C1 .1UF 10% 6.3V X5R 402
C3C2 .01UF 10% 16V X7R 402
PLACE C3C2 CLOSE TO U3R1
PLACE C3C1 NEAR C3C2
VCC3=6
GND=4
H_SMI_R*
R1C192 33 603 5% CH
H_SMI*
PLACE R1C19 NEAR U2D1
C1D5 100PF 10% 50V X7R 603
C1D3 100PF 10% 50V X7R 603
[PAGE_TITLE=PENTIUM III BGA2 PART 2 OF 4]
DRAWING
DVTFABK.SCH.1.6
Thu Aug 30 08:40:30 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER A72507
PAGE 6
REV 9.0



[PAGE_TITLE=PENTIUM III BGA2 PARTS 3 & 4]

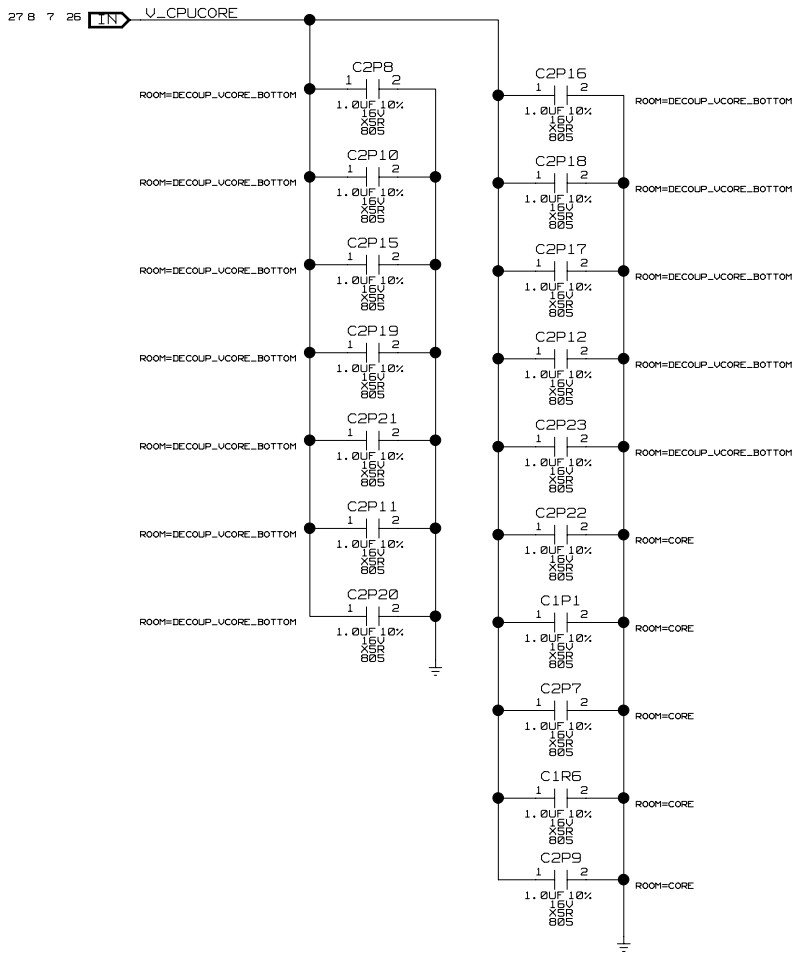
DRAWING
DVTFABK.SCH.1.7
Thu Aug 30 08:40:33 2001

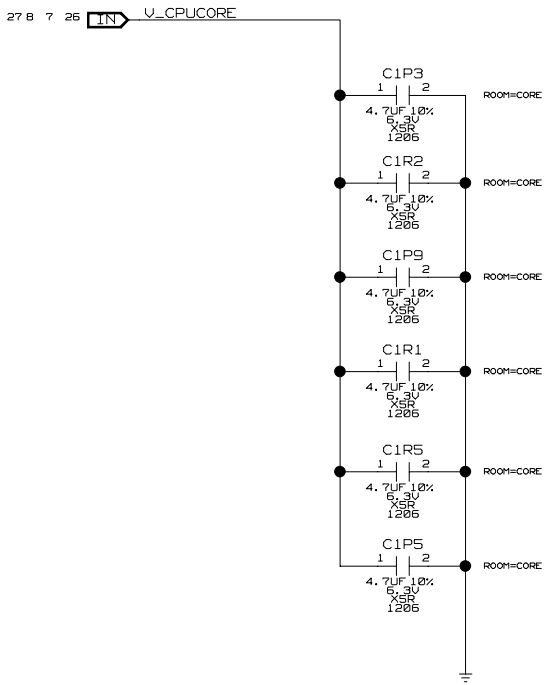
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	7	9.0

[DONOR_REV=1.0/page7]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page7]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:13:40 PM]

[FULL_ID=1146-8-16124] [PAGE_INFO_ID=16124] [OWNED_BY=DE] [MODULE_ID=356-38-5676] [DONOR_ID=532-8-8156]

CPU VCORE DECOUPLING



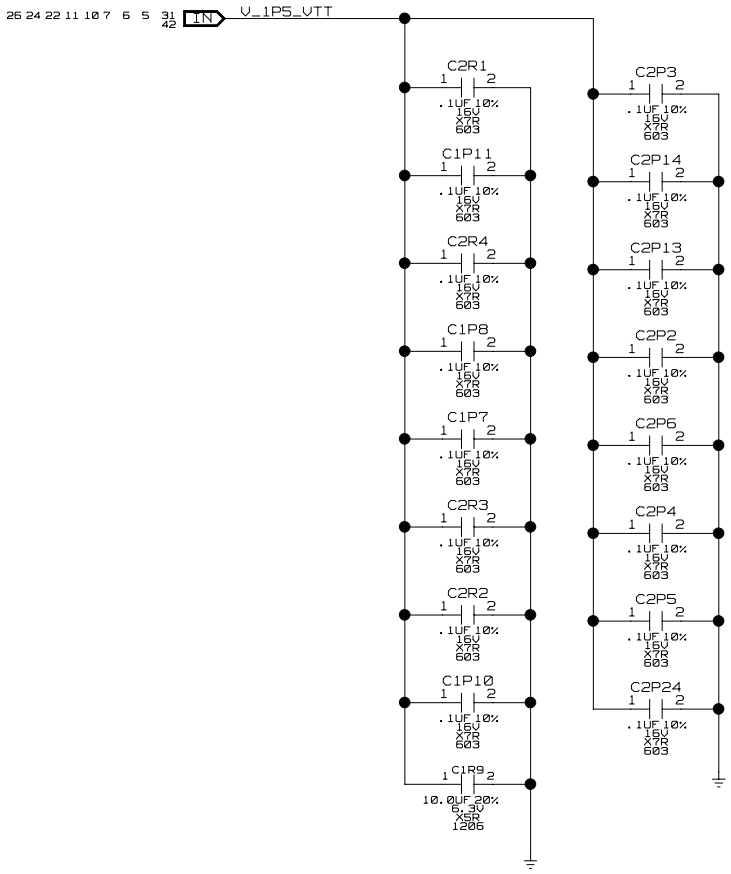


[PAGE_TITLE=CPU VCORE DECOUPLING]

DRAWING
DVTFABK.SCH.1.8
Thu Aug 30 08:40:36 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	8	9.0

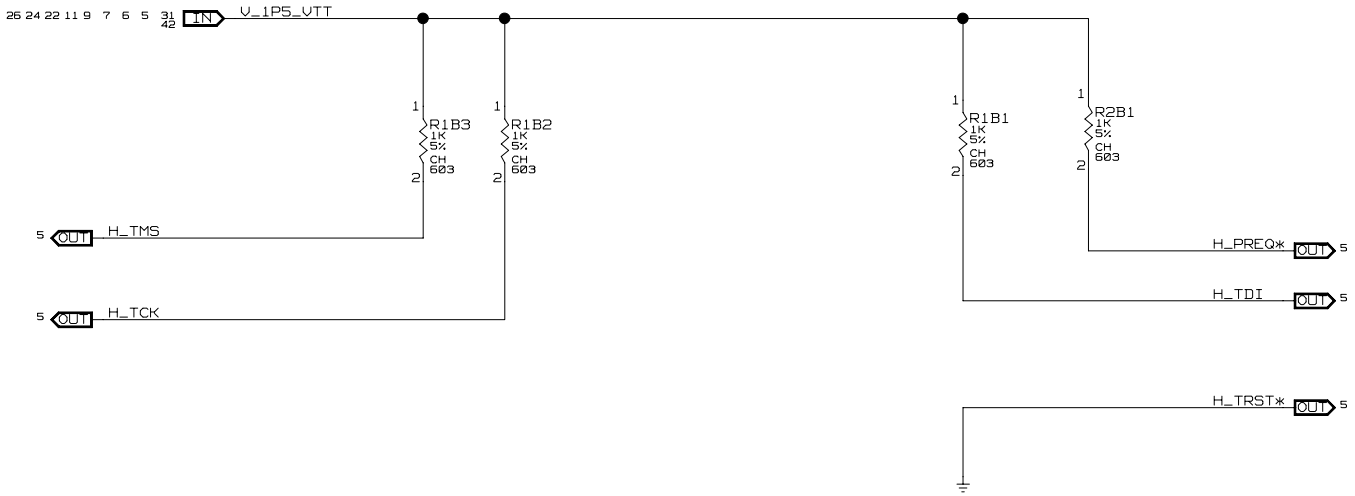
CPU VTT DECOUPLING



[PAGE_TITLE=CPU VTT DECOUPLING]

DRAWING
DVTFABK.SCH.1.9
Thu Aug 30 08:40:39 2001

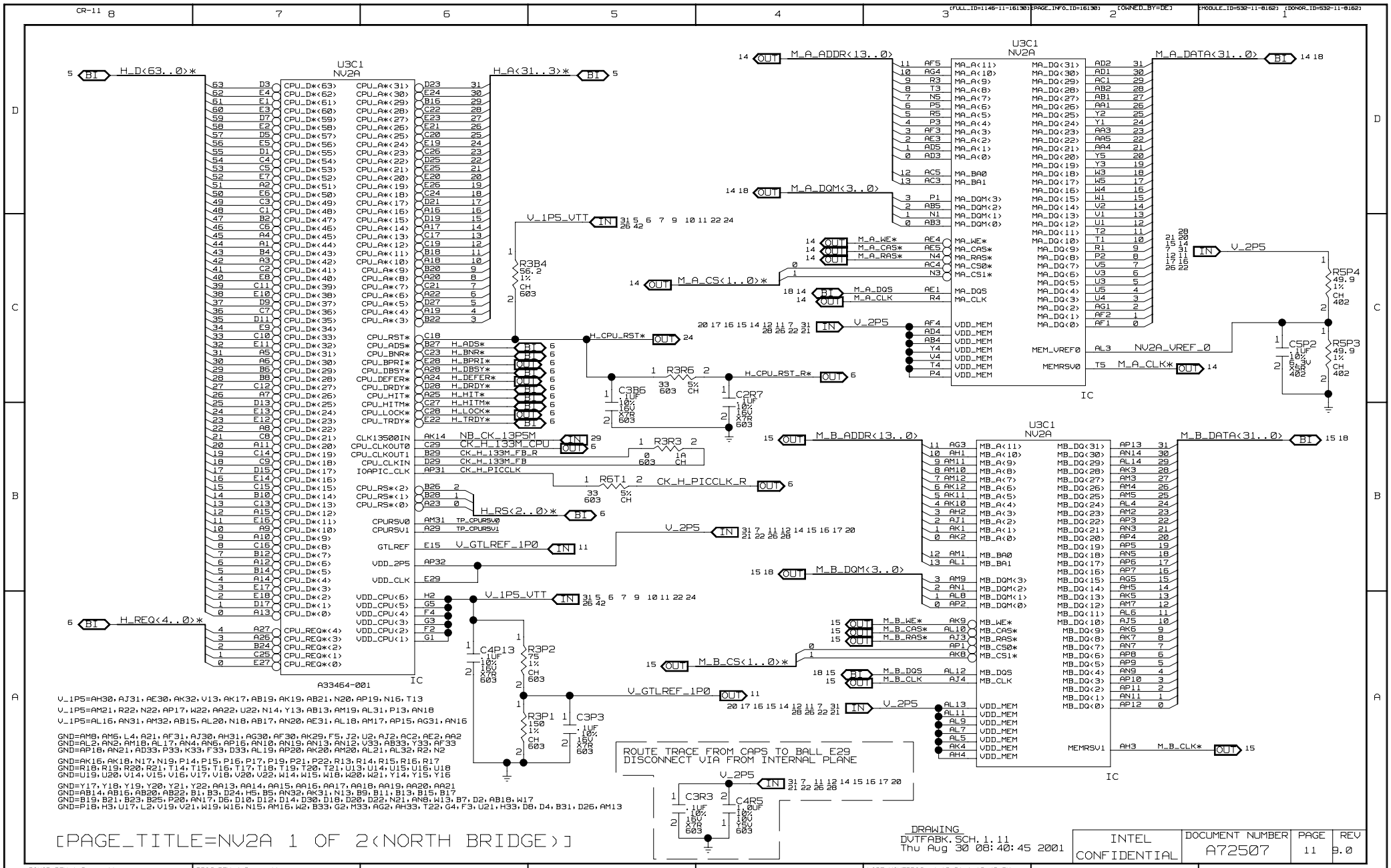
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	9	9.0

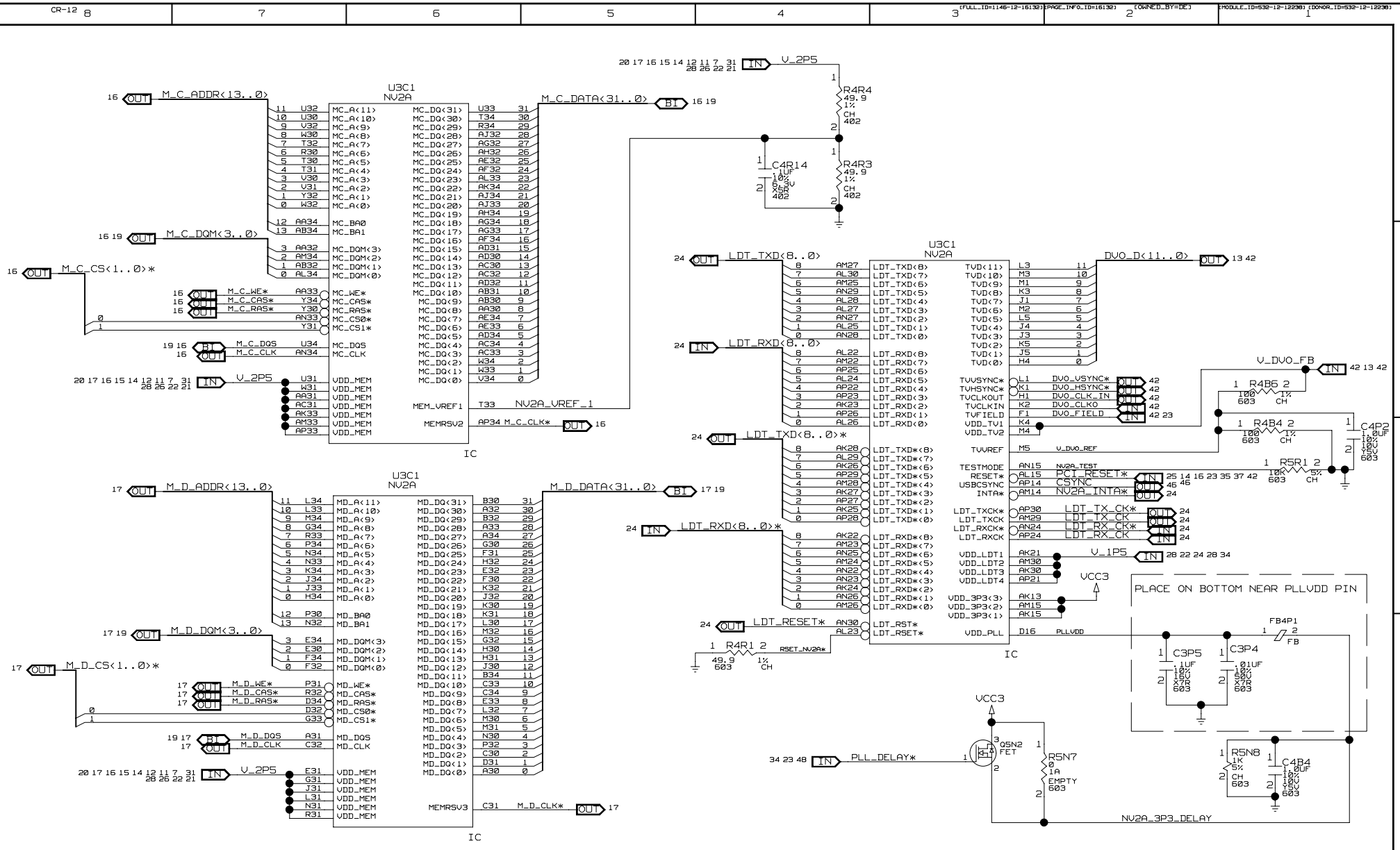


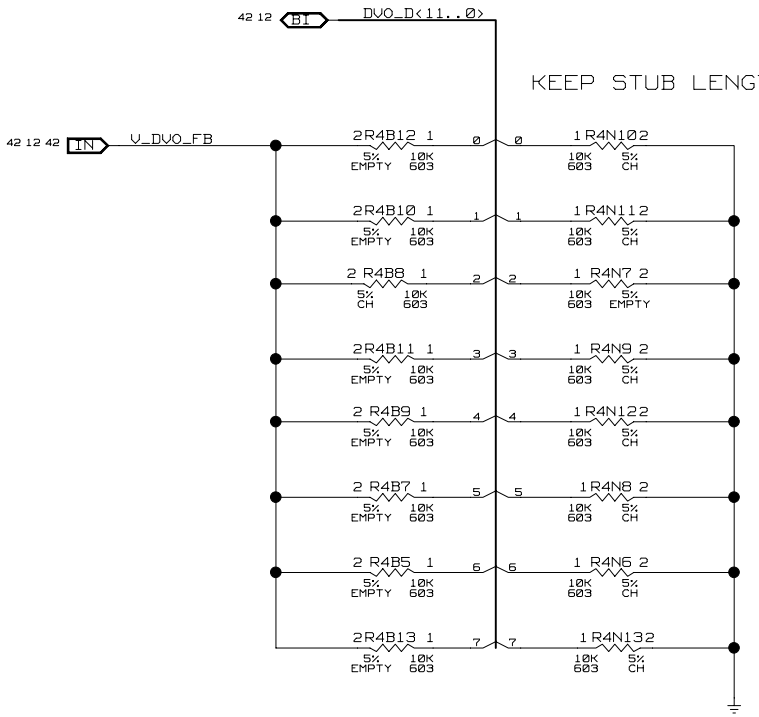
[PAGE_TITLE=ITP TERMINATION]

DRAWING
DVTFABK.SCH.1.10
Thu Aug 30 08:40:42 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	10	9.0


U3C1
NV2A
H_D<63..0>*
H_A<31..3>*
M_A_ADDR<13..0>
M_A_DATA<31..0>
M_A_DQM<3..0>
M_A_CS<1..0>*
M_A_WE*
M_A_CAS*
M_A_RAS*
M_A_DQS
M_A_CLK
V_1P5_VTT
V_2P5
H_CPU_RST*
H_CPU_RST_R*
NB_CK_13P5M
CK_H_133M_CPU
CK_H_133M_FB_R
CK_H_133M_FB
CK_H_PICCLK
CK_H_PICCLK_R
H_RS<2..0>*
V_GTLREF_1P0
NV2A_VREF_0
M_A_CLK*
M_B_ADDR<13..0>
M_B_DATA<31..0>
M_B_DQM<3..0>
M_B_CS<1..0>*
M_B_WE*
M_B_CAS*
M_B_RAS*
M_B_DQS
M_B_CLK
H_REQ<4..0>*
R3B4 56.2 1% CH 603
R3R6 33 5% CH
R3R3 0 1A CH
R6T1 33 5% CH
R5P4 49.9 1% CH 402
R5P3 49.9 1% CH 402
C3B6 .1UF 10% 16V X7R 603
C2R7 .1UF 10% 16V X7R 603
C5P2 .1UF 10% 16V X5R 402
C4P13 .1UF 10% 16V X7R 603
R3P2 75 1% CH 603
R3P1 150 1% CH 603
C3P3 .1UF 10% 16V X7R 603
C3R3 .1UF 10% 16V X7R 603
C4R5 1.0UF 10% 10V X5R 603
ROUTE TRACE FROM CAPS TO BALL E29
DISCONNECT VIA FROM INTERNAL PLANE
A33464-001
IC
V_1P5=AH30,AJ31,AE30,AK32,V13,AK17,AB19,AK19,AB21,N20,AP19,N16,T13
V_1P5=AM21,R22,N22,AP17,W22,AA22,U22,N14,Y13,AB13,AM19,AL31,P13,AN18
V_1P5=AL16,AN31,AM32,AB15,AL20,N18,AB17,AN20,AE31,AL18,AM17,AP15,AG31,AN16
GND=AM8,AM6,L4,A21,AF31,AJ30,AH31,AG30,AF30,AK29,F5,J2,U2,AJ2,AC2,AE2,AA2
GND=AL2,AN2,AM18,AL17,AN4,AN6,AP16,AN10,AN19,AN13,AN12,V33,AB33,Y33,AF33
GND=AP18,AN21,AD33,P33,K33,F33,D33,AL19,AP20,AK20,AM20,AL21,AL32,R2,N2
GND=AK16,AK18,N17,N19,P14,P15,P16,P17,P19,P21,P22,R13,R14,R15,R16,R17
GND=R18,R19,R20,R21,T14,T15,T16,T17,T18,T19,T20,T21,U13,U14,U15,U16,U18
GND=U19,U20,V14,V15,V16,V17,V18,V20,V22,W14,W15,W18,W20,W21,Y14,Y15,Y16
GND=Y17,Y18,Y19,Y20,Y21,Y22,AA13,AA14,AA15,AA16,AA17,AA18,AA19,AA20,AA21
GND=AB14,AB16,AB20,AB22,B1,B3,D24,H5,B5,AN32,AK31,N13,B9,B11,B13,B15,B17
GND=B19,B21,B23,B25,P20,AN17,D6,D10,D12,D14,D30,D18,D20,D22,N21,AN8,W13,B7,D2,AB18,W17
GND=P18,H3,U17,L2,V19,V21,W19,W16,N15,AM16,W2,B33,G2,M33,AG2,AH33,T22,G4,F3,U21,H33,D8,D4,B31,D26,AM13
[PAGE_TITLE=NV2A 1 OF 2(NORTH BRIDGE)]
DRAWING
DVTFABK.SCH.1.11
Thu Aug 30 08:40:45 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER A72507
PAGE 11
REV 9.0


U3C1
NV2A
M_C_ADDR<13..0>
M_C_DATA<31..0>
M_C_DQM<3..0>
M_C_CS<1..0>*
M_C_WE*
M_C_CAS*
M_C_RAS*
M_C_DQS
M_C_CLK
V_2P5
MEM_VREF1
NV2A_VREF_1
MEMRSV2
M_C_CLK*
R4R4 49.9 1% CH 402
R4R3 49.9 1% CH 402
C4R14 .1UF 10% 6.3V X5R 402
IC
U3C1
NV2A
M_D_ADDR<13..0>
M_D_DATA<31..0>
M_D_DQM<3..0>
M_D_CS<1..0>*
M_D_WE*
M_D_CAS*
M_D_RAS*
M_D_DQS
M_D_CLK
V_2P5
MEMRSV3
M_D_CLK*
IC
U3C1
NV2A
LDT_TXD<8..0>
LDT_RXD<8..0>
LDT_TXD<8..0>*
LDT_RXD<8..0>*
LDT_RESET*
RSET_NV2A*
R4R1 2 49.9 1% 603 CH
DVO_D<11..0>
DVO_VSYNC*
DVO_HSYNC*
DVO_CLK_IN
DVO_CLKO
DVO_FIELD
V_DVO_FB
R4B6 2 100 1% 603 CH
R4B4 2 100 1% 603 CH
C4P2 1.0UF 10% 10V X5V 603
V_DVO_REF
R5R1 2 10K 5% 603 CH
PCI_RESET*
CSYNC
NV2A_INTA*
LDT_TX_CK*
LDT_TX_CK
LDT_RX_CK*
LDT_RX_CK
V_1P5
VCC3
PLACE ON BOTTOM NEAR PLLVDD PIN
FB4P1 FB
C3P5 .1UF 10% 10V X7R 603
C3P4 .01UF 10% 50V X7R 603
R5N8 1K 5% CH 603
C4B4 1.0UF 10% 10V 603
Q5N2 FET
R5N7 0 1A EMPTY 603
PLL_DELAY*
NV2A_3P3_DELAY
IC
[PAGE_TITLE=NV2A 2 OF 2(NORTH BRIDGE)]
DRAWING
DVTFABK.SCH.1.12
Thu Aug 30 08:40:49 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER A72507
PAGE 12
REV 9.0



TVD		DEFINITION
[7]	0*	ENABLE INTERNAL LDT TERMINATION
	1	DISABLE INTERNAL LDT TERMINATION
[6]	0*	13.5MHZ OR 16.6MHZ
	1	14.31818MHZ
[5:4]	00*	USE FSB FREQUENCY BASED ON TVD[3:2]
	01	USE INTERNAL PROGRAMMED VALUE A
	10	USE INTERNAL PROGRAMMED VALUE B
	11	FORCE 66MHZ
[3:2]	00	NA
	01*	FSB FREQ=133MHZ FOR 16.6MHZ INPUT CLK
	10	NA
	11	NA
[1:0]	00*	EMRS MICRON MATCHED MODE
	01	EMRS [6,1]=[0,1], HALF OF NORMAL DRIVE MODE
	10	RESERVED
	11	EMRS MATCHED 30% DRIVE MODE(SAMSUNG)

* = CURRENT SETTING

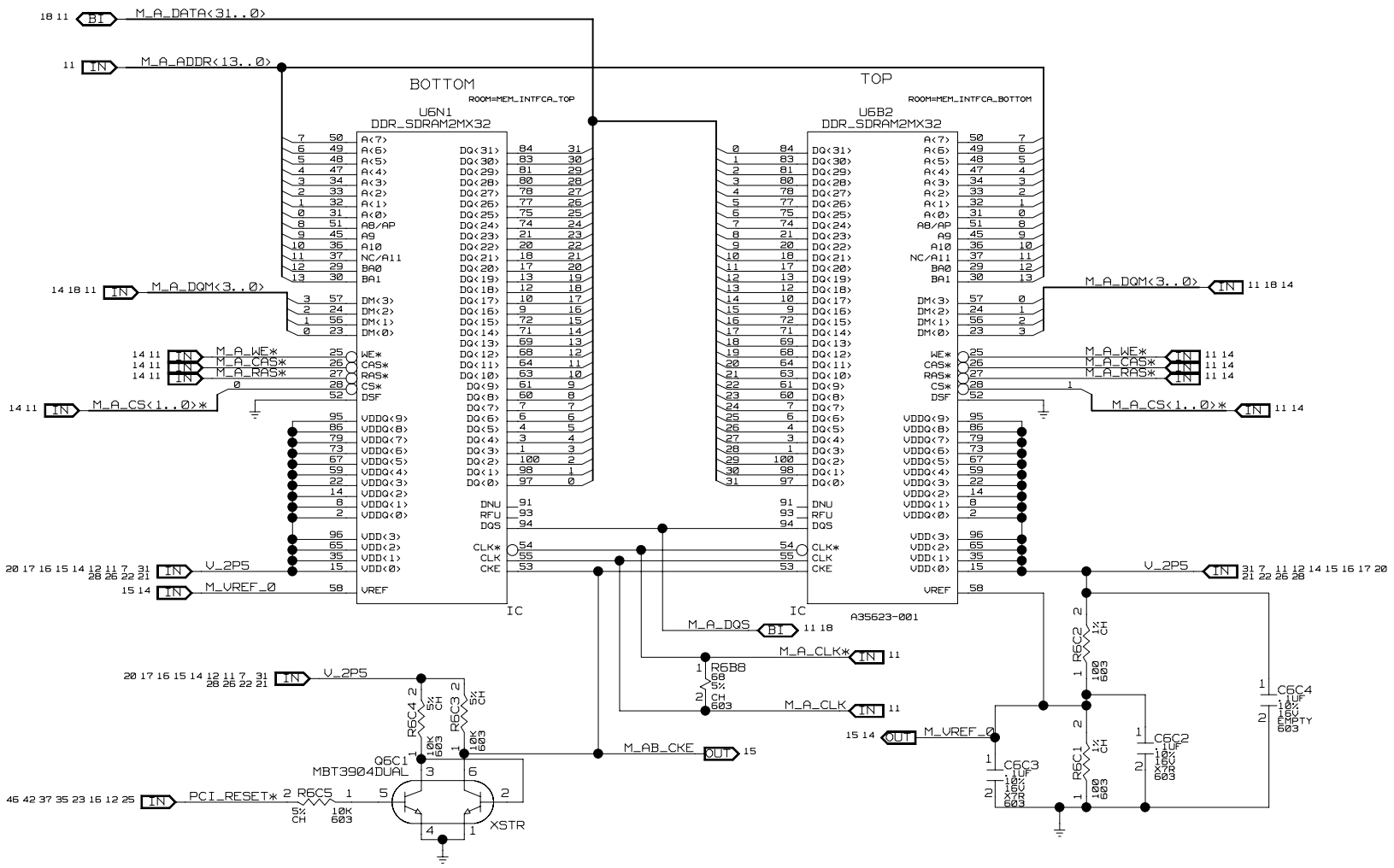
FOR SAMSUNG DDR:
EMPTY R4N10 AND R4N11
STUFF R4B12 AND R4B10

[PAGE_TITLE=NV2A STRAPPING]

DRAWING
DVTFABK.SCH.1.13
Thu Aug 30 08:40:52 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	13	9.0

MEMORY INTERFACE PARTITION A

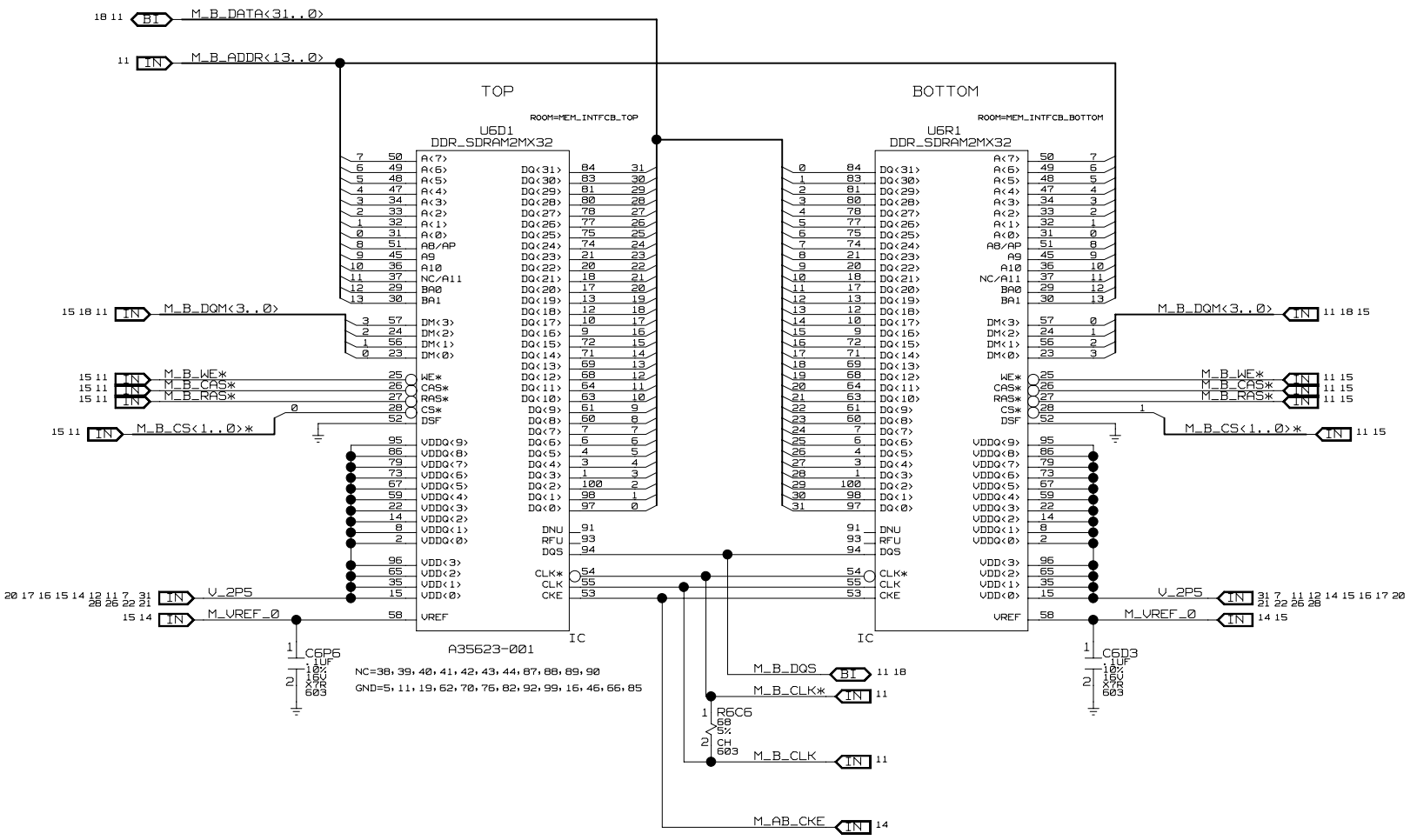


[PAGE_TITLE=DDR SDRAM (PARTITION A)]

DRAWING
DVTFABK.SCH.1.14
Thu Aug 30 08:40:55 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	14	9.0

MEMORY INTERFACE PARTITION B

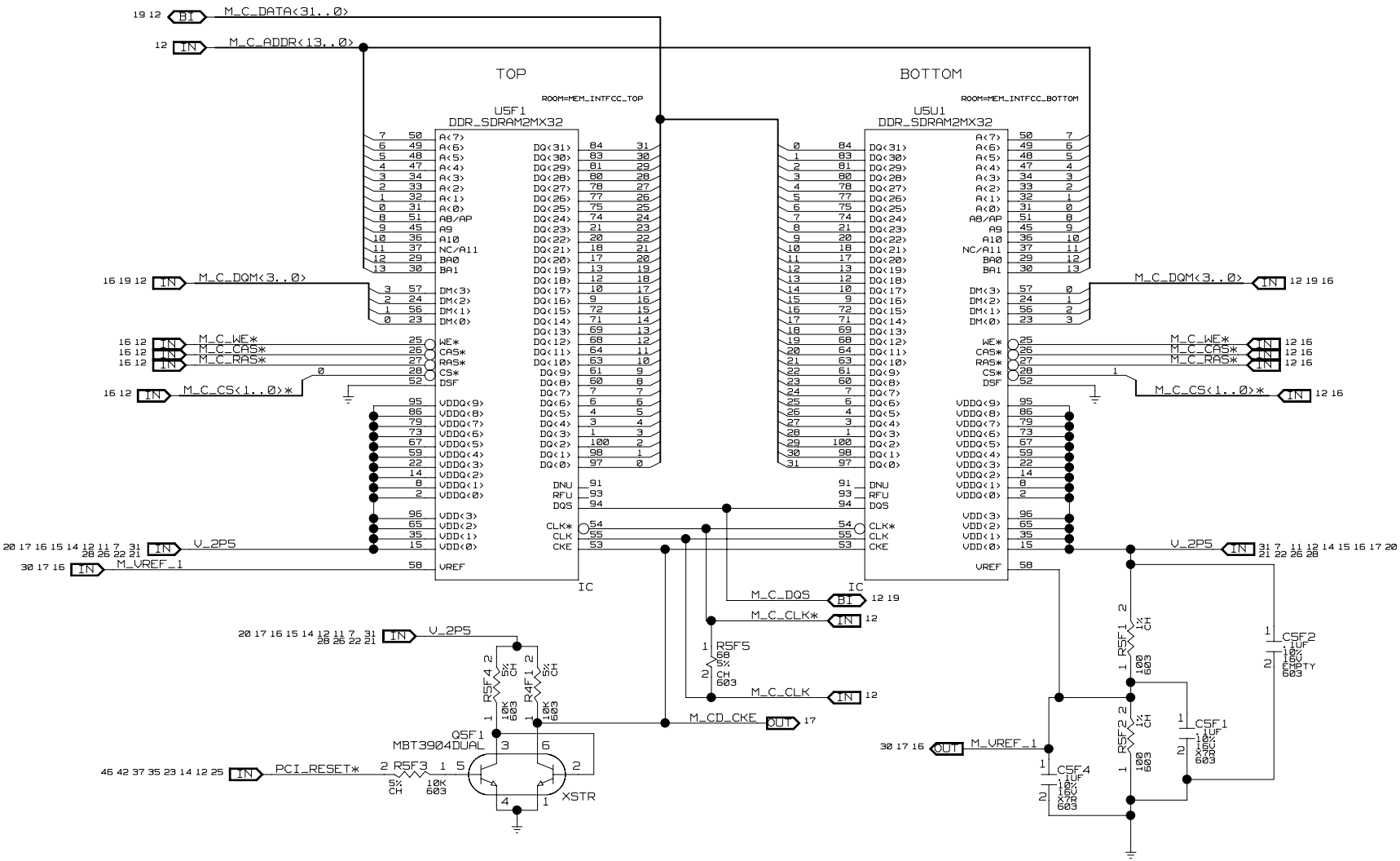


[PAGE_TITLE=DDR SDRAM (PARTITION B)]

DRAWING
DVTFABK.SCH.1.15
Thu Aug 30 08:40:58 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	15	9.0

MEMORY INTERFACE PARTITION C

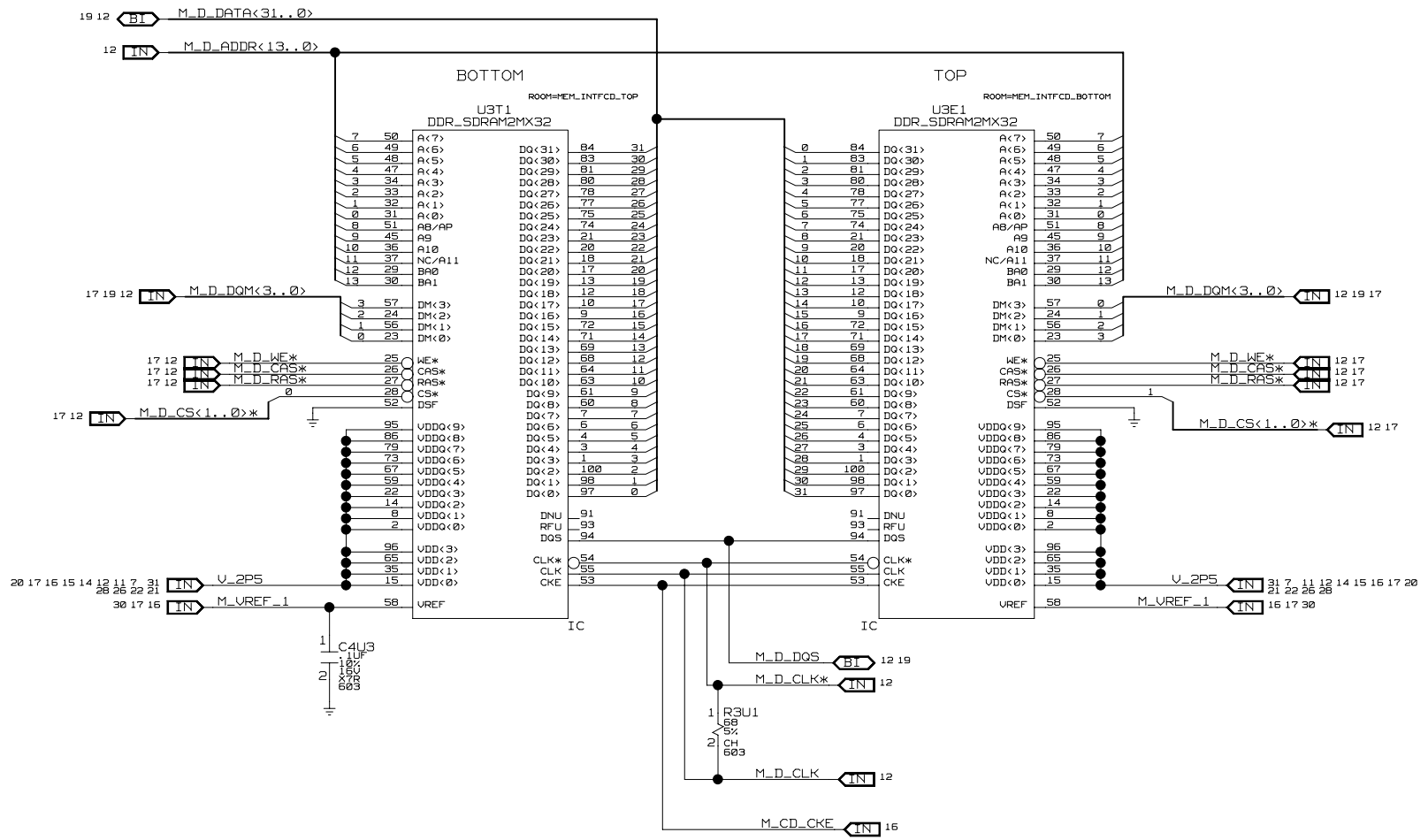


[PAGE_TITLE=DDR SDRAM (PARTITION C)]

DRAWING
DVTFABK.SCH.1.16
Thu Aug 30 08:41:01 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	16	9.0

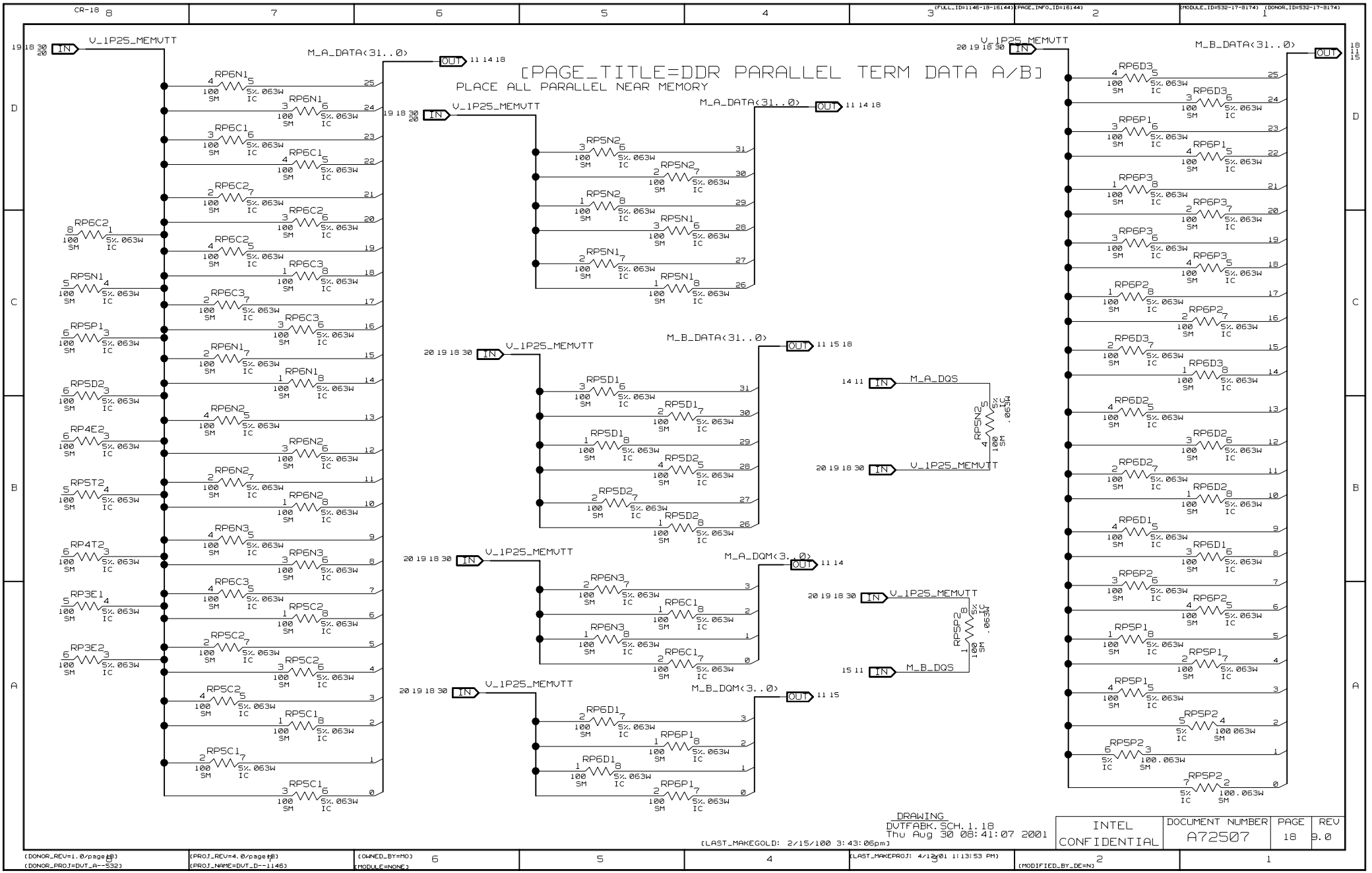
MEMORY INTERFACE PARTITION D



[PAGE_TITLE=DDR SDRAM (PARTITION D)]

DRAWING
DVTFABK.SCH.1.17
Thu Aug 30 08:41:04 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	17	9.0



DRAWING
DVTFABK.SCH.1.18
Thu Aug 30 08:41:07 2001

[LAST_MAKEGOLD: 2/15/100 3:43:06pm]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	18	3.0

[DONOR_REV=1.0/page#0]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page#0]
[PROJ_NAME=DVT_D--1146]
[OWNED_BY=MO]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:13:53 PM]
[MODIFIED_BY_DE=N]
[FULL_ID=1146-18-16144]
[PAGE_INFO_ID=16144]
[MODULE_ID=532-17-8174]
[DONOR_ID=532-17-8174]
CR-18

[PAGE_TITLE=DDR PARALLEL TERM DATA C/D]

PLACE ALL PARALLEL NEAR MEMORY

V_1P25_MEMVTT

M_C_DATA<31..0>

M_D_DATA<31..0>

M_C_DQM<3..0>

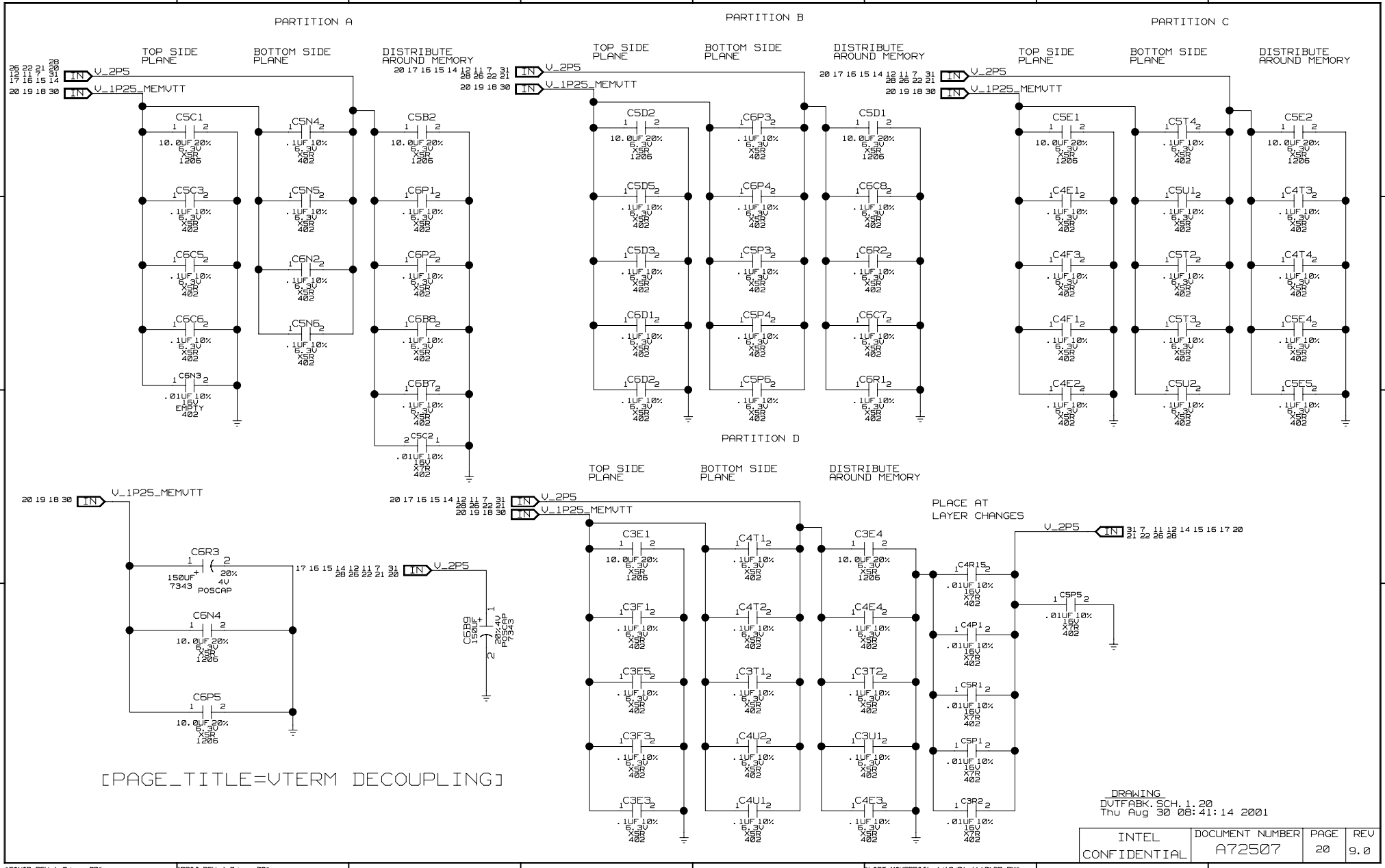
M_D_DQM<3..0>

M_C_DQS

M_D_DQS

DRAWING
DVTFABK.SCH.1.19
Thu Aug 30 08:41:10 2001

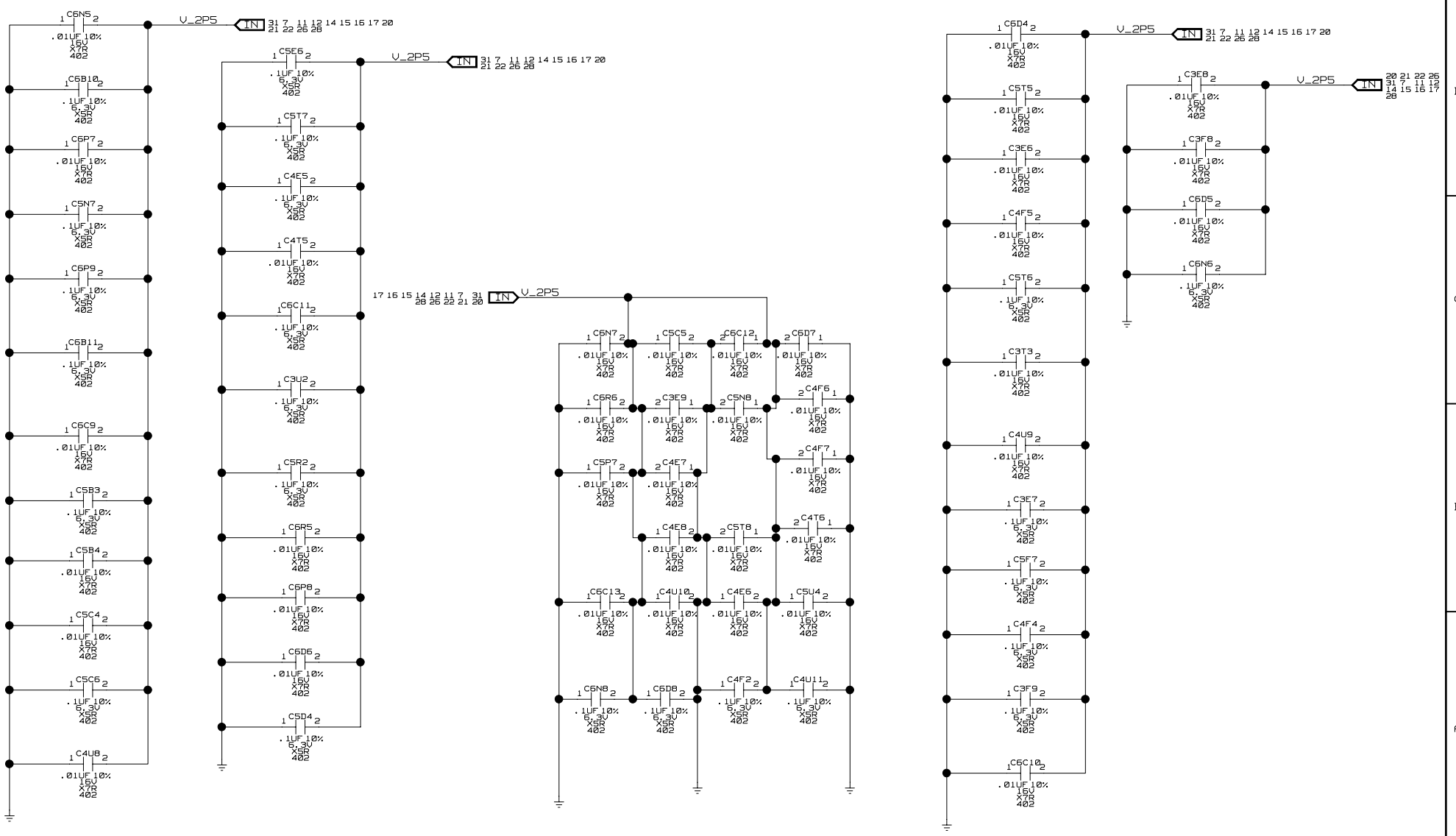
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	19	9.0



[PAGE_TITLE=VTERM DECOUPLING]

DRAWING
DVTFABK.SCH.1.20
Thu Aug 30 08:41:14 2001

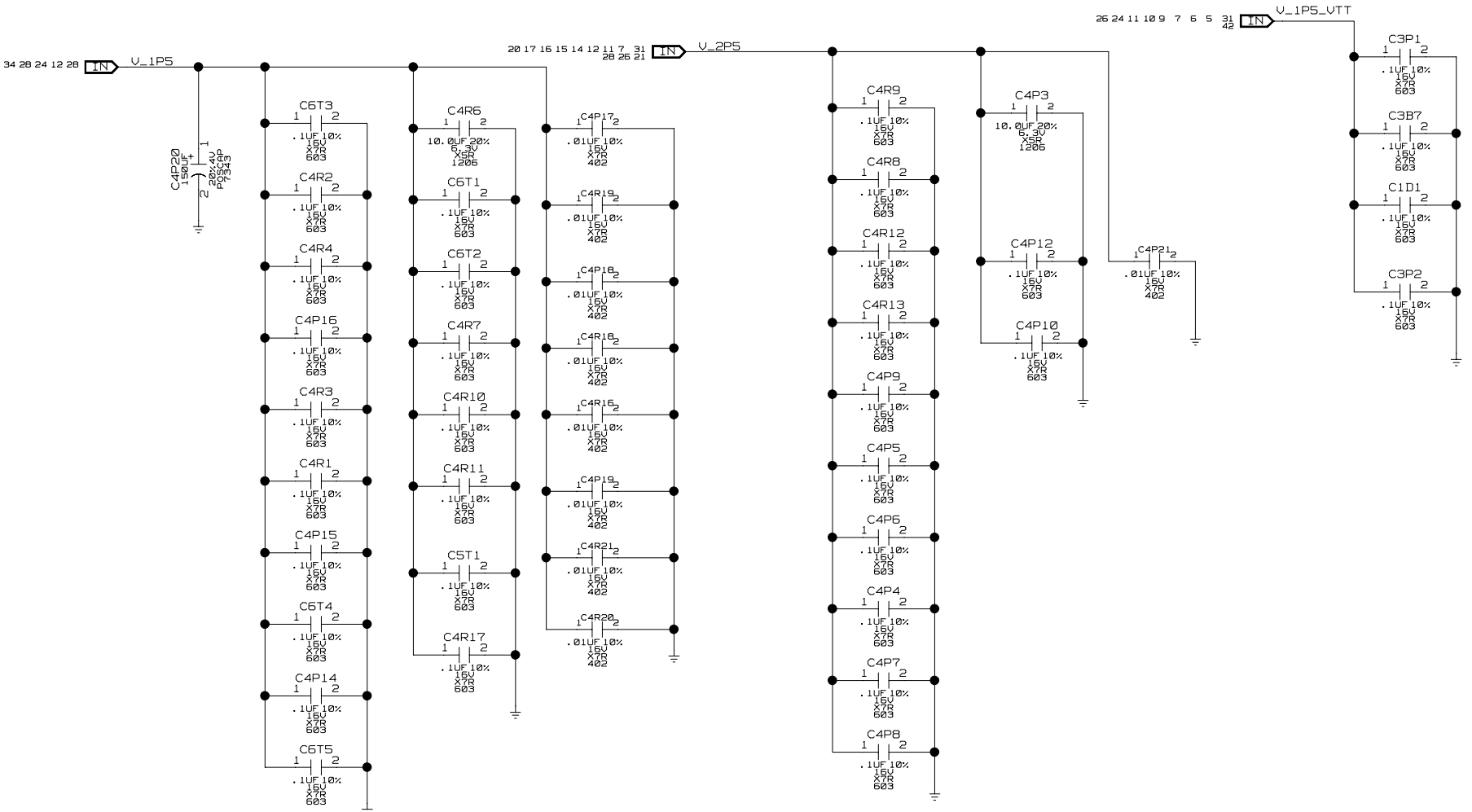
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	20	9.0



[PAGE_TITLE=MEMORY DECOUPLING]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	21	9.0

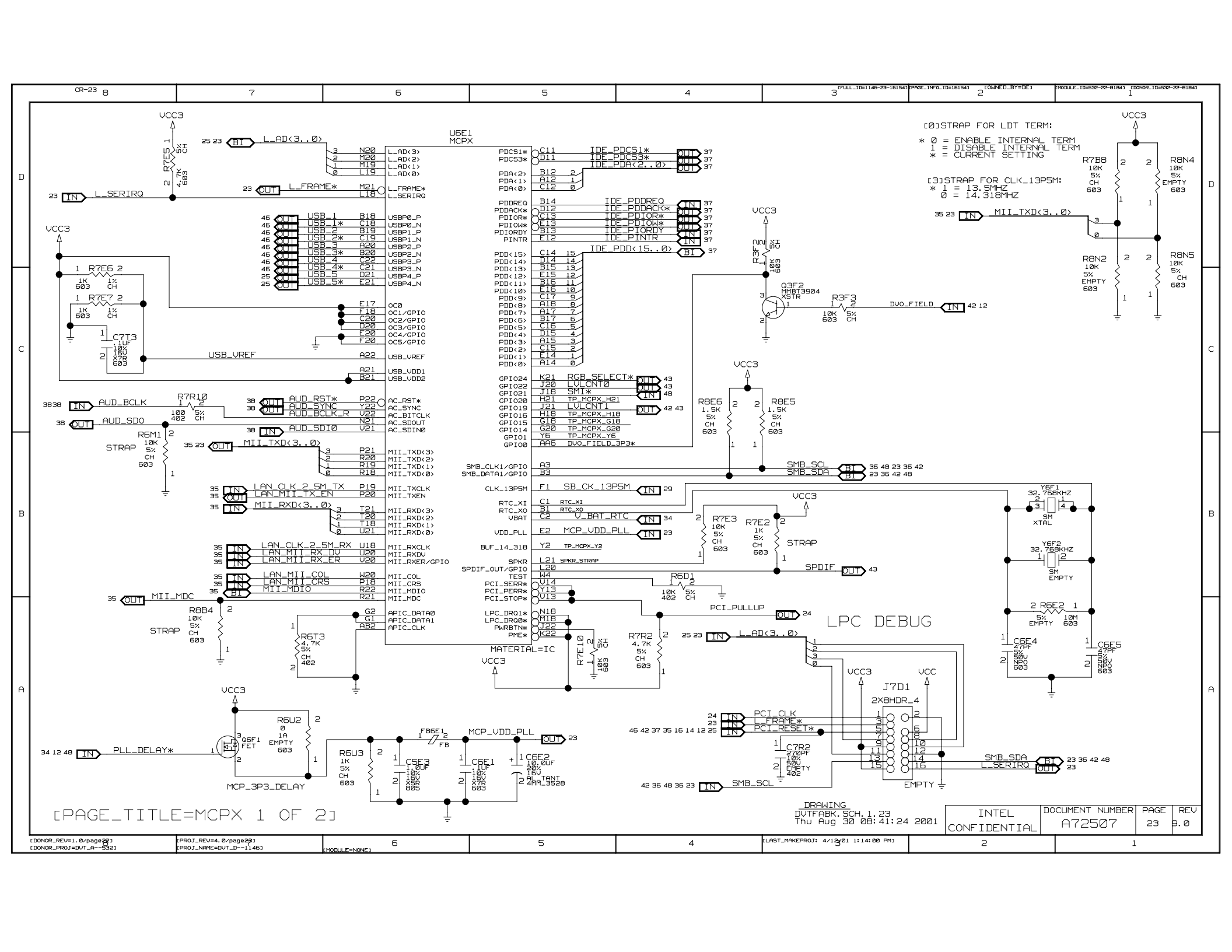
NV2A DECOUPLING

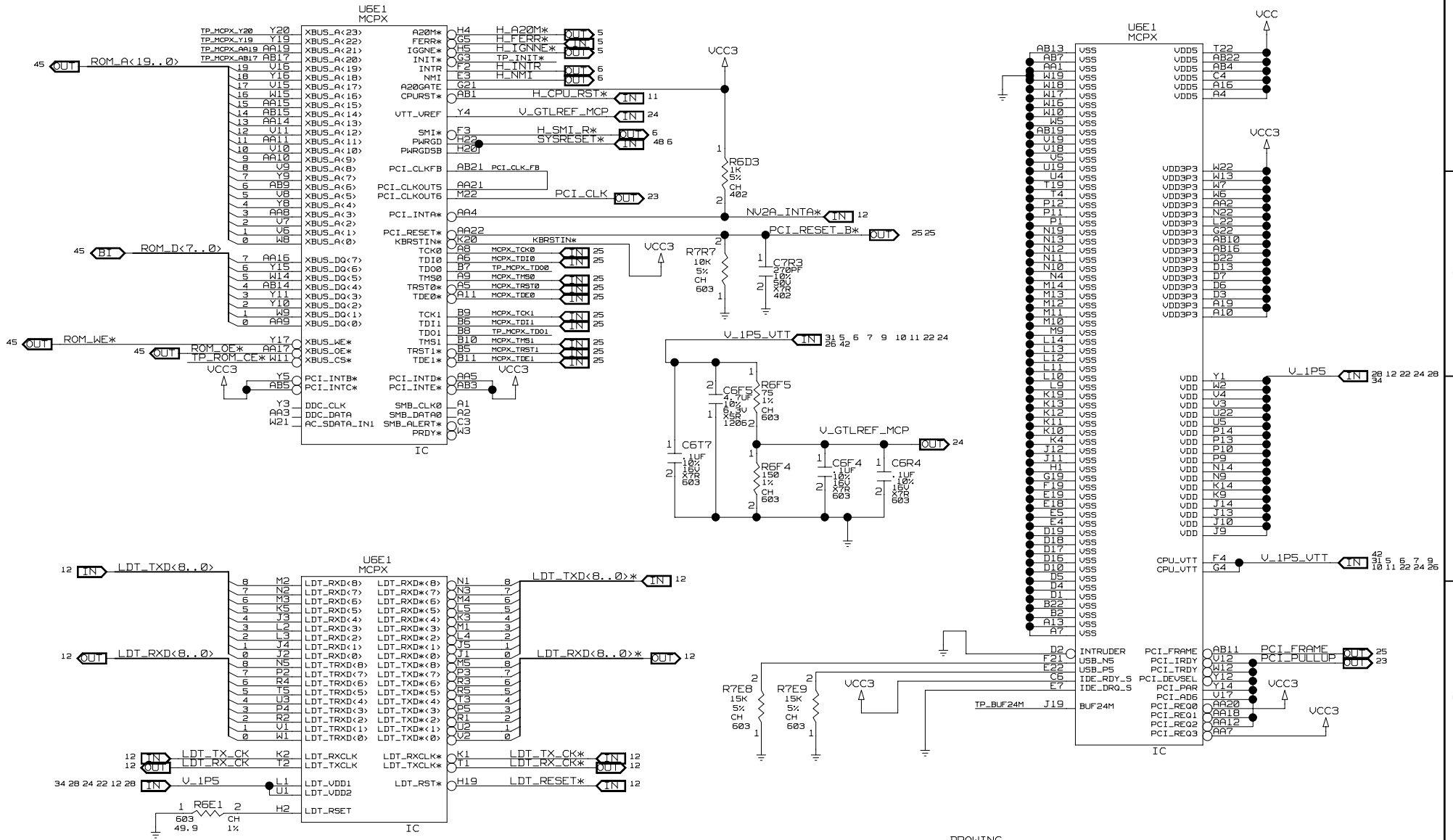


[PAGE_TITLE=NV2A DECOUPLING]

DRAWING
DVTFABK.SCH.1.22
Thu Aug 30 08:41:20 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	22	9.0


[PAGE_TITLE=MCPX 1 OF 2]
LPC DEBUG
MATERIAL=IC
U6E1
MCPX
[0]STRAP FOR LDT TERM:
* 0 = ENABLE INTERNAL TERM
1 = DISABLE INTERNAL TERM
* = CURRENT SETTING
[3]STRAP FOR CLK_13P5M:
* 1 = 13.5MHZ
0 = 14.318MHZ
L_AD<3..0>
L_FRAME*
L_SERIRQ
USB_1
USB_1*
USB_2
USB_2*
USB_3
USB_3*
USB_4
USB_4*
USB_5
USB_5*
USB_VREF
AUD_BCLK
AUD_SDO
AUD_RST*
AUD_SYNC
AUD_BCLK_R
AUD_SDI0
MII_TXD<3..0>
LAN_CLK_2_5M_TX
LAN_MII_TX_EN
MII_RXD<3..0>
LAN_CLK_2_5M_RX
LAN_MII_RX_DV
LAN_MII_RX_ER
LAN_MII_COL
LAN_MII_CRS
MII_MDIO
MII_MDC
IDE_PDCS1*
IDE_PDCS3*
IDE_PDA<2..0>
IDE_PDDREQ
IDE_PDDACK*
IDE_PDIOR*
IDE_PDIOW*
IDE_PDIORDY
IDE_PINTR
IDE_PDD<15..0>
RGB_SELECT*
LVLCNT0
SMI*
LVLCNT1
SMB_SCL
SMB_SDA
SB_CK_13P5M
V_BAT_RTC
MCP_VDD_PLL
SPDIF
PCI_PULLUP
PCI_CLK
L_FRAME*
PCI_RESET*
SMB_SDA
L_SERIRQ
SMB_SCL
PLL_DELAY*
MCP_3P3_DELAY
MCP_VDD_PLL
MII_TXD<3..0>
DVO_FIELD
R7E5
R7E6
R7E7
C7T3
R7R10
R6M1
R8B4
R6T3
R7E10
R6D1
R7E3
R7E2
R3F2
R3F3
R8E6
R8E5
R7B8
R8N4
R8N2
R8N5
R6U2
R6U3
C5E3
C6E1
C6E2
FB6E1
Q06F1
Q3F2
MMBT3904
J7D1
2X8HDR_4
R7R2
C7R2
Y6F1
Y6F2
32.768KHZ
C6E4
C6E5
R6E2
VCC3
VCC
STRAP
EMPTY
DRAWING
DVTFABK.SCH.1.23
Thu Aug 30 08:41:24 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER
A72507
PAGE
23
REV
9.0

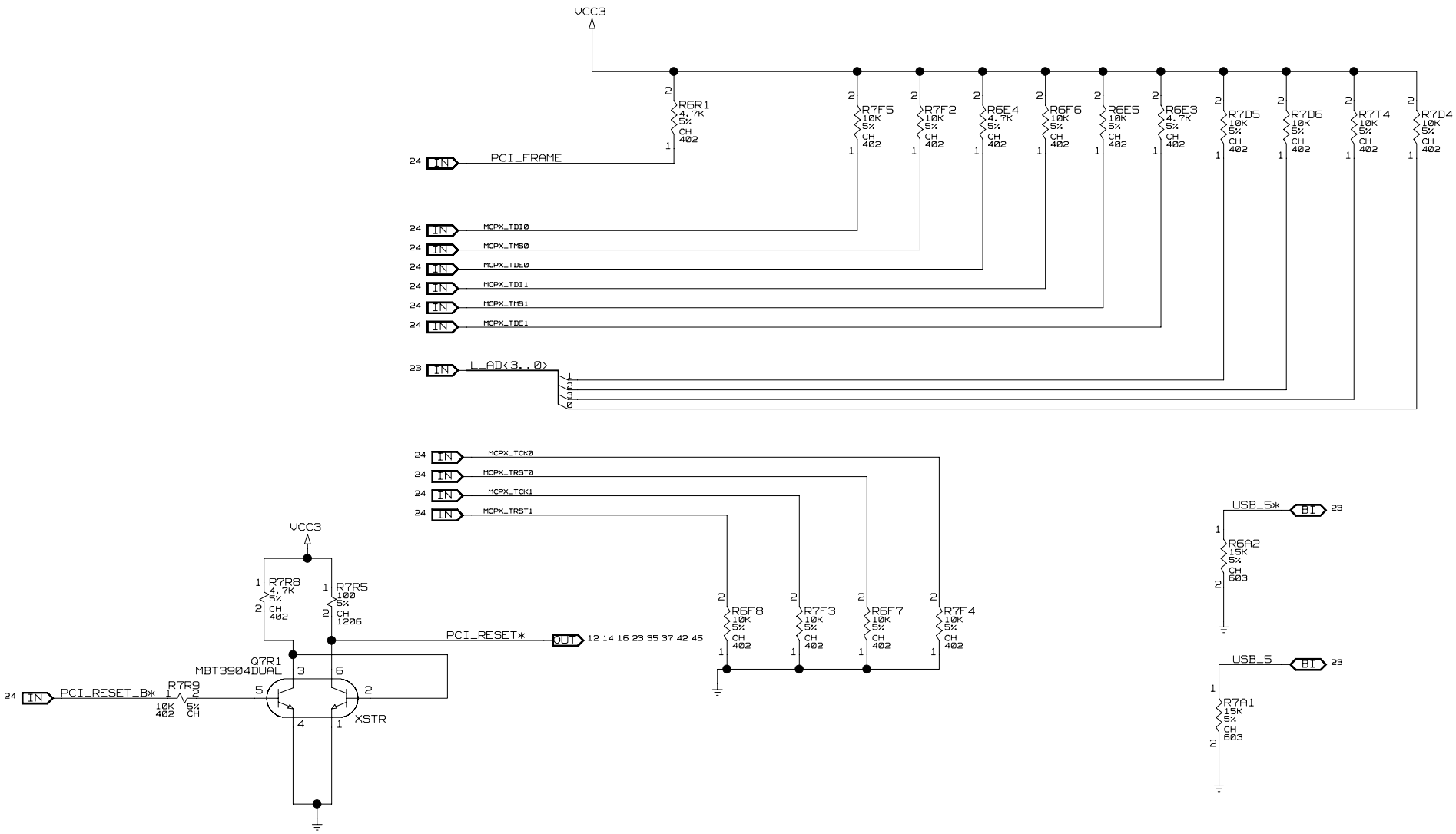


[PAGE_TITLE=MCPX 2 OF 2]

DRAWING
DVTFABK.SCH.1.24
Thu Aug 30 08:41:27 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	24	9.0

[DONOR_REV=1.0/page23]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page24]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:01 PM]

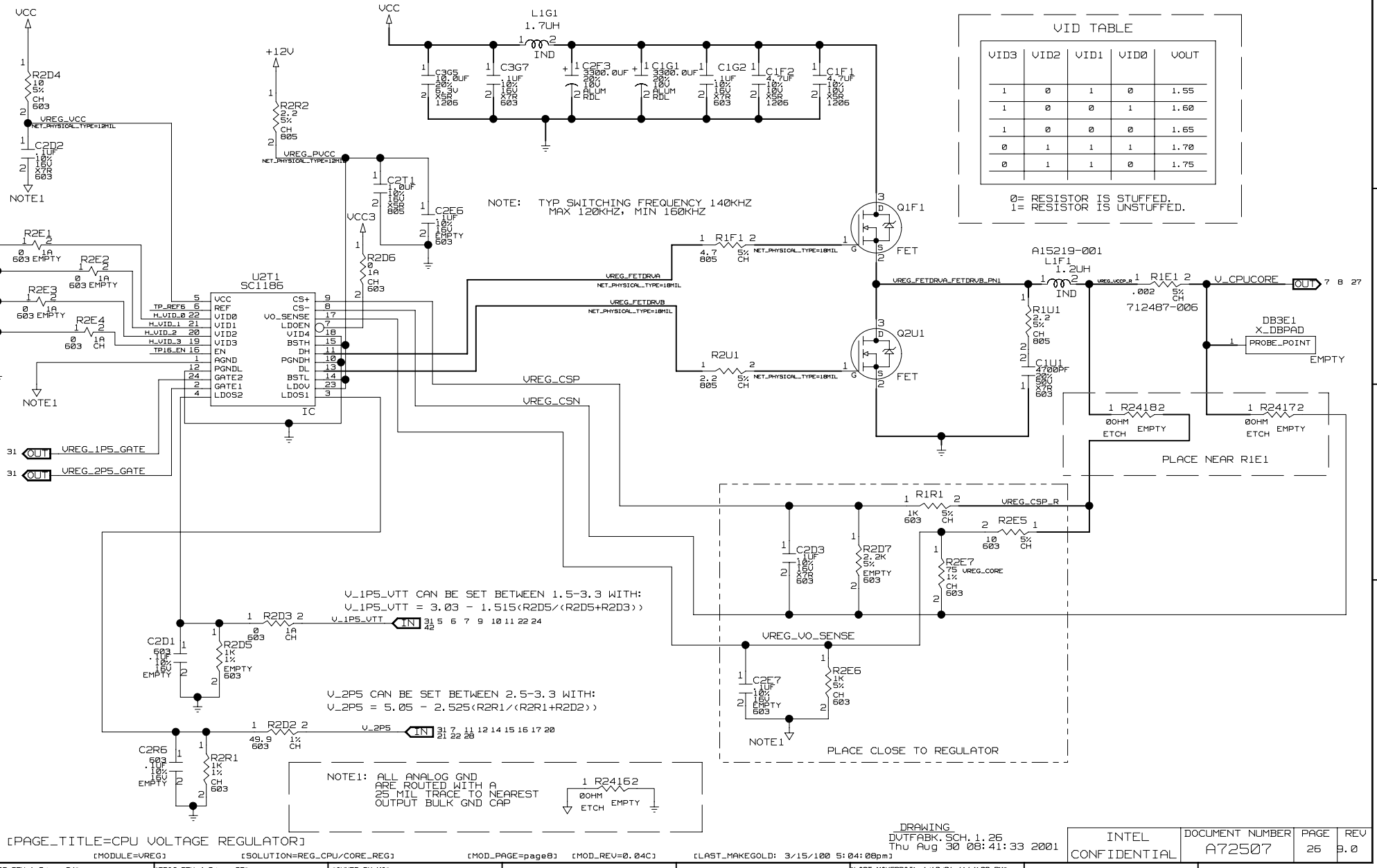


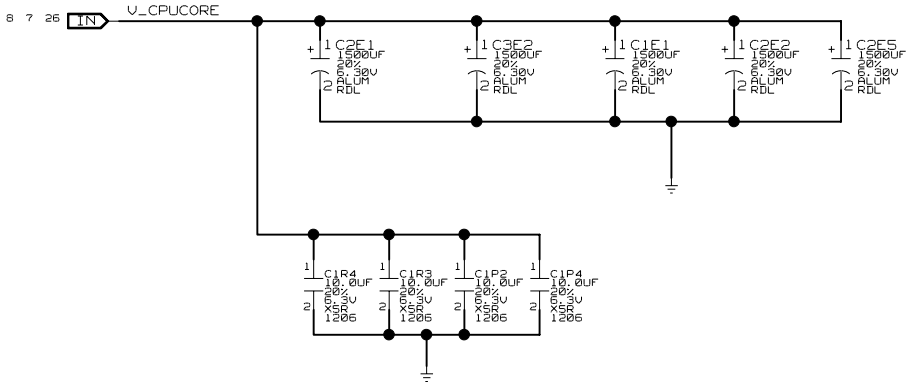
[PAGE_TITLE=MCPX INPUT STRAPS]

DRAWING

DVTFABK.SCH.1.25
LAST_MODIFIED=Thu Aug 30 08:41:30 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	25	9.0


VID TABLE
VID3 VID2 VID1 VID0 VOUT
1 0 1 0 1.55
1 0 0 1 1.60
1 0 0 0 1.65
0 1 1 1 1.70
0 1 1 0 1.75
0= RESISTOR IS STUFFED.
1= RESISTOR IS UNSTUFFED.
NOTE: TYP SWITCHING FREQUENCY 140KHZ
MAX 120KHZ, MIN 150KHZ
U2T1
SC1186
IC
VCC
+12V
VCC3
L1G1
1.7UH
IND
Q1F1
Q2U1
FET
A15219-001
L1F1
1.2UH
712487-006
V_CPUCORE
DB3E1
X_DBPAD
PROBE_POINT
EMPTY
VREG_FETDRVA
VREG_FETDRVB
VREG_CSP
VREG_CSN
VREG_VO_SENSE
VREG_CSP_R
VREG_1P5_GATE
VREG_2P5_GATE
V_1P5_VTT CAN BE SET BETWEEN 1.5-3.3 WITH:
V_1P5_VTT = 3.03 - 1.515(R2D5/(R2D5+R2D3))
V_2P5 CAN BE SET BETWEEN 2.5-3.3 WITH:
V_2P5 = 5.05 - 2.525(R2R1/(R2R1+R2D2))
PLACE NEAR R1E1
PLACE CLOSE TO REGULATOR
NOTE1: ALL ANALOG GND
ARE ROUTED WITH A
25 MIL TRACE TO NEAREST
OUTPUT BULK GND CAP
NOTE1
[PAGE_TITLE=CPU VOLTAGE REGULATOR]
[MODULE=VREG]
[SOLUTION=REG_CPU/CORE_REG]
[MOD_PAGE=page8]
[MOD_REV=0.04C]
[LAST_MAKEGOLD: 3/15/100 5:04:08pm]
DRAWING
DVTFABK.SCH.1.25
Thu Aug 30 08:41:33 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER A72507
PAGE 26
REV 9.0

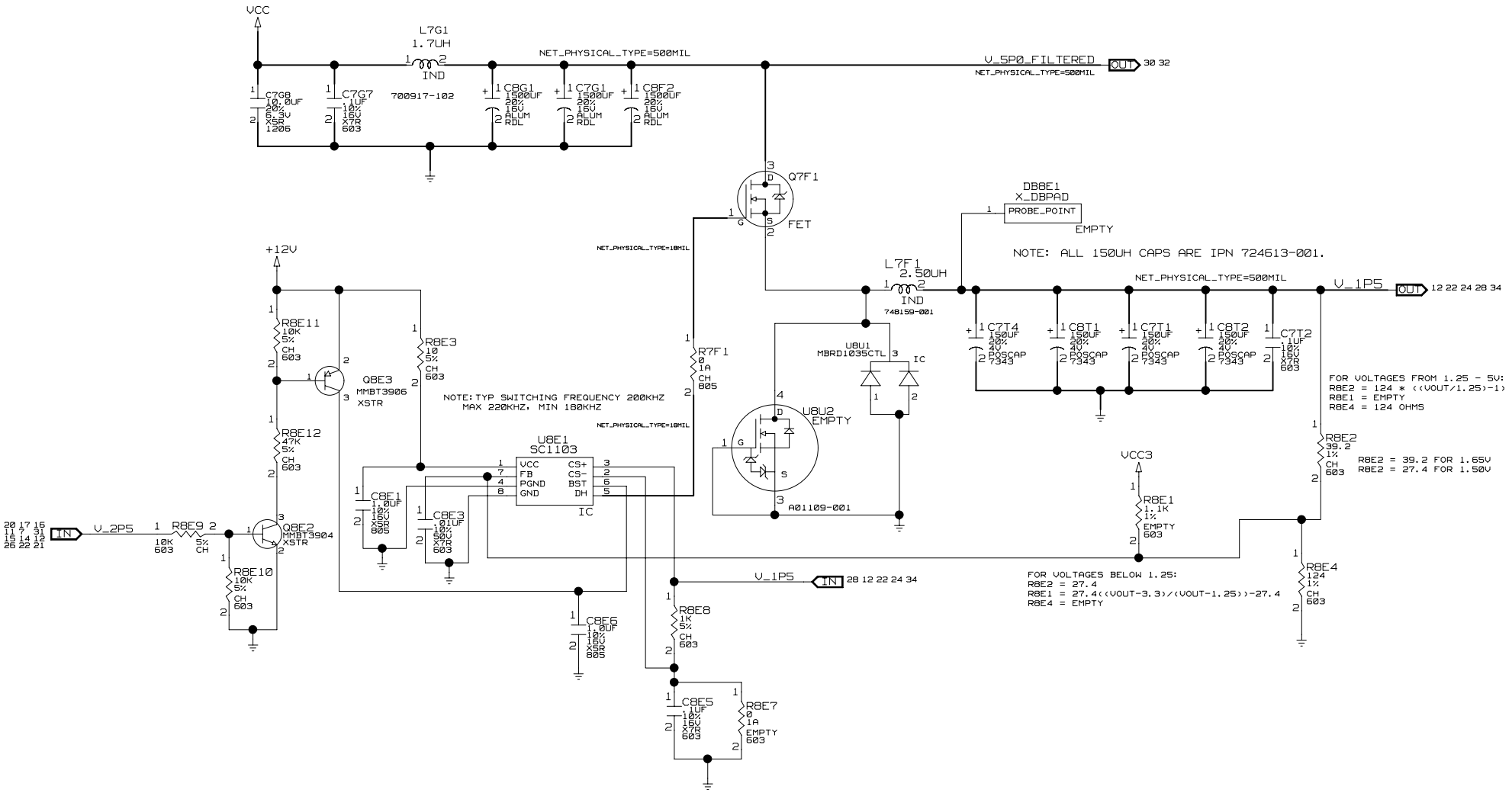


{PAGE_TITLE=CPU VREG OUTPUT FILTER}

{MODULE=VREG} {SOLUTION=REG_CPU/CORE_REG} {MOD_PAGE=page10} {MOD_REV=0.04C}
{PAGE_TITLE=NO_TITLE}
{LAST_MAKEGOLD: 3/15/100 5:02:46pm}

DRAWING
DVTFABK.SCH.1.27
Thu Aug 30 08:41:36 2001

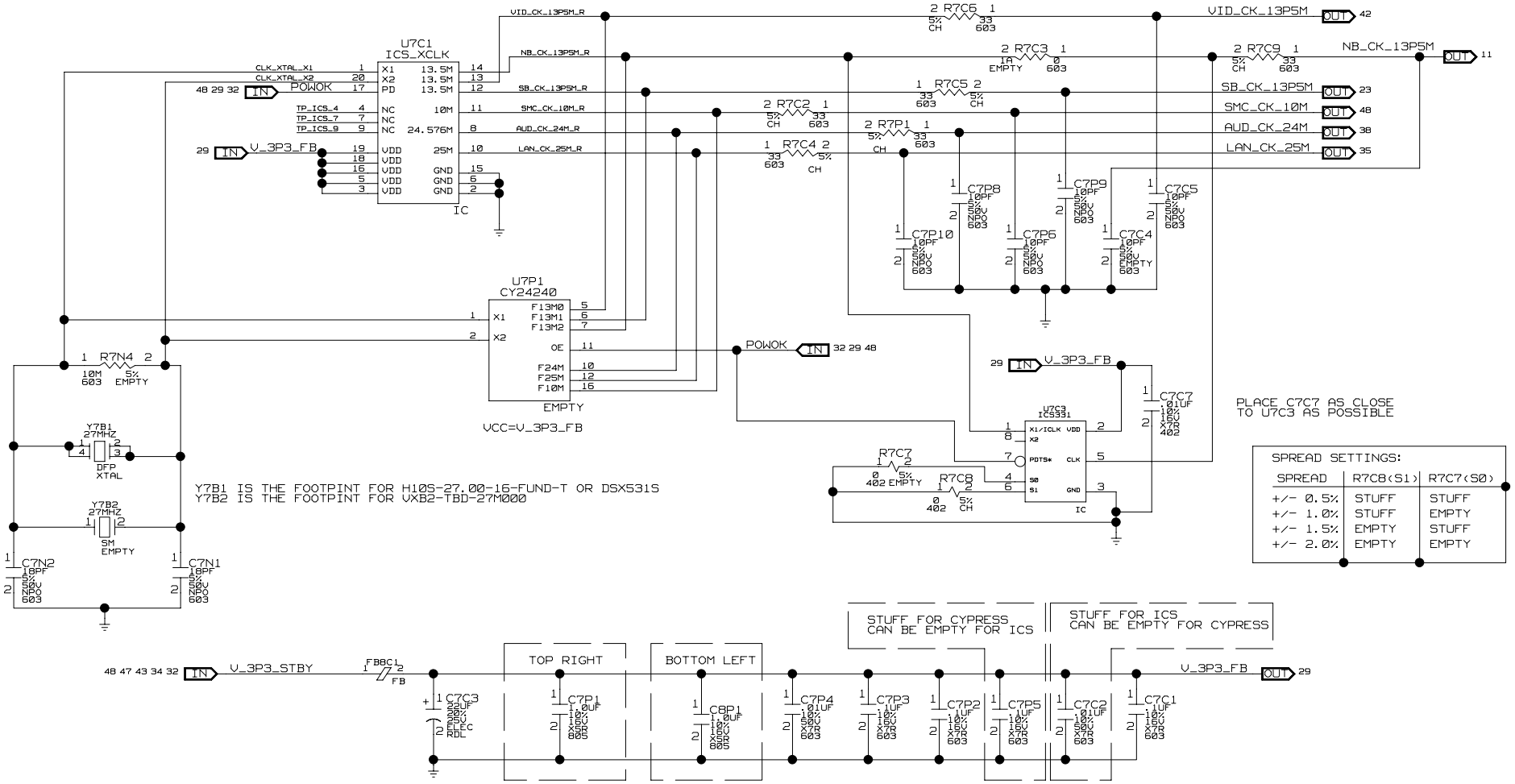
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	27	9.0



[PAGE_TITLE=1.5V SWITCHING REGULATOR]

DRAWING
DVTFABK.SCH.1.28
Thu Aug 30 08:41:39 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	28	9.0

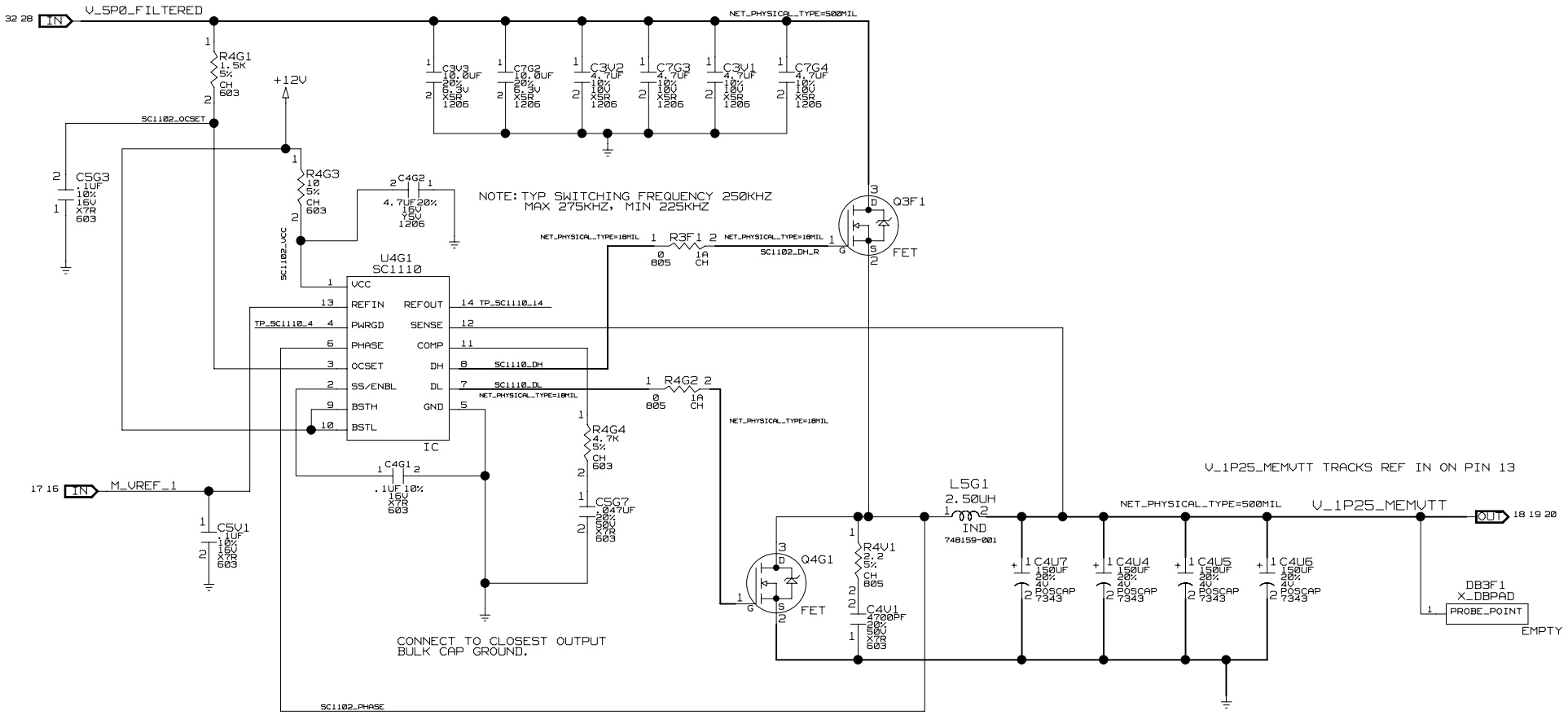


[PAGE_TITLE=CLOCK GENERATOR]

DRAWING
DVTFABK.SCH.1.29
Thu Aug 30 08:41:42 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	29	9.0

[DONOR_REV=1.0/page27]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page29]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:04 PM]

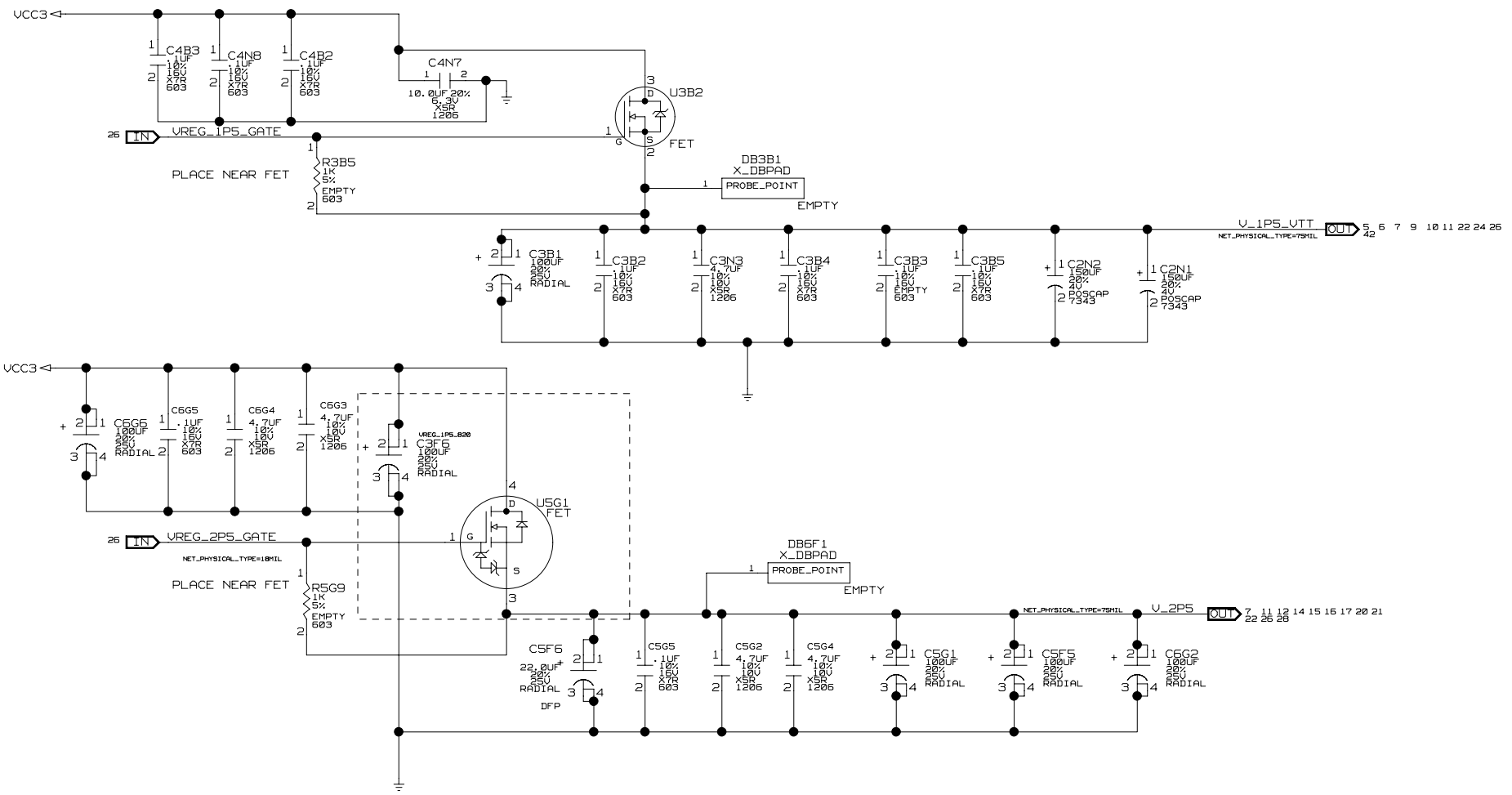


[PAGE_TITLE=1.25V SWITCHING REGULATOR]

DRAWING
DVTFABK.SCH.1.30
Thu Aug 30 08:41:45 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	30	9.0

[DONOR_REV=1.0/page29]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page29]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:05 PM]
[FULL_ID=1146-29-16166] [PAGE_INFO_ID=16166] [OWNED_BY=DE] [MODULE_ID=356-43-8110] [DONOR_ID=532-29-8870]

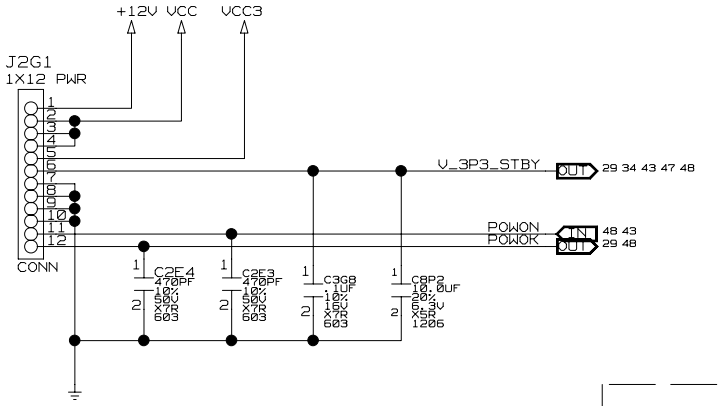


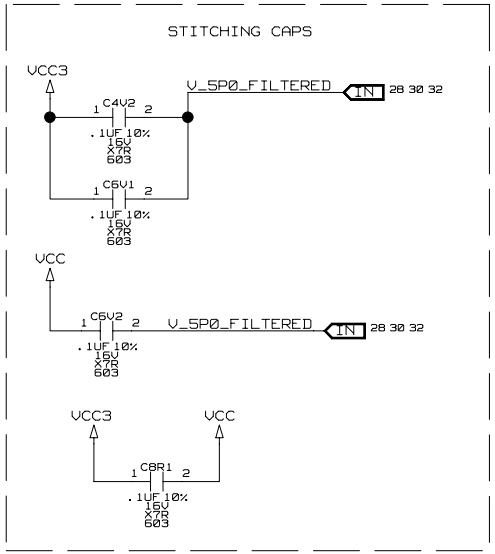
[PAGE_TITLE=LINEAR_REGULATORS_1.5_2.5]

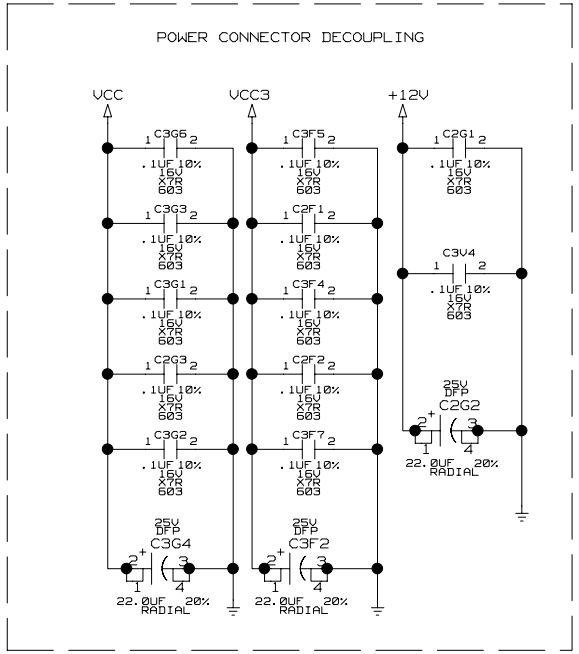
DRAWING
DVTFABK.SCH.1.31
Thu Aug 30 08:41:48 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	31	9.0

[DONOR_REV=1.0/page29] [DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page30] [PROJ_NAME=DVT_D--1146]
[OWNED_BY=MO] [MODULE=VREG]
[SOLUTION=SYSTEM_POWER_DELIVEY/INTEL]
[MOD_PAGE=page18]
[LAST_MAKEPROJ: 4/12/01 1:14:06 PM] [LAST_MAKEGOLD: 3/15/100 4:32:00pm]
[MODIFIED_BY_DE=N]
[MOD_REV=0.04]



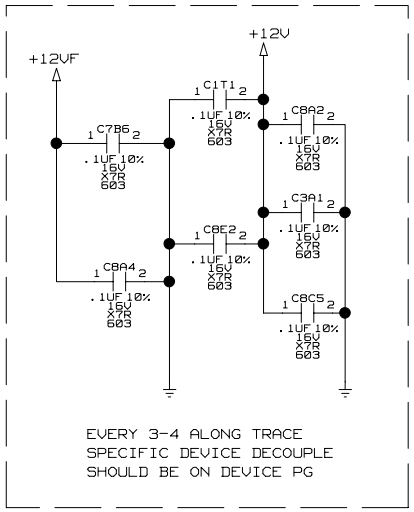


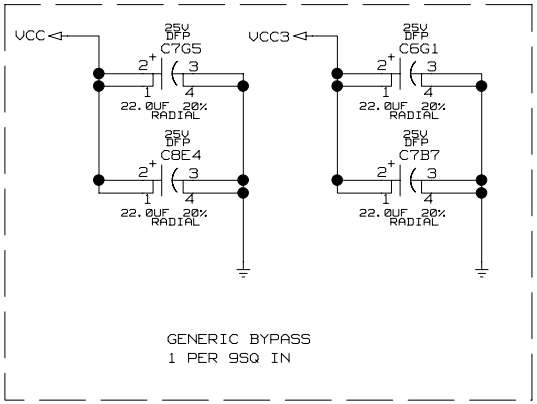


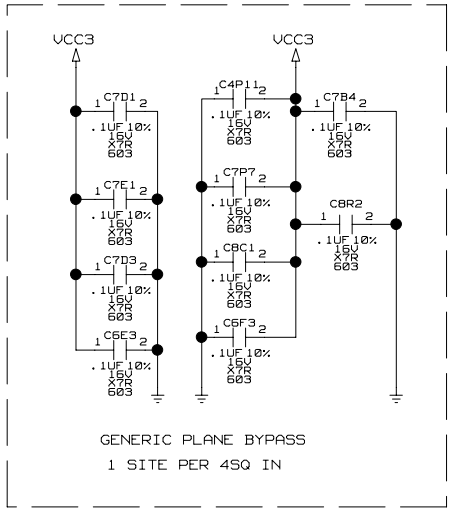
[PAGE_TITLE=DVT POWER CONNECTOR]

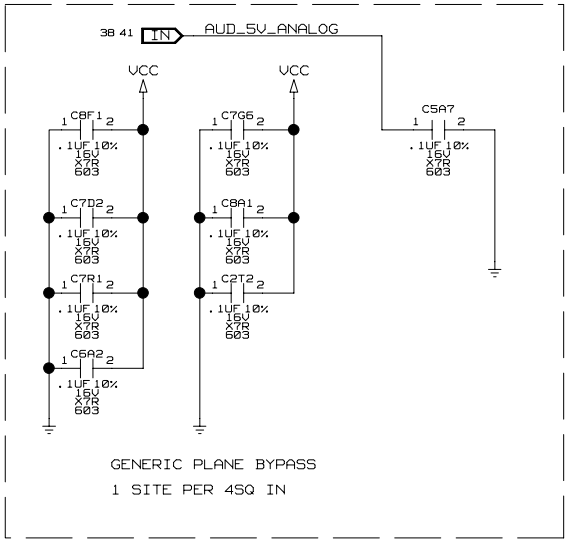
DRAWING
DVTFABK.SCH.1.32
Thu Aug 30 08:41:51 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	32	9.0





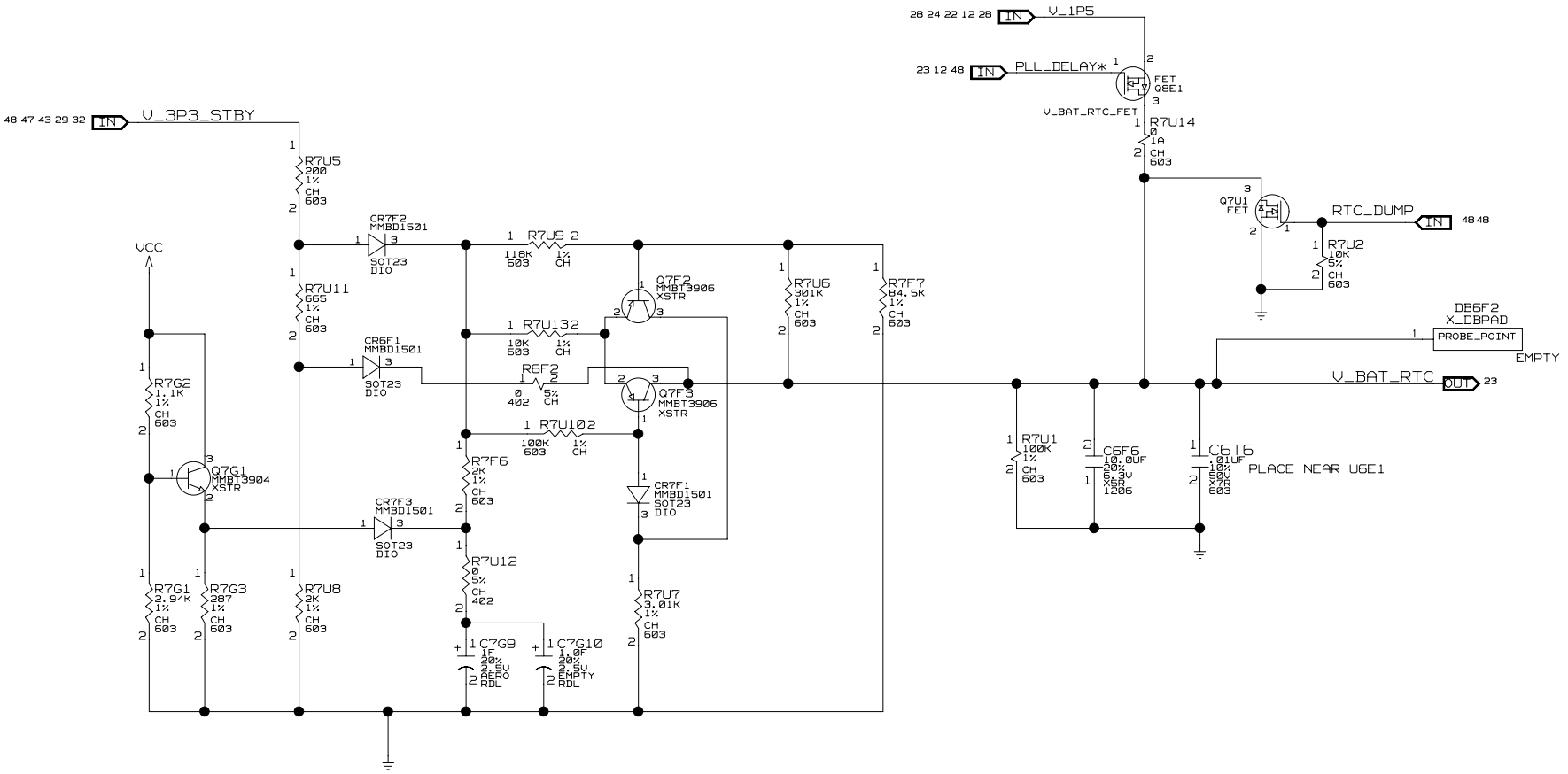




[PAGE_TITLE=BULK DECOUPLING]

DRAWING
DVTFABK.SCH.1.33
Thu Aug 30 08:41:54 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	33	9.0

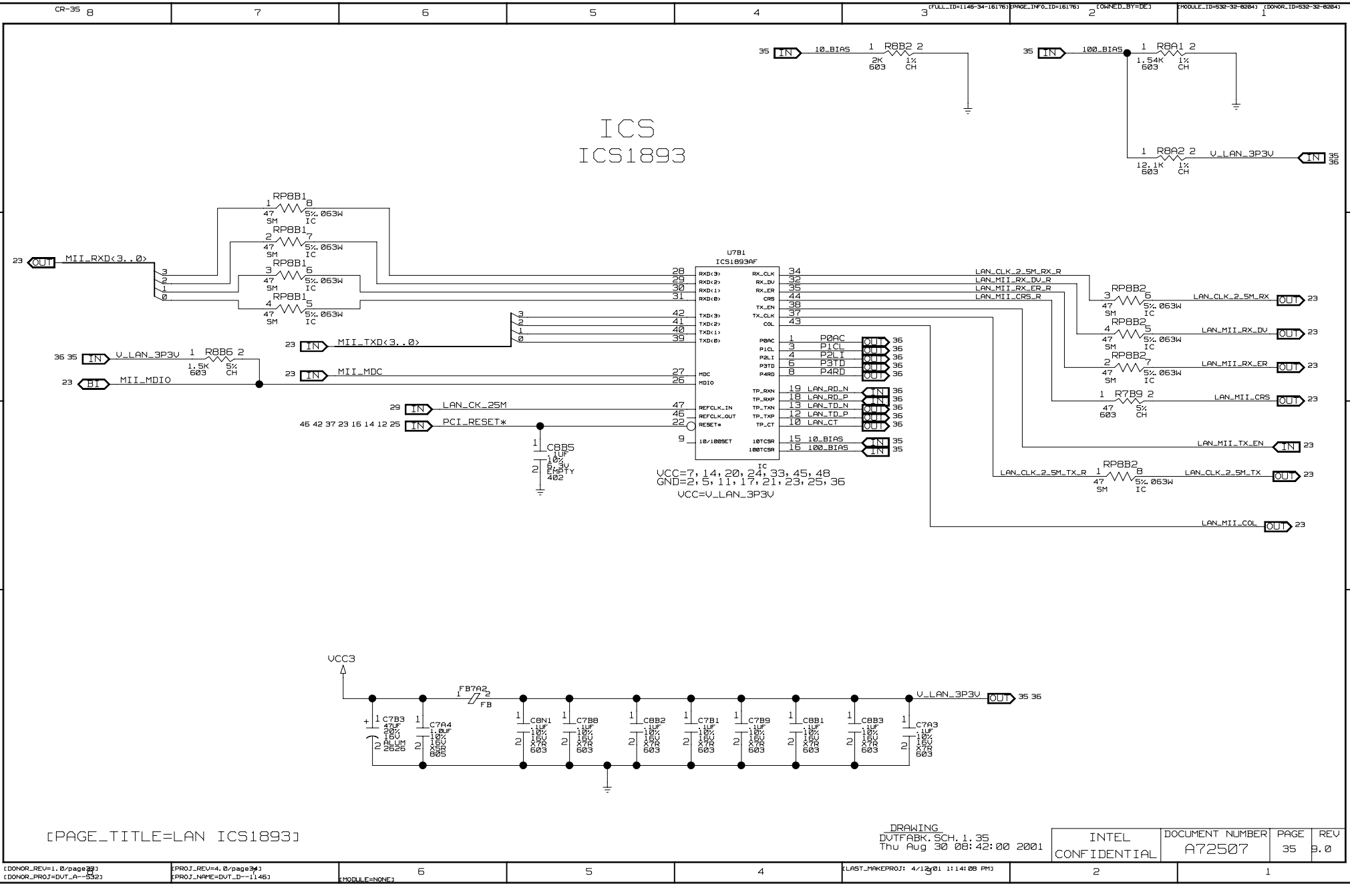


[PAGE_TITLE=SUPERCAP VBAT REGULATOR]

DRAWING
DVTFABK.SCH.1.34
Thu Aug 30 08:41:56 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	34	9.0

[DONOR_REV=1.0/page32] [DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page32] [PROJ_NAME=DVT_D--1146]
[OWNED_BY=MO] [MODULE=VREG]
[SOLUTION=SYSTEM_POWER_DELIVEY/INTEL]
[MOD_PAGE=page5]
[LAST_MAKEPROJ: 4/12/01 1:14:08 PM]
[LAST_MAKEGOLD: 3/15/100 4:32:25pm]
[MODIFIED_BY_DE=N]
[MOD_REV=0.04]



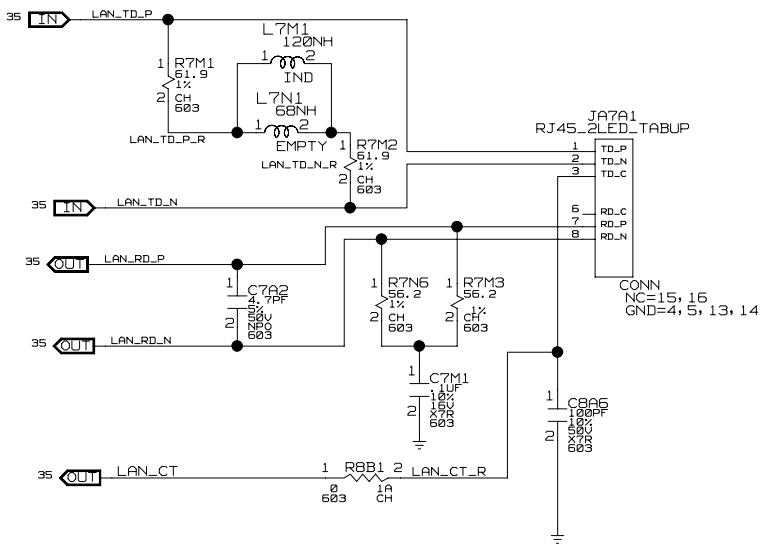
[PAGE_TITLE=LAN ICS1893]

DRAWING
DVTFABK.SCH.1.35
Thu Aug 30 08:42:00 2001

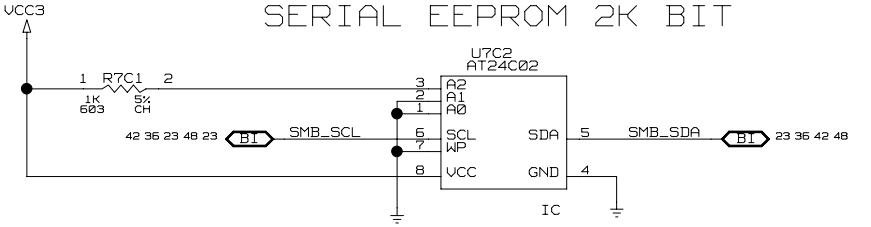
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	35	9.0

[DONOR_REV=1.0/page23]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page34]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:08 PM]

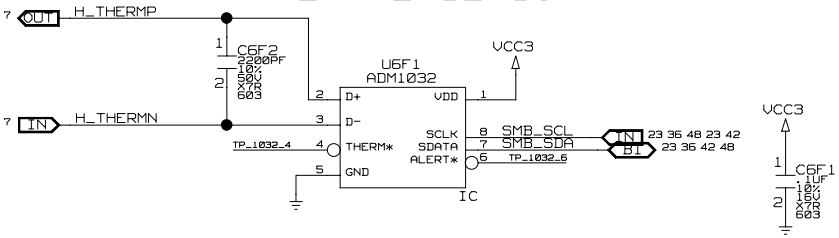
RJ45 SP JACK

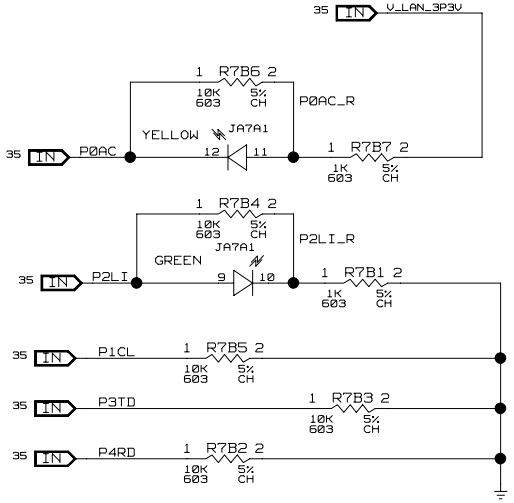


SERIAL EEPROM 2K BIT

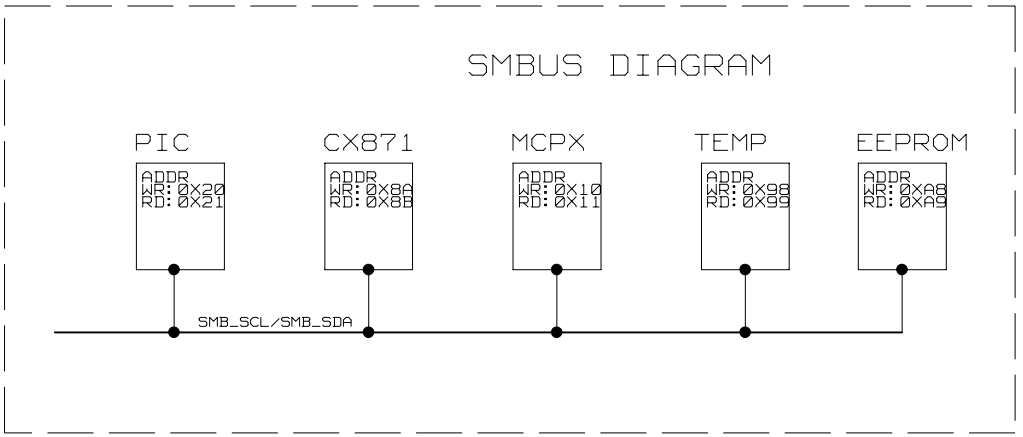


THERMAL SENSOR





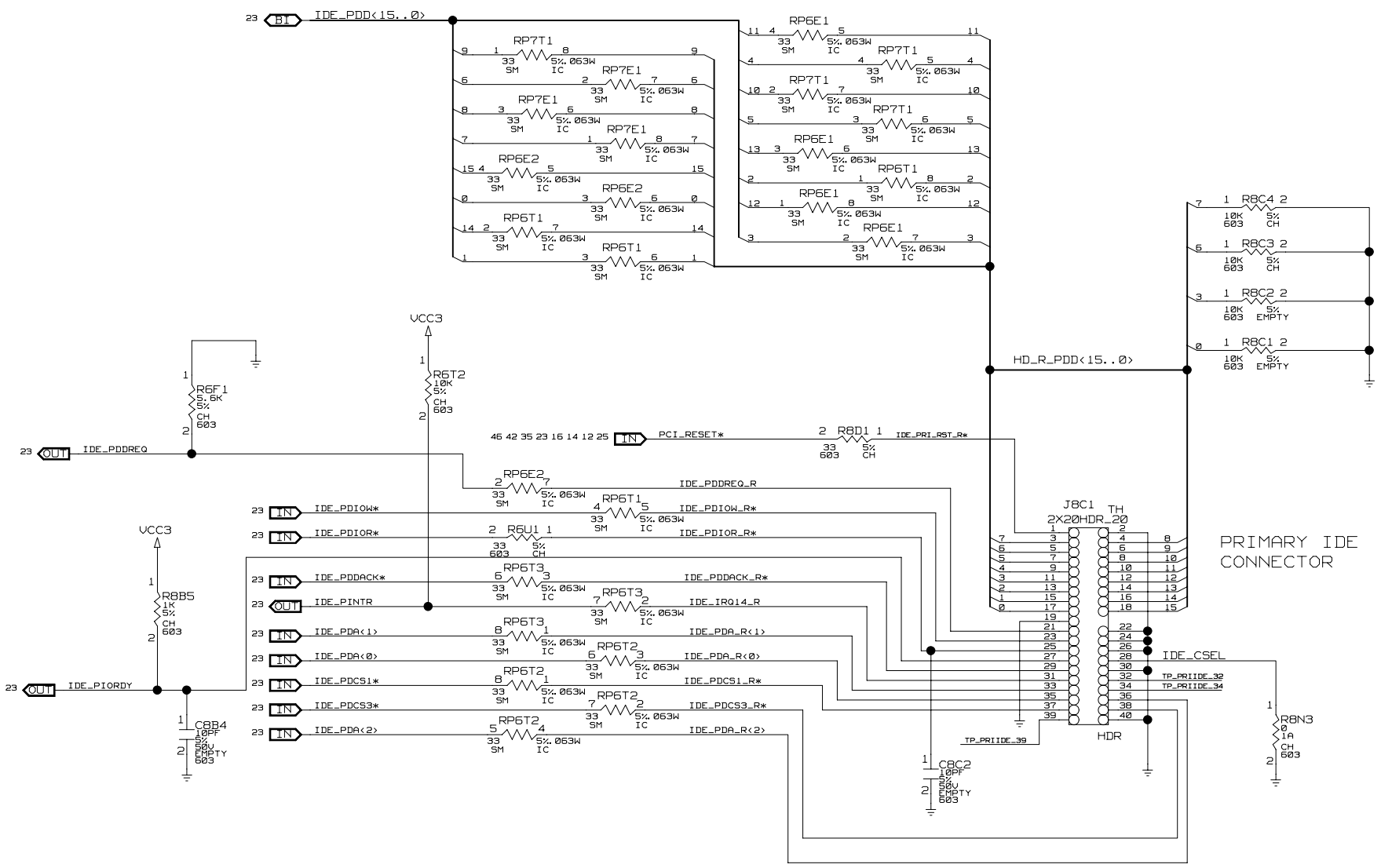
SMBUS DIAGRAM



[PAGE_TITLE=LAN JACK/THERMAL SENSE/EEPROM]

DRAWING
DVTFABK.SCH.1.36
Thu Aug 30 08:42:02 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	36	9.0

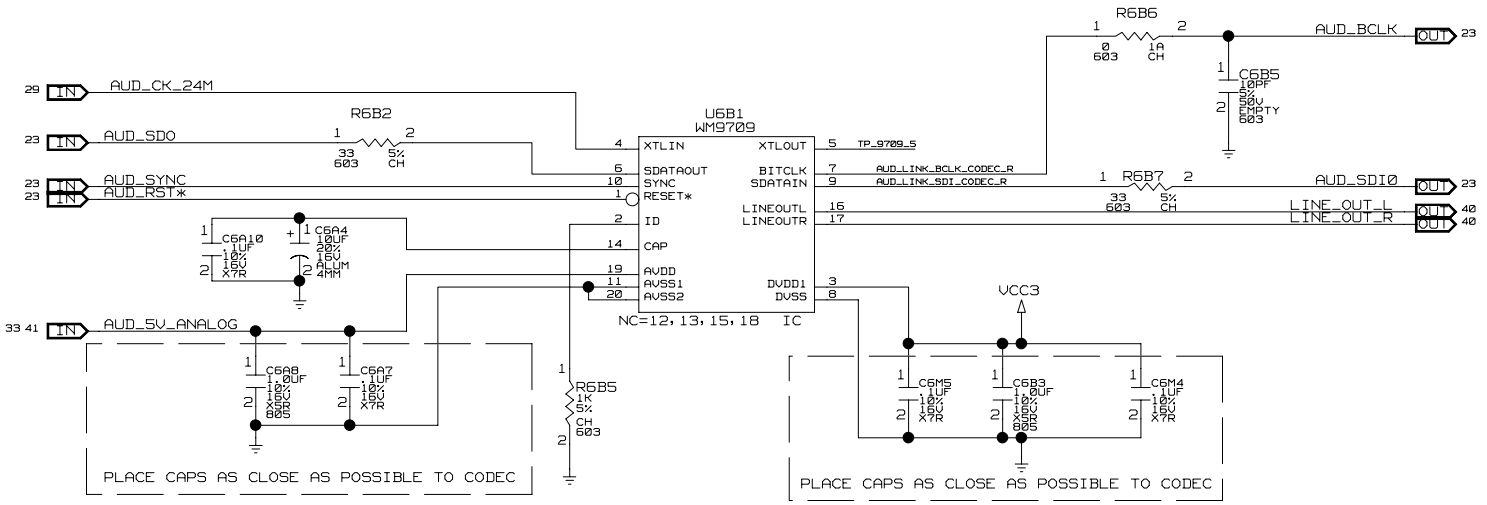


[PAGE_TITLE=IDE]

DRAWING
DVTFABK.SCH.1.37
Thu Aug 30 08:42:05 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	37	9.0

[MOD_REV=0.06D]

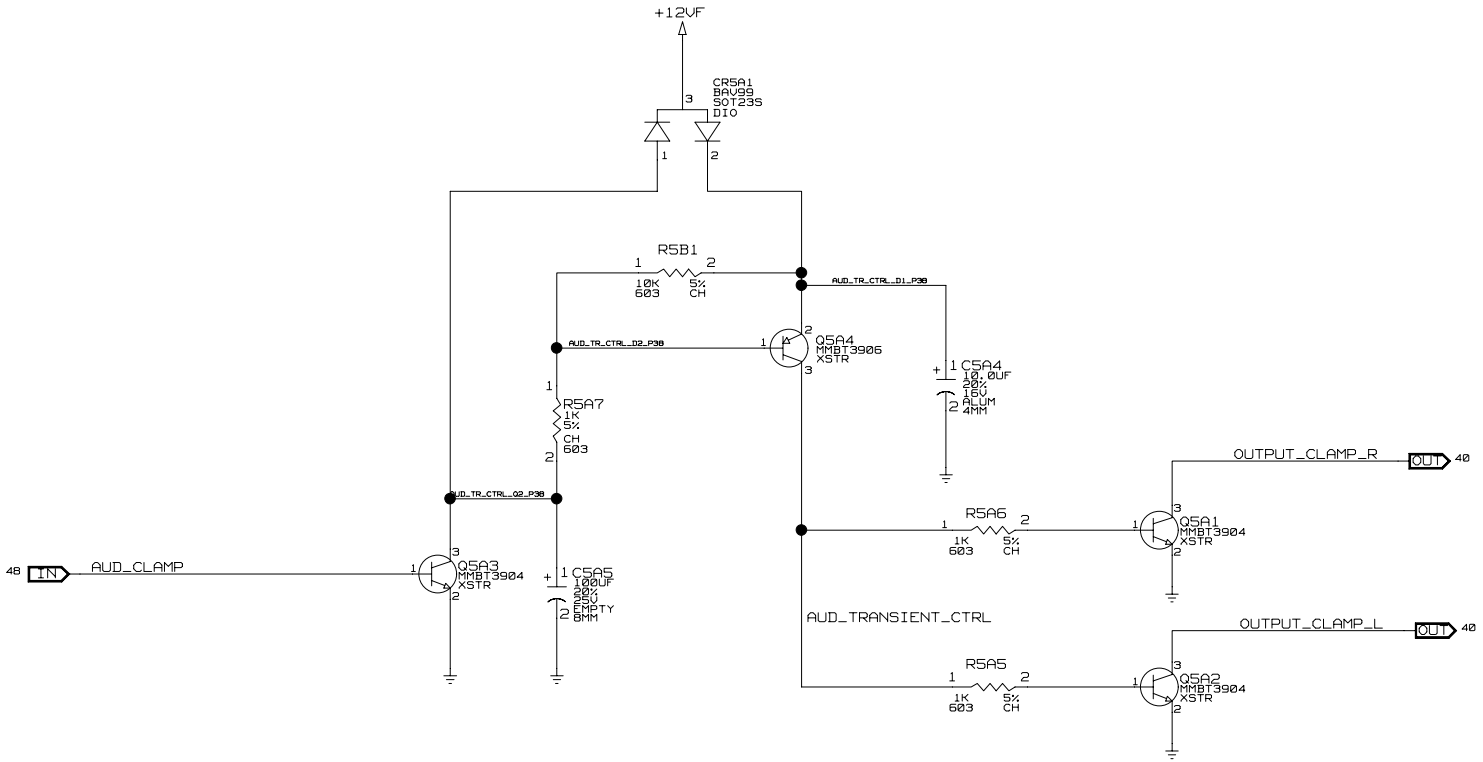


[PAGE_TITLE=AUDIO CODEC]

DRAWING
DVTFABK.SCH.1.38
Thu Aug 30 08:42:08 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	38	9.0

[FULL_ID=1146-38-16184] [PAGE_INFO_ID=16184] [MODULE_ID=372-27-6448] [DONOR_ID=532-38-9420]



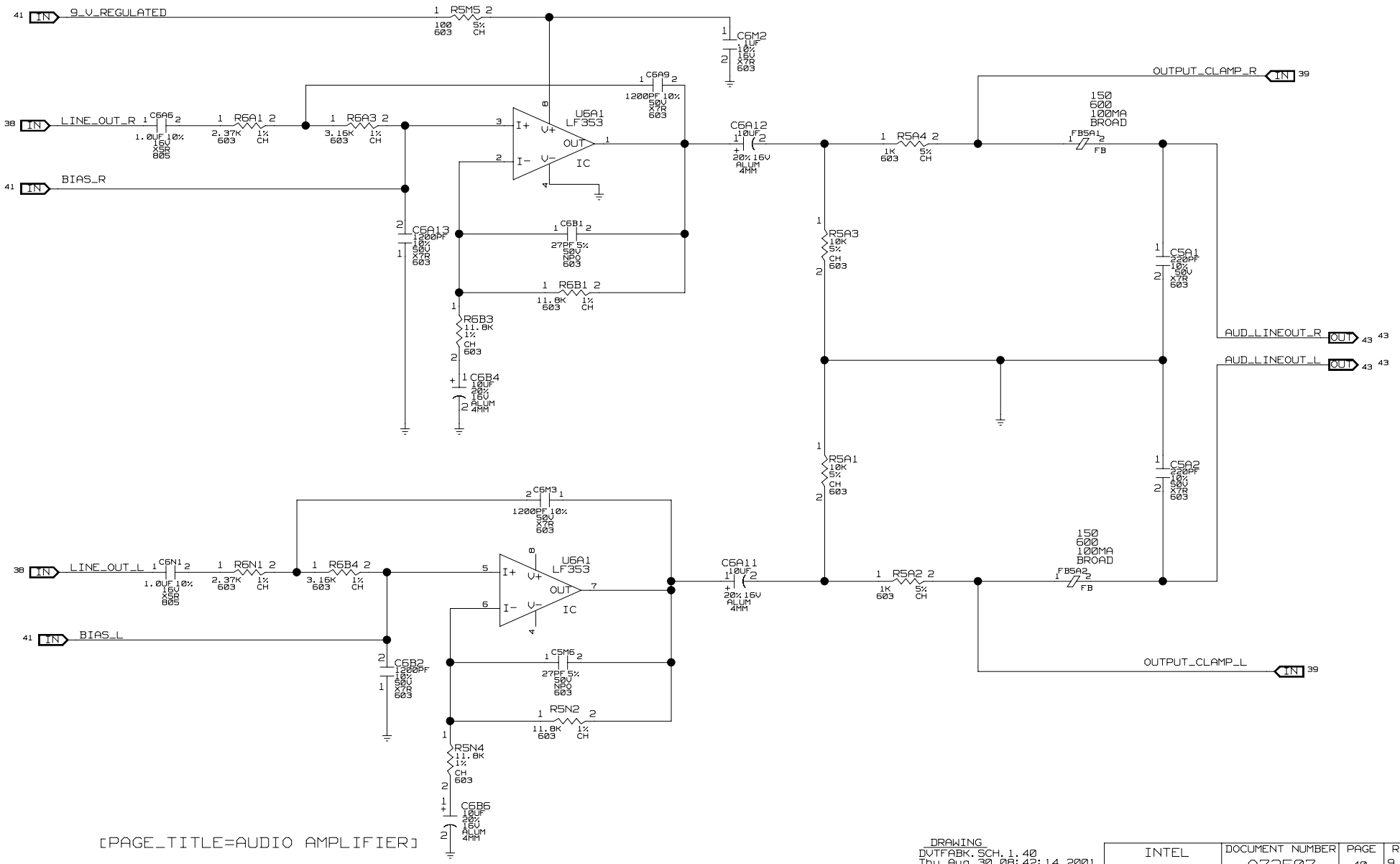
[PAGE_TITLE=AUDIO NO POP]

DRAWING
DVTFABK.SCH.1.39
Thu Aug 30 08:42:11 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	39	9.0

[MODULE=AUDIO] [SOLUTION=AUDIO\AUDIO--372] [MOD_PAGE=PAGE27] [MOD_REV=0.66C] [LAST_MAKEGOLD: 6/27/00 1:10:42 AM]

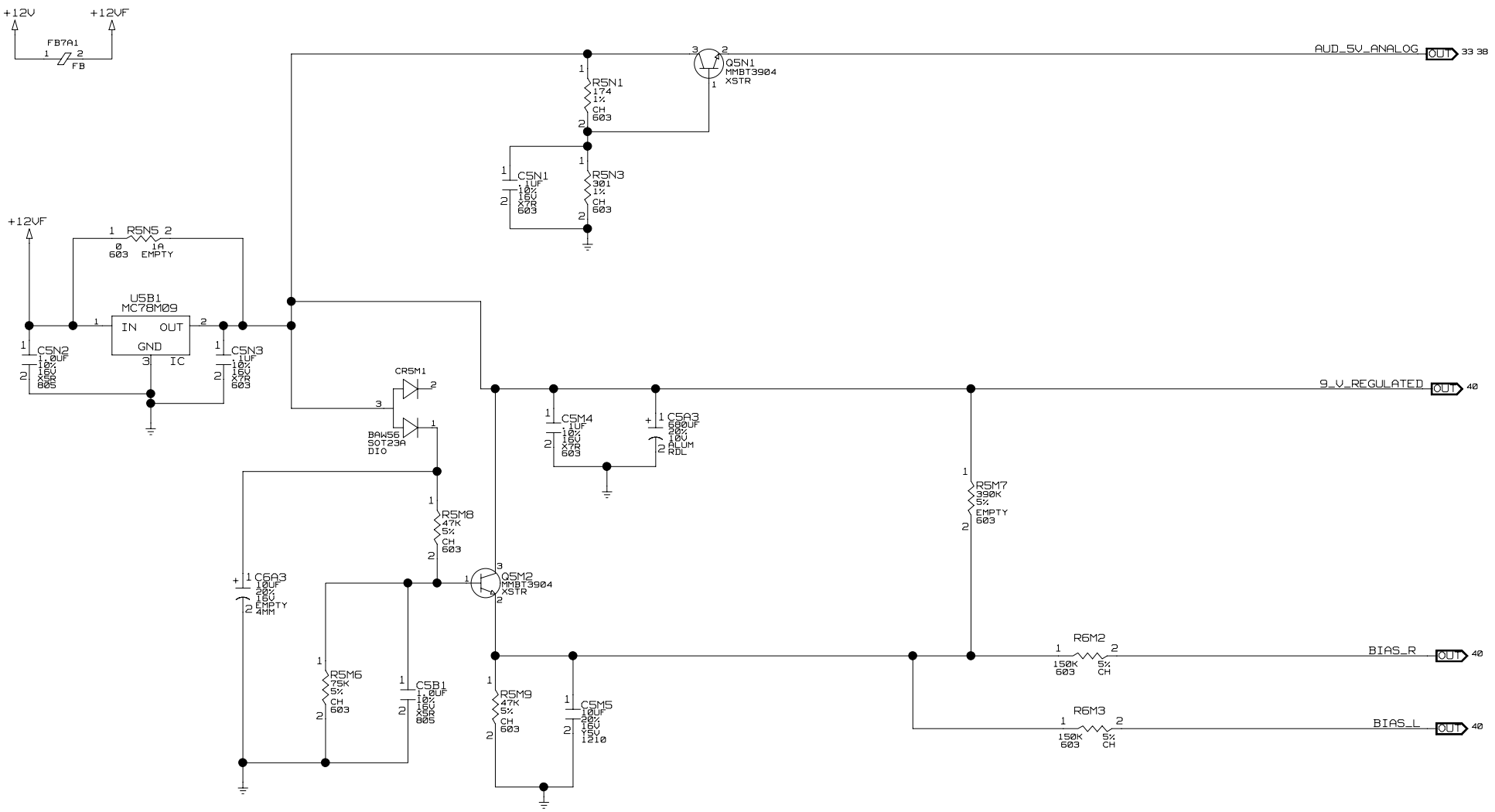
[DONOR_REV=1.0/page37] [DONOR_PROJ=DVT_A--532] [PROJ_REV=4.0/page38] [PROJ_NAME=DVT_D--1146] [OWNED_BY=MO] [LAST_MAKEPROJ: 4/12/01 1:14:12 PM] [MODIFIED_BY_DE=N]



[PAGE_TITLE=AUDIO AMPLIFIER]

DRAWING
DVTFABK.SCH.1.40
Thu Aug 30 08:42:14 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	40	9.0

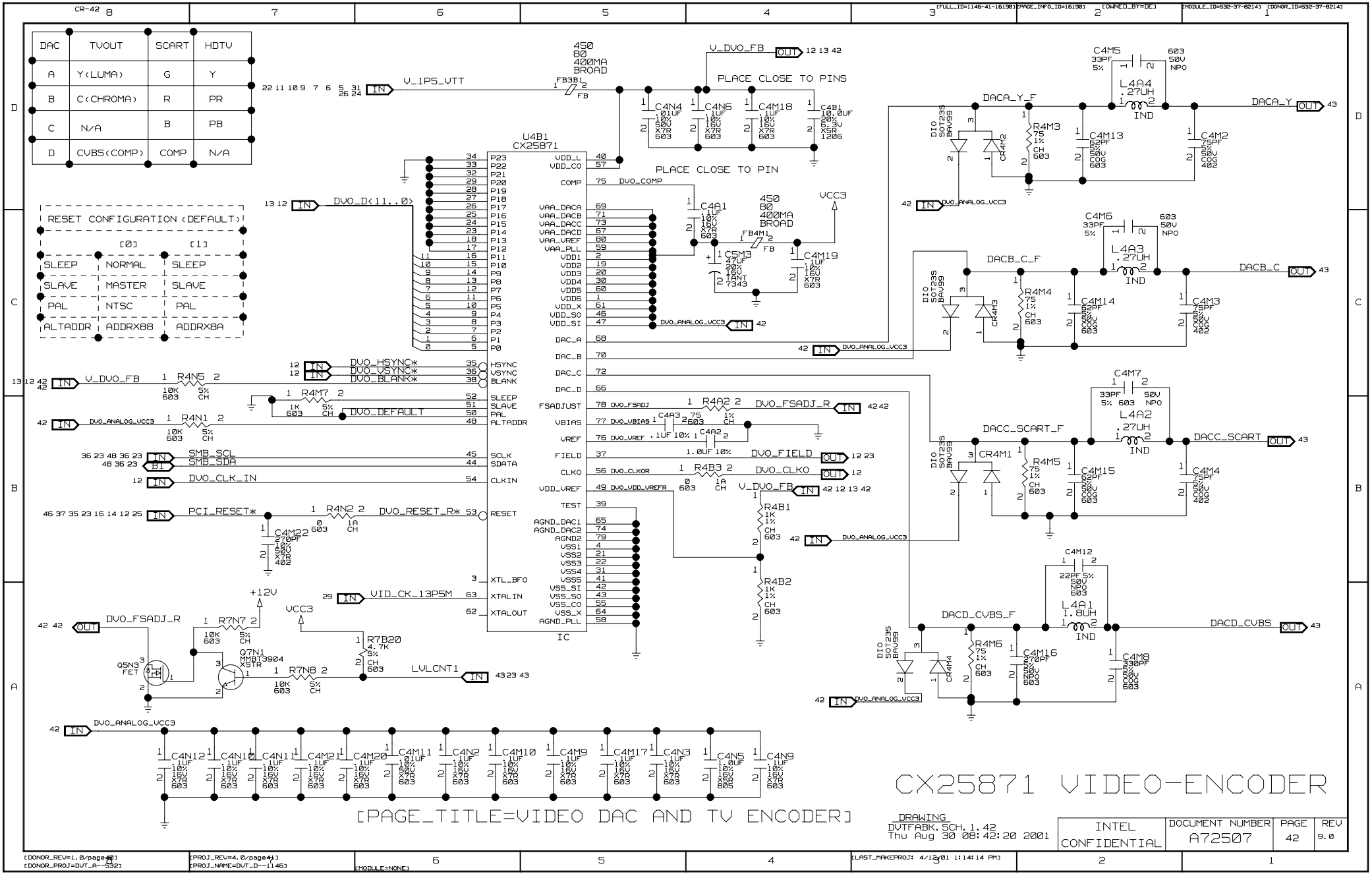


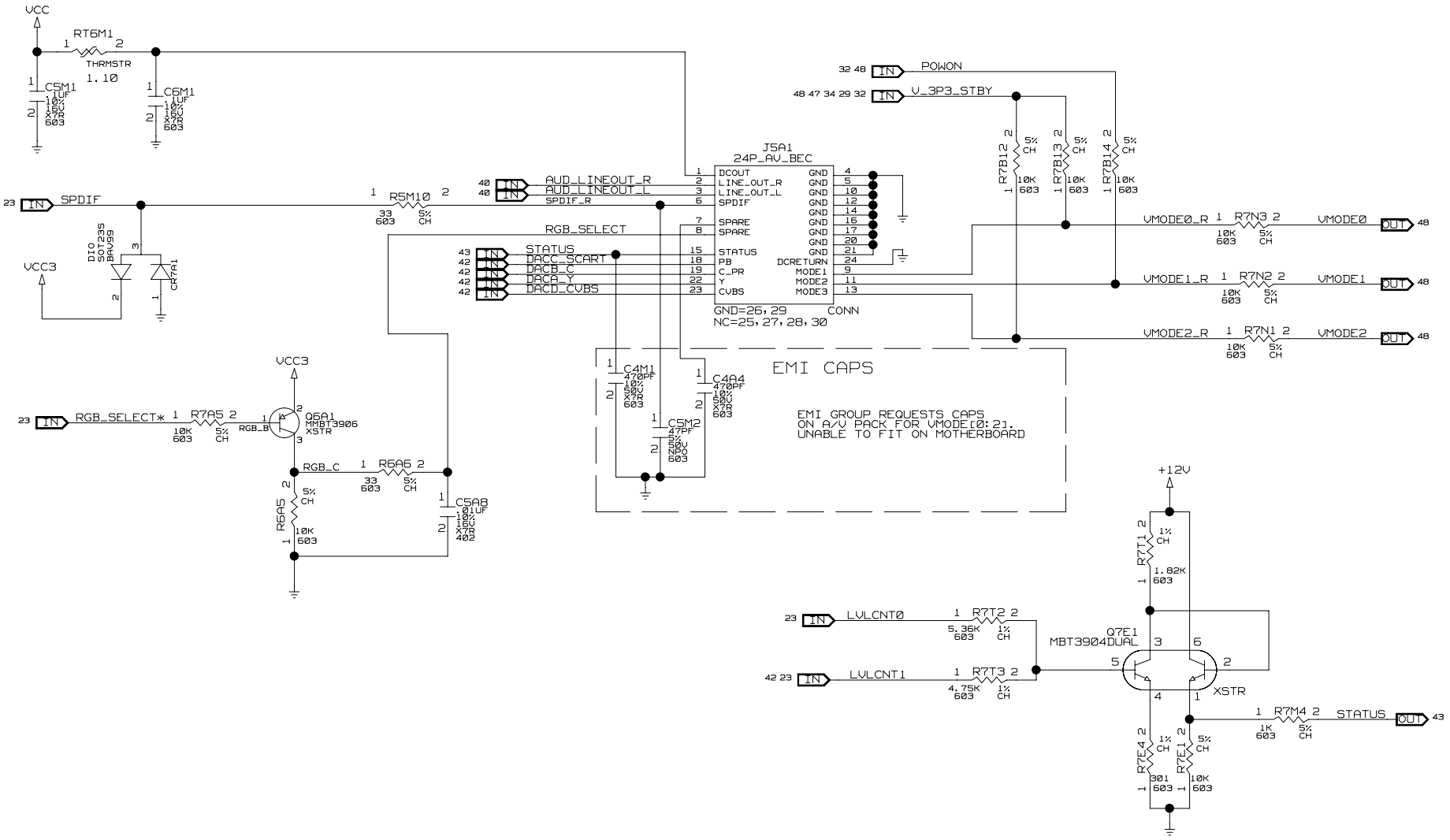
[PAGE_TITLE=AUDIO VREG AND BIAS]

DRAWING
DVTFABK.SCH.1.41
Thu Aug 30 08:42:17 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	41	9.0

[DONOR_REV=1.0/page29]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page40]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:13 PM]
[FULL_ID=1146-40-16188] [PAGE_INFO_ID=16188] [OWNED_BY=DE] [MODULE_ID=532-40-9424] [DONOR_ID=532-40-9424]


DAC | TVOUT | SCART | HDTV
A | Y(LUMA) | G | Y
B | C(CHROMA) | R | PR
C | N/A | B | PB
D | CVBS(COMP) | COMP | N/A
RESET CONFIGURATION (DEFAULT)
[0] [1]
SLEEP | NORMAL | SLEEP
SLAVE | MASTER | SLAVE
PAL | NTSC | PAL
ALTADDR | ADDRX88 | ADDRX8A
U4B1
CX25871
IC
V_1P5_VTT
V_DVO_FB
PLACE CLOSE TO PINS
PLACE CLOSE TO PIN
DVO_D<11..0>
DVO_HSYNC*
DVO_VSYNC*
DVO_BLANK*
DVO_DEFAULT
DVO_ANALOG_VCC3
SMB_SCL
SMB_SDA
DVO_CLK_IN
PCI_RESET*
DVO_RESET_R*
VID_CK_13P5M
DVO_FSADJ_R
LVLCNT1
VCC3
+12V
DACA_Y_F
DACB_C_F
DACC_SCART_F
DACD_CVBS_F
DACA_Y
DACB_C
DACC_SCART
DACD_CVBS
CX25871 VIDEO-ENCODER
[PAGE_TITLE=VIDEO DAC AND TV ENCODER]
DRAWING
DVTFABK.SCH.1.42
Thu Aug 30 08:42:20 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER A72507
PAGE 42
REV 9.0



[PAGE_TITLE=AV CONNECTOR]

DRAWING
DVTFABK.SCH.1.43
Thu Aug 30 08:42:24 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	43	9.0

[FULL_ID=1146-43-16194] [PAGE_INFO_ID=16194] [OWNED_BY=DE] [MODULE_ID=532-39-8218] [DONOR_ID=532-39-8218]

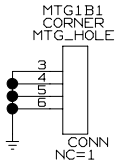
LABELS

A19177-001
LB8D1
LABEL

1375X250_TARGET

INTEL INTELLIGENT SERIAL NUMBER TARGET.

MOUNTING HOLES



MTG6F1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MTG8A1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MTG1E1
MTG_HOLE_EDGE
NC1 1
EMPTY
GND=2, 3, 4, 5, 6, 7, 8

MTG1F1
MTG_HOLE_EDGE
NC1 1
EMPTY
GND=2, 3, 4, 5, 6, 7, 8

MTG8G1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MTG4E1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MTG7C1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MTG4B1
MTG_HOLE
NC9 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

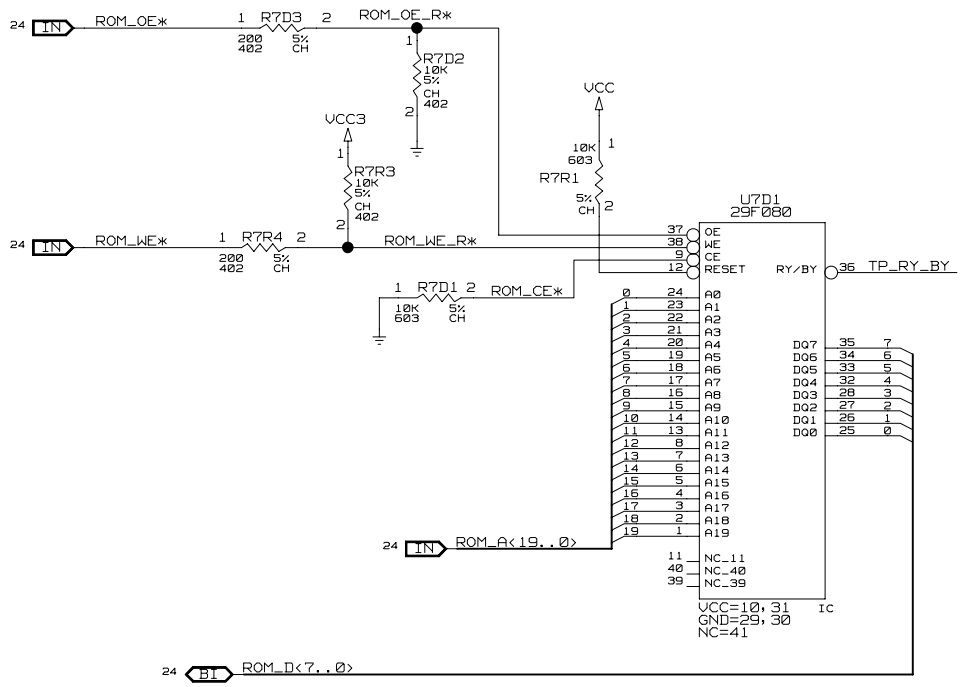
[PAGE_TITLE=LABELS AND MOUNTING HOLES]

DRAWING
DVTFABK.SCH.1.44
Thu Aug 30 08:42:27 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	44	9.0

[DONOR_REV=1.0/page42] [DONOR_PROJ=DVT_A--532] [PROJ_REV=4.0/page42] [PROJ_NAME=DVT_D--1146] [MODULE=NONE] [LAST_MAKEPROJ: 4/12/01 1:14:15 PM]

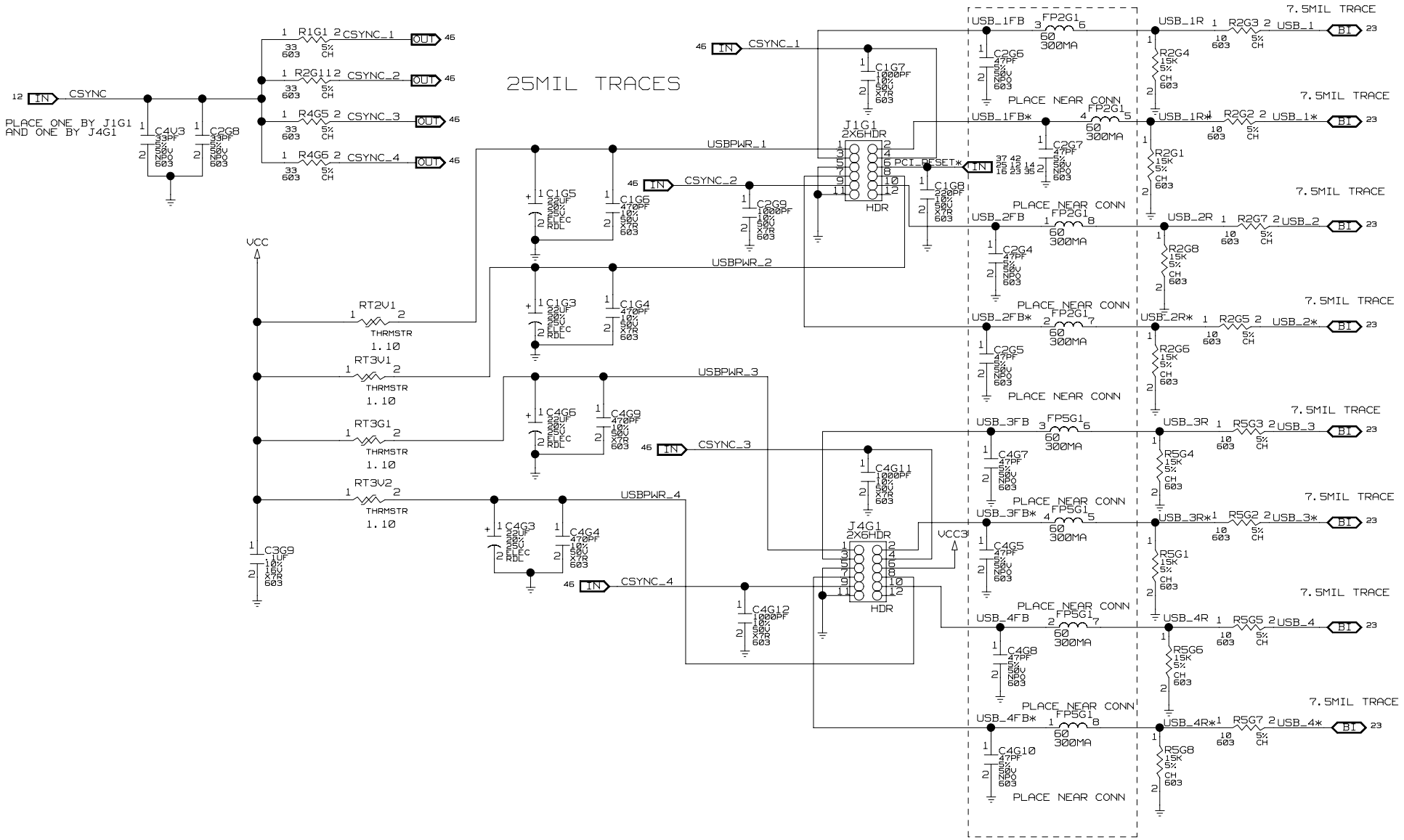
FOR PRODUCTION:
EMPTY R7D3 AND R7R4



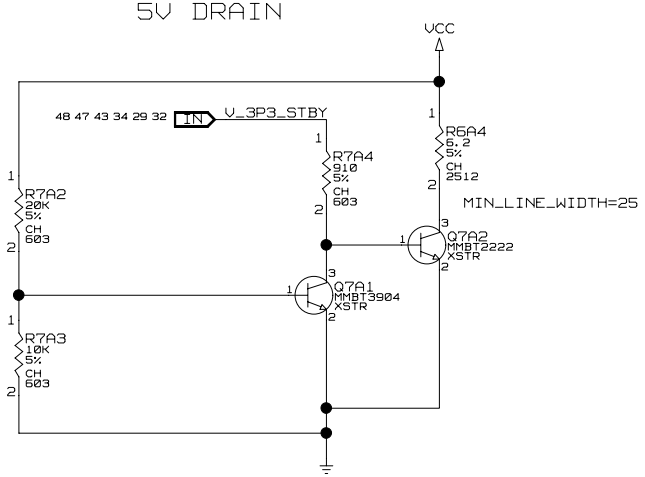
[PAGE_TITLE=FLASH]

DRAWING
DVTFABK.SCH.1.45
Thu Aug 30 08:42:30 2001

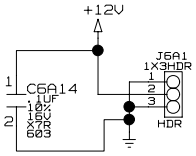
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	45	9.0


25MIL TRACES
7.5MIL TRACE
PLACE NEAR CONN
PLACE ONE BY J1G1 AND ONE BY J4G1
CSYNC
CSYNC_1
CSYNC_2
CSYNC_3
CSYNC_4
USBPWR_1
USBPWR_2
USBPWR_3
USBPWR_4
PCI_RESET*
VCC
VCC3
J1G1 2X6HDR
J4G1 2X6HDR
HDR
FP2G1
FP5G1
USB_1FB
USB_1FB*
USB_2FB
USB_2FB*
USB_3FB
USB_3FB*
USB_4FB
USB_4FB*
USB_1R
USB_1R*
USB_2R
USB_2R*
USB_3R
USB_3R*
USB_4R
USB_4R*
USB_1
USB_1*
USB_2
USB_2*
USB_3
USB_3*
USB_4
USB_4*
THRMSTR
1.10
[PAGE_TITLE=USB FRONT PANEL]
DRAWING
DVTFABK.SCH.1.46
Thu Aug 30 08:42:32 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER
A72507
PAGE
46
REV
9.0
[FULL_ID=1146-45-16198]
[PAGE_INFO_ID=16198]
[OWNED_BY=DE]
[MODULE_ID=356-31-5662]
[DONOR_ID=532-41-8222]
[DONOR_REV=1.0/page44]
[DONOR_PROJ=DVT_A--532]
[PROJ_REV=4.0/page45]
[PROJ_NAME=DVT_D--1146]
[MODULE=NONE]
[LAST_MAKEPROJ: 4/12/01 1:14:17 PM]

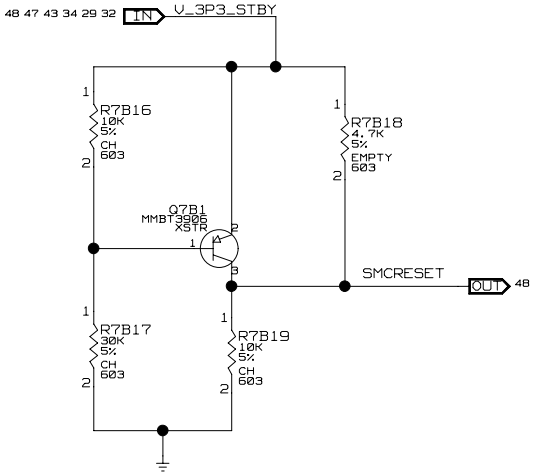
5V DRAIN



NV2A FAN HEADER



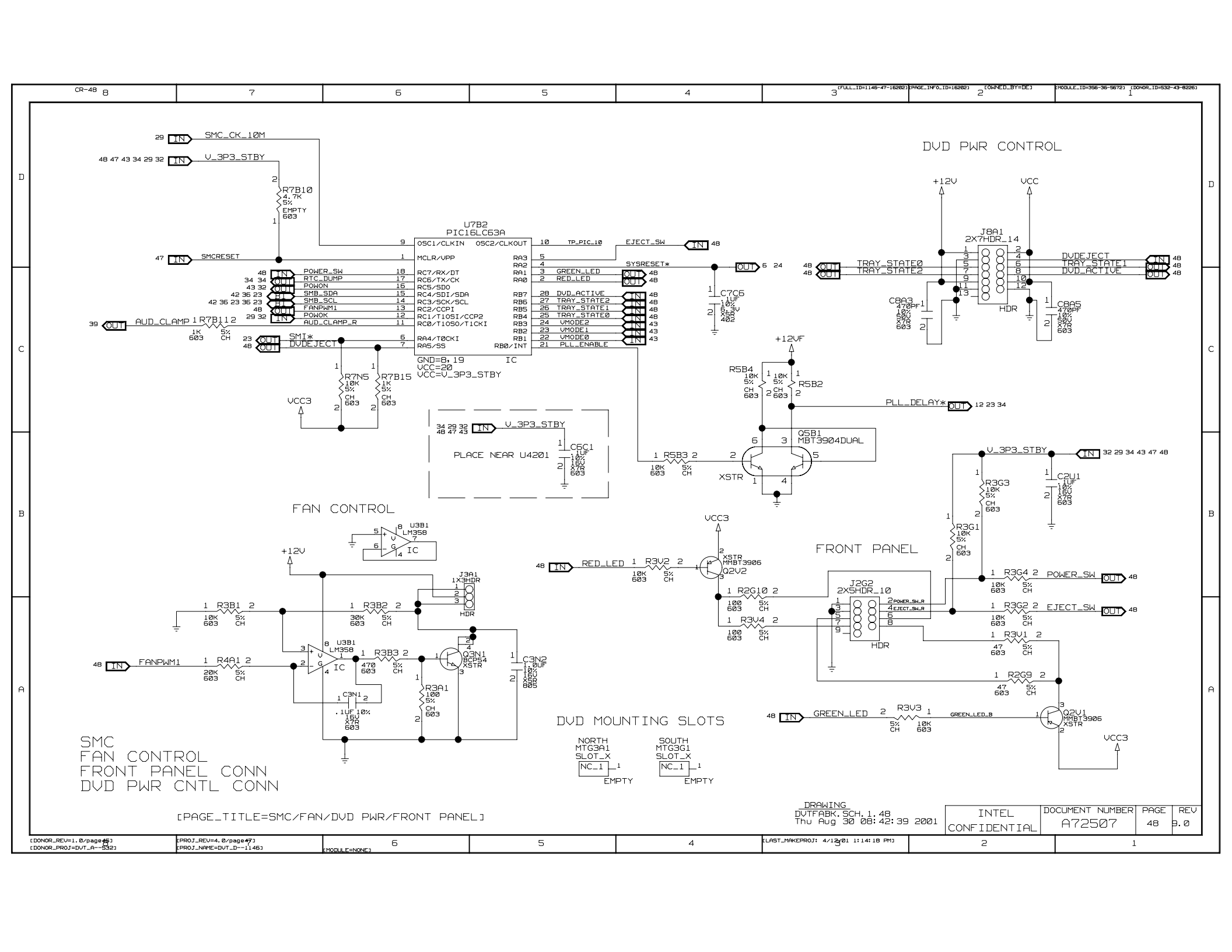
SMC BROWN OUT



[PAGE_TITLE=NV2A FAN/5V DRAIN/BROWN OUT]

DRAWING
DVTFABK.SCH.1.47
Thu Aug 30 08:42:36 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	47	9.0


DVD PWR CONTROL
FAN CONTROL
FRONT PANEL
DVD MOUNTING SLOTS
SMC_CK_10M
V_3P3_STBY
SMCRESET
POWER_SW
RTC_DUMP
POWON
SMB_SDA
SMB_SCL
FANPWM1
POWOK
AUD_CLAMP
SMI*
DVDEJECT
AUD_CLAMP_R
EJECT_SW
SYSRESET*
GREEN_LED
RED_LED
DVD_ACTIVE
TRAY_STATE2
TRAY_STATE1
TRAY_STATE0
VMODE2
VMODE1
VMODE0
PLL_ENABLE
TP_PIC_10
U7B2
PIC16LC63A
GND=8,19
VCC=20
VCC=V_3P3_STBY
PLACE NEAR U4201
PLL_DELAY*
Q5B1
MBT3904DUAL
XSTR
U3B1
LM358
IC
HDR
Q3N1
BCP54
Q2V2
MMBT3906
Q2V1
NORTH
MTG3A1
SLOT_X
SOUTH
MTG3G1
EMPTY
SMC
FAN CONTROL
FRONT PANEL CONN
DVD PWR CNTL CONN
[PAGE_TITLE=SMC/FAN/DVD PWR/FRONT PANEL]
DRAWING
DVTFABK.SCH.1.48
Thu Aug 30 08:42:39 2001
INTEL CONFIDENTIAL
DOCUMENT NUMBER
A72507
PAGE
48
REV
9.0

MCPX MUXED PIN ASSIGNMENT

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
A5	IDE_ADDR_S0	TRST0	Y20	PCI_AD0	XBUS_A23
E6	IDE_ADDR_S1	RESERVED	Y19	PCI_AD1	XBUS_A22
B5	IDE_ADDR_S2	TRST1	AA19	PCI_AD2	XBUS_A21
C5	IDE_CS1_S*	RESERVED	AB17	PCI_AD3	XBUS_A20
B4	IDE_CS3_S*	RESERVED	AA17	PCI_AD4	XBUS_OE*
A6	IDE_DACK_S*	TDI0	Y17	PCI_AD5	XBUS_WE*
B8	IDE_DATA_S0	TDO1	V17	PCI_AD6	RESERVED
C8	IDE_DATA_S1	RESERVED	AA16	PCI_AD7	XBUS_DQ7
D8	IDE_DATA_S2	RESERVED	V16	PCI_AD8	XBUS_A19
B9	IDE_DATA_S3	TCK1	AB15	PCI_AD9	XBUS_A14
D9	IDE_DATA_S4	RESERVED	AA15	PCI_AD10	XBUS_A15
B10	IDE_DATA_S5	TMS1	Y15	PCI_AD11	XBUS_DQ6
E10	IDE_DATA_S6	RESERVED	W15	PCI_AD12	XBUS_A16
B11	IDE_DATA_S7	TDE1*	V15	PCI_AD13	XBUS_A17
A11	IDE_DATA_S8	TDE0*	AB14	PCI_AD14	XBUS_DQ4
E11	IDE_DATA_S9	RESERVED	AA14	PCI_AD15	XBUS_A13
C10	IDE_DATA_S10	RESERVED	Y11	PCI_AD16	XBUS_DQ3
E9	IDE_DATA_S11	RESERVED	W11	PCI_AD17	XBUS_CE*
A9	IDE_DATA_S12	TMS0	V11	PCI_AD18	XBUS_A12
C9	IDE_DATA_S13	RESERVED	AA10	PCI_AD19	XBUS_A9
E8	IDE_DATA_S14	RESERVED	Y10	PCI_AD20	XBUS_DQ2
A8	IDE_DATA_S15	TCK0	V10	PCI_AD21	XBUS_A10
E7	IDE_DRQ_S	RESERVED	AB9	PCI_AD22	XBUS_A6
B6	IDE_INTR_S	TDI1	AA9	PCI_AD23	XBUS_DQ0
B7	IDE_IOR_S*	TDO0	W9	PCI_AD24	XBUS_DQ1
C7	IDE_IOW_S*	RESERVED	V9	PCI_AD25	XBUS_A8
C6	IDE_RDY_S	RESERVED	AA8	PCI_AD26	XBUS_A3
			Y8	PCI_AD27	XBUS_A4
			W8	PCI_AD28	XBUS_A0
Y21	PCI_GNT0*	RESERVED	V8	PCI_AD29	XBUS_A5
Y18	PCI_GNT1*	RESERVED	V7	PCI_AD30	XBUS_A2
AA13	PCI_GNT2*	RESERVED	V6	PCI_AD31	XBUS_A1

BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME	BALL LOCATION	MCP-1 SIGNAL NAME	MCPX SIGNAL NAME
Y7	PCI_GNT3*	RESERVED	Y16	PCI_CBE0*	XBUS_A18
Y6	PCI_GNT4*	RESERVED	W14	PCI_CBE1*	XBUS_DQ5
V12	PCI_IRDY*	RESERVED	AA11	PCI_CBE2*	XBUS_A11
Y14	PCI_PAR	RESERVED	Y9	PCI_CBE3*	XBUS_A7
Y13	PCI_PERR*	RESERVED	Y12	PCI_DEVSEL*	RESERVED
AA20	PCI_REQ0*	RESERVED	AB11	PCI_FRAME*	RESERVED
AA18	PCI_REQ1*	RESERVED	V14	PCI_SERR*	RESERVED
AA12	PCI_REQ2*	RESERVED	V13	PCI_STOP*	RESERVED
AA7	PCI_REQ3*	RESERVED	W12	PCI_TRDY*	RESERVED
AA6	PCI_REQ4*	RESERVED			

VOLTAGE RAILS

RAIL	TYPICAL(V)	
V_CPUCORE	1.7V (CPU DEPENDENT)	
VCC	5V	
VCC3	3.3V	
V_5P0_STBY	5V STANDBY	
V_3P3_STBY	3.3V STANDBY	
V_2P5	2.65V	
V_1P5_VTT	1.5V	
V_1P25_MEMVTT	1.25V	
V_1P5	1.65V	
V_AGP_VDDQ	1.5V	
V_0P75_AGPVREF	0.75V	
V_1P0_CPUGTLREF	1.0V	

[PAGE_TITLE=MCPX MUXED PIN ASSIGNMENT]

DRAWING
DVTFABK.SCH.1.49
Thu Aug 30 08:42:42 2001

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	A72507	49	9.0

*** Signal Cross-Reference ***
--- for the entire design --

9_V_REGULATED	41 40
10_BIAS	35
100_BIAS	35
AUD_5V_ANALOG	41 33 38
AUD_BCLK	38 23
AUD_BCLK_R	23
AUD_CK_24M	29 38
AUD_CK_24M_R	29
AUD_CLAMP	48 39
AUD_CLAMP_R	48
AUD_LINEOUT_L	40 43
AUD_LINEOUT_R	40 43
AUD_LINK_BCLK_CODEC_R	38
AUD_LINK_SDI_CODEC_R	38
AUD_RST*	23 38
AUD_SDI0	38 23
AUD_SDO	23 38
AUD_SYNC	23 38
AUD_TRANSIENT_CTRL	39
AUD_TR_CTRL_D1_P3B	39
AUD_TR_CTRL_D2_P3B	39
AUD_TR_CTRL_Q2_P3B	39
BGA2_BREQ0_C6	6
BIAS_L	41 40
BIAS_R	41 40
CK_H_133M_CPU	11 6
CK_H_133M_CPU_BUF	6
CK_H_133M_CPU_R	6
CK_H_133M_FB	11
CK_H_133M_FB_R	11
CK_H_PICCLK	11
CK_H_PICCLK_R	11 6
CLK_XTAL_X1	29
CLK_XTAL_X2	29
CSYNC	12 46
CSYNC_1	46
CSYNC_2	46
CSYNC_3	46
CSYNC_4	46
DACA_Y	42 43
DACA_Y_F	42
DACB_C	42 43
DACB_C_F	42
DACC_SCART	42 43
DACC_SCART_F	42
DACD_CVBS	42 43
DACD_CVBS_F	42
DVDEJECT	48
DVD_ACTIVE	48
DVO_ANALOG_VCC3	42
DVO_BLANK*	42
DVO_CLKO	42 12
DVO_CLKOR	42
DVO_CLK_IN	12 42
DVO_COMP	42
DVO_D<11..0>	12 13 42
DVO_DEFAULT	42
DVO_FIELD	42 12 23
DVO_FIELD_3P3*	23
DVO_FSADJ	42
DVO_FSADJ_R	42
DVO_HSYNC*	12 42
DVO_RESET_R*	42
DVO_VBIAS	42
DVO_VDD_VREFR	42
DVO_VREF	42
DVO_VSYNC*	12 42

EJECT_SW	48
EJECT_SW_R	48
FANPWM1	48
GREEN_LED	48
GREEN_LED_B	48
HD_R_PDD<15..0>	37
H_A#<31..3>	5 11
H_A20M*	24 5
H_A20M_R*	5
H_ADS*	6 11
H_BNR*	6 11
H_BPRI*	11 6
H_CPU_RST*	11 24
H_CPU_RST_R*	11 6
H_D#<63..0>	5 11
H_DBSY*	6 11
H_DEFER*	11 6
H_DRDY*	6 11
H_FERR*	5 24
H_HIT*	6 11
H_HITM*	6 11
H_IGNNE*	24 5
H_INIT*	6
H_INTR	24 6
H_INTR_R	6
H_LOCK*	6 11
H_NMI	24 6
H_NMI_R	6
H_PREQ*	10 5
H_REQ#<4..0>	6 11
H_RS#<2..0>	11 6
H_SMI*	6
H_SMI_R*	24 6
H_TCK	10 5
H_TDI	10 5
H_THERMN	7 36
H_THERMP	36 7
H_TMS	10 5
H_TRDY*	11 6
H_TRST*	10 5
H_VID_0	26
H_VID_1	26
H_VID_2	26
H_VID_3	26
IDE_CSEL	37
IDE_IRQ14_R	37
IDE_PDA<2..0>	23 37
IDE_PDA_R<2..0>	37
IDE_PDCS1*	23 37
IDE_PDCS1_R*	37
IDE_PDCS3*	23 37
IDE_PDCS3_R*	37
IDE_PDD<15..0>	23 37
IDE_PDDACK*	23 37
IDE_PDDACK_R*	37
IDE_PDDREQ	37 23
IDE_PDDREQ_R	37
IDE_PDIOR*	23 37
IDE_PDIOR_R*	37
IDE_PDIOW*	23 37
IDE_PDIOW_R*	37
IDE_PINTR	37 23
IDE_PIORDY	37 23
IDE_PRI_RST_R*	37
KBRSTIN*	24
LAN_CK_25M	29 35
LAN_CK_25M_R	29
LAN_CLK_2_5M_RX	35 23
LAN_CLK_2_5M_RX_R	35
LAN_CLK_2_5M_TX	35 23

LAN_CLK_2_5M_TX_R	35
LAN_CT	35 36
LAN_CT_R	36
LAN_MII_COL	35 23
LAN_MII_CRS	35 23
LAN_MII_CRS_R	35
LAN_MII_RX_DV	35 23
LAN_MII_RX_DV_R	35
LAN_MII_RX_ER	35 23
LAN_MII_RX_ER_R	35
LAN_MII_TX_EN	23 35
LAN_RD_N	36 35
LAN_RD_P	36 35
LAN_TD_N	35 36
LAN_TD_N_R	36
LAN_TD_P	35 36
LAN_TD_P_R	36
LDT_RESET*	12 24
LDT_RXD#<8..0>	24 12
LDT_RXD<8..0>	24 12
LDT_RX_CK	24 12
LDT_RX_CK*	24 12
LDT_TXD#<8..0>	12 24
LDT_TXD<8..0>	12 24
LDT_TX_CK	12 24
LDT_TX_CK*	12 24
LINE_OUT_L	38 40
LINE_OUT_R	38 40
LVLCNT0	23 43
LVLCNT1	23 42 43
L_AD<3..0>	23 25
L_FRAME*	23
L_SERIRQ	23
MCPX_TCK0	24 25
MCPX_TCK1	24 25
MCPX_TDE0	24 25
MCPX_TDE1	24 25
MCPX_TDI0	24 25
MCPX_TDI1	24 25
MCPX_TMS0	24 25
MCPX_TMS1	24 25
MCPX_TRST0	24 25
MCPX_TRST1	24 25
MCP_3P3_DELAY	23
MCP_VDD_PLL	23
MII_MDC	23 35
MII_MDIO	23 35
MII_RXD<3..0>	35 23
MII_TXD<3..0>	23 35
M_AB_CKE	14 15
M_A_ADDR<13..0>	11 14
M_A_CAS*	11 14
M_A_CLK	11 14
M_A_CLK*	11 14
M_A_CS#<1..0>	11 14
M_A_DATA<31..0>	11 14 18
M_A_DQM<3..0>	11 18 14
M_A_DQS	11 14 18
M_A_RAS*	11 14
M_A_WE*	11 14
M_B_ADDR<13..0>	11 15
M_B_CAS*	11 15
M_B_CLK	11 15
M_B_CLK*	11 15
M_B_CS#<1..0>	11 15
M_B_DATA<31..0>	11 15 18
M_B_DQM<3..0>	11 18 15
M_B_DQS	11 15 18
M_B_RAS*	11 15
M_B_WE*	11 15

M_CD_CKE	16 17
M_C_ADDR<13..0>	12 16
M_C_CAS*	12 16
M_C_CLK	12 16
M_C_CLK*	12 16
M_C_CS#<1..0>	12 16
M_C_DATA<31..0>	12 16 19
M_C_DQM<3..0>	12 19 16
M_C_DQS	12 16 19
M_C_RAS*	12 16
M_C_WE*	12 16
M_D_ADDR<13..0>	12 17
M_D_CAS*	12 17
M_D_CLK	12 17
M_D_CLK*	12 17
M_D_CS#<1..0>	12 17
M_D_DATA<31..0>	12 17 19
M_D_DQM<3..0>	12 19 17
M_D_DQS	12 17 19
M_D_RAS*	12 17
M_D_WE*	12 17
M_VREF_0	14 15
M_VREF_1	16 17 30
NB_CK_13P5M	29 11
NB_CK_13P5M_R	29
NV2A_3P3_DELAY	12
NV2A_INTA*	12 24
NV2A_TEST	12
NV2A_VREF_0	11
NV2A_VREF_1	12
OUTPUT_CLAMP_L	39 40
OUTPUT_CLAMP_R	39 40
P0AC	35 36
P0AC_R	36
P1CL	35 36
P2LI	35 36
P2LI_R	36
P3TD	35 36
P4RD	35 36
PCI_CLK	24 23
PCI_CLK_FB	24
PCI_FRAME	24 25
PCI_PULLUP	23 24
PCI_RESET*	25 12 14 16 23 35 37 42 46
PCI_RESET_B*	24 25
PICD0	6
PICD1	6
PLLVDD	12
PLL_DELAY*	48 12 23 34
PLL_ENABLE	48
POWER_SW	48
POWER_SW_R	48
POWOK	32 29 48
POWON	48 32 43
RED_LED	48
RGB_B	43
RGB_C	43
RGB_SELECT	43
RGB_SELECT*	23 43
ROM_A<19..0>	24 45
ROM_CE*	45
ROM_D<7..0>	24 45
ROM_OE*	24 45
ROM_OE_R*	45
ROM_WE*	24 45
ROM_WE_R*	45
RSET_NV2A*	12
RTC_DUMP	48 34
RTC_XI	23
RTC_XO	23

SB_CK_13P5M	29 23
SB_CK_13P5M_R	29
SC1102_DH_R	30
SC1102_OCSET	30
SC1102_PHASE	30
SC1102_VCC	30
SC1110_DH	30
SC1110_DL	30
SMB_SCL	23 36 48 23 36 42
SMB_SDA	23 36 42 48
SMCRESET	47 48
SMC_CK_10M	29 48
SMC_CK_10M_R	29
SMI*	48 23
SPDIF	23 43
SPDIF_R	43
SPKR_STRAP	23
STATUS	43
SYSRESET*	48 6 24
SYSRESET_R*	6
TP16_EN	26
TP_1032_4	36
TP_1032_6	36
TP_9709_5	38
TP_BGA2_A4	5
TP_BGA2_A5	5
TP_BGA2_AA1	6
TP_BGA2_AA17	7
TP_BGA2_AA21	5
TP_BGA2_AB1	6
TP_BGA2_AB19	7
TP_BGA2_AC17	7
TP_BGA2_AD9	5
TP_BGA2_AD20	7
TP_BGA2_B4	5
TP_BGA2_C5	5
TP_BGA2_E6	5
TP_BGA2_G4	7
TP_BGA2_H4	7
TP_BGA2_P20	6
TP_BGA2_P21	6
TP_BGA2_R2	7
TP_BGA2_R21	6
TP_BGA2_T21	6
TP_BGA2_U19	6
TP_BGA2_U21	6
TP_BGA2_V18	6
TP_BGA2_V20	6
TP_BGA2_V21	5
TP_BGA2_W2	6
TP_BGA2_W19	5
TP_BGA2_W21	5
TP_BGA2_Y1	6
TP_BGA2_Y2	6
TP_BGA2_Y21	5
TP_BUF24M	24
TP_CPURSV0	11
TP_CPURSV1	11
TP_ICS_4	29
TP_ICS_7	29
TP_ICS_9	29
TP_INIT*	24
TP_MCPX_AA19	24
TP_MCPX_AB17	24
TP_MCPX_G18	23
TP_MCPX_G20	23
TP_MCPX_H18	23
TP_MCPX_H21	23
TP_MCPX_TDO0	24
TP_MCPX_TDO1	24

TP_MCPX_Y2	23
TP_MCPX_Y6	23
TP_MCPX_Y19	24
TP_MCPX_Y20	24
TP_PIC_10	48
TP_PRIIDE_32	37
TP_PRIIDE_34	37
TP_PRIIDE_39	37
TP_REF6	26
TP_ROM_CE*	24
TP_RY_BY	45
TP_SC1110_4	30
TP_SC1110_14	30
TRAY_STATE0	48
TRAY_STATE1	48
TRAY_STATE2	48
USBPWR_1	46
USBPWR_2	46
USBPWR_3	46
USBPWR_4	46
USB_1	23 46
USB_1*	23 46
USB_1FB	46
USB_1FB*	46
USB_1R	46
USB_1R*	46
USB_2	23 46
USB_2*	23 46
USB_2FB	46
USB_2FB*	46
USB_2R	46
USB_2R*	46
USB_3	23 46
USB_3*	23 46
USB_3FB	46
USB_3FB*	46
USB_3R	46
USB_3R*	46
USB_4	23 46
USB_4*	23 46
USB_4FB	46
USB_4FB*	46
USB_4R	46
USB_4R*	46
USB_5	23 25
USB_5*	23 25
USB_VREF	23
VID_CK_13P5M	29 42
VID_CK_13P5M_R	29
VMODE0	43 48
VMODE0_R	43
VMODE1	43 48
VMODE1_R	43
VMODE2	43 48
VMODE2_R	43
VREG_1P5_GATE	26 31
VREG_2P5_GATE	26 31
VREG_CSN	26
VREG_CSP	26
VREG_CSP_R	26
VREG_FETDRVA	26
VREG_FETDRVA_FETDRVB_PN1	26
VREG_FETDRVB	26
VREG_PVCC	26
VREG_VCC	26
VREG_VCCP_R	26
VREG_VO_SENSE	26
V_1P5	28 12 22 24 28 34
V_1P5_VTT	31 5 6 7 9 10 11 22 24 26 42
V_1P25_MEMVTT	30 18 19 20

V_2P5	31 7 11 12 14 15 16 17 20 21 22 26 28
V_3P3_FB	29
V_3P3_STBY	32 29 34 43 47 48
V_5P0_FILTERED	28 30 32
V_BAT_RTC	34 23
V_BAT_RTC_FET	34
V_CLKREF	7
V_CPUCORE	26 7 8 27
V_DVO_FB	42 12 13 42
V_DVO_REF	12
V_GTLREF	7
V_GTLREF_1P0	11
V_GTLREF_MCP	24
V_LAN_3P3V	35 36

*** Unit Cross-Reference ***
--- for the entire design --

C1C2	CAPN	7
C1D1	CAPN	22
C1D2	CAPN	7
C1D3	CAPN	6
C1D4	CAPN	7
C1D5	CAPN	6
C1E1	CAP-P	27
C1F1	CAPN	26
C1F2	CAPN	26
C1G1	CAP-P	26
C1G2	CAPN	26
C1G3	CAP-P	46
C1G4	CAPN	46
C1G5	CAP-P	46
C1G6	CAPN	46
C1G7	CAPN	46
C1G8	CAPN	46
C1P1	CAPN	8
C1P2	CAPN	27
C1P3	CAPN	8
C1P4	CAPN	27
C1P5	CAPN	8
C1P6	CAPN	7
C1P7	CAPN	9
C1P8	CAPN	9
C1P9	CAPN	8
C1P10	CAPN	9
C1P11	CAPN	9
C1P12	CAPN	7
C1R1	CAPN	8
C1R2	CAPN	8
C1R3	CAPN	27
C1R4	CAPN	27
C1R5	CAPN	8
C1R6	CAPN	8
C1R7	CAPN	7
C1R8	CAPN	7
C1R9	CAPN	9
C1T1	CAPN	33
C1U1	CAPN	26
C2D1	CAPN	26
C2D2	CAPN	26
C2D3	CAPN	26
C2E1	CAP-P	27
C2E2	CAP-P	27
C2E3	CAPN	32
C2E4	CAPN	32
C2E5	CAP-P	27
C2E6	CAPN	26
C2E7	CAPN	26
C2F1	CAPN	32
C2F2	CAPN	32
C2F3	CAP-P	26
C2G1	CAPN	32
C2G2	CAPPDFPN	32
C2G3	CAPN	32
C2G4	CAPN	46
C2G5	CAPN	46
C2G6	CAPN	46
C2G7	CAPN	46
C2G8	CAPN	46
C2G9	CAPN	46
C2N1	CAP-P	31
C2N2	CAP-P	31
C2P1	CAPN	7
C2P2	CAPN	9
C2P3	CAPN	9
C2P4	CAPN	9
C2P5	CAPN	9
C2P6	CAPN	9
C2P7	CAPN	8
C2P8	CAPN	8
C2P9	CAPN	8
C2P10	CAPN	8
C2P11	CAPN	8
C2P12	CAPN	8
C2P13	CAPN	9
C2P14	CAPN	9
C2P15	CAPN	8
C2P16	CAPN	8
C2P17	CAPN	8
C2P18	CAPN	8
C2P19	CAPN	8
C2P20	CAPN	8
C2P21	CAPN	8
C2P22	CAPN	8
C2P23	CAPN	8
C2P24	CAPN	9
C2R1	CAPN	9
C2R2	CAPN	9
C2R3	CAPN	9
C2R4	CAPN	9
C2R5	CAP-P	7
C2R6	CAPN	26
C2R7	CAPN	11
C2T1	CAPN	26
C2T2	CAPN	33
C2U1	CAPN	48
C3A1	CAPN	33
C3B1	CAPPDFPN	31
C3B2	CAPN	31
C3B3	CAPN	31
C3B4	CAPN	31
C3B5	CAPN	31
C3B6	CAPN	11
C3B7	CAPN	22
C3C1	XCAP	6
C3C2	XCAP	6
C3E1	CAPN	20
C3E2	CAP-P	27
C3E3	XCAP	20
C3E4	CAPN	20
C3E5	XCAP	20
C3E6	XCAP	21
C3E7	XCAP	21
C3E8	XCAP	21
C3E9	XCAP	21
C3F1	XCAP	20
C3F2	CAPPDFPN	32
C3F3	XCAP	20
C3F4	CAPN	32
C3F5	CAPN	32
C3F6	CAPPDFPN	31
C3F7	CAPN	32
C3F8	XCAP	21
C3F9	XCAP	21
C3G1	CAPN	32
C3G2	CAPN	32
C3G3	CAPN	32
C3G4	CAPPDFPN	32
C3G5	CAPN	26
C3G6	CAPN	32
C3G7	CAPN	26
C3G8	CAPN	32
C3G9	CAPN	46
C3N1	CAPN	48
C3N2	CAPN	48
C3N3	CAPN	31
C3P1	CAPN	22
C3P2	CAPN	22
C3P3	CAPN	11
C3P4	CAPN	12
C3P5	CAPN	12
C3R2	XCAP	20
C3R3	CAPN	11
C3T1	XCAP	20
C3T2	XCAP	20
C3T3	XCAP	21
C3U1	XCAP	20
C3U2	XCAP	21
C3V1	CAPN	30
C3V2	CAPN	30
C3V3	CAPN	30
C3V4	CAPN	32
C4A1	CAPN	42
C4A2	CAPN	42
C4A3	CAPN	42
C4A4	CAPN	43
C4B1	CAPN	42
C4B2	CAPN	31
C4B3	CAPN	31
C4B4	CAPN	12
C4E1	XCAP	20
C4E2	XCAP	20
C4E3	XCAP	20
C4E4	XCAP	20
C4E5	XCAP	21
C4E6	XCAP	21
C4E7	XCAP	21
C4E8	XCAP	21
C4F1	XCAP	20
C4F2	XCAP	21
C4F3	XCAP	20
C4F4	XCAP	21
C4F5	XCAP	21
C4F6	XCAP	21
C4F7	XCAP	21
C4G1	CAPN	30
C4G2	CAPN	30
C4G3	CAP-P	46
C4G4	CAPN	46
C4G5	CAPN	46
C4G6	CAP-P	46
C4G7	CAPN	46
C4G8	CAPN	46
C4G9	CAPN	46
C4G10	CAPN	46
C4G11	CAPN	46
C4G12	CAPN	46
C4M1	CAPN	43
C4M2	XCAP	42
C4M3	XCAP	42
C4M4	XCAP	42
C4M5	CAPN	42
C4M6	CAPN	42
C4M7	CAPN	42
C4M8	CAPN	42
C4M9	CAPN	42
C4M10	CAPN	42
C4M11	CAPN	42
C4M12	CAPN	42
C4M13	CAPN	42
C4M14	CAPN	42
C4M15	CAPN	42
C4M16	CAPN	42
C4M17	CAPN	42
C4M18	CAPN	42
C4M19	CAPN	42
C4M20	CAPN	42
C4M21	CAPN	42
C4M22	XCAP	42
C4N2	CAPN	42
C4N3	CAPN	42
C4N4	CAPN	42
C4N5	CAPN	42
C4N6	CAPN	42
C4N7	CAPN	31
C4N8	CAPN	31
C4N9	CAPN	42
C4N10	CAPN	42
C4N11	CAPN	42
C4N12	CAPN	42
C4P1	XCAP	20
C4P2	CAPN	12
C4P3	CAPN	22
C4P4	CAPN	22
C4P5	CAPN	22
C4P6	CAPN	22
C4P7	CAPN	22
C4P8	CAPN	22
C4P9	CAPN	22
C4P10	CAPN	22
C4P11	CAPN	33
C4P12	CAPN	22
C4P13	CAPN	11
C4P14	CAPN	22
C4P15	CAPN	22
C4P16	CAPN	22
C4P17	XCAP	22
C4P18	XCAP	22
C4P19	XCAP	22
C4P20	CAP-P	22
C4P21	XCAP	22
C4R1	CAPN	22
C4R2	CAPN	22
C4R3	CAPN	22
C4R4	CAPN	22
C4R5	CAPN	11
C4R6	CAPN	22
C4R7	CAPN	22
C4R8	CAPN	22
C4R9	CAPN	22
C4R10	CAPN	22
C4R11	CAPN	22
C4R12	CAPN	22
C4R13	CAPN	22
C4R14	XCAP	12
C4R15	XCAP	20
C4R16	XCAP	22
C4R17	CAPN	22
C4R18	XCAP	22
C4R19	XCAP	22
C4R20	XCAP	22
C4R21	XCAP	22
C4T1	XCAP	20
C4T2	XCAP	20
C4T3	XCAP	20
C4T4	XCAP	20
C4T5	XCAP	21
C4T6	XCAP	21
C4U1	XCAP	20
C4U2	XCAP	20
C4U3	CAPN	17
C4U4	CAP-P	30
C4U5	CAP-P	30
C4U6	CAP-P	30
C4U7	CAP-P	30

C4U8	XCAP	21
C4U9	XCAP	21
C4U10	XCAP	21
C4U11	XCAP	21
C4V1	CAPN	30
C4V2	CAPN	32
C4V3	CAPN	46
C5A1	CAPN	40
C5A2	CAPN	40
C5A3	CAP-P	41
C5A4	CAP-P	39
C5A5	CAP-P	39
C5A7	CAPN	33
C5A8	XCAP	43
C5B1	CAPN	41
C5B2	CAPN	20
C5B3	XCAP	21
C5B4	XCAP	21
C5C1	CAPN	20
C5C2	XCAP	20
C5C3	XCAP	20
C5C4	XCAP	21
C5C5	XCAP	21
C5C6	XCAP	21
C5D1	CAPN	20
C5D2	CAPN	20
C5D3	XCAP	20
C5D4	XCAP	21
C5D5	XCAP	20
C5E1	CAPN	20
C5E2	CAPN	20
C5E3	CAPN	23
C5E4	XCAP	20
C5E5	XCAP	20
C5E6	XCAP	21
C5F1	CAPN	16
C5F2	CAPN	16
C5F4	CAPN	16
C5F5	CAPPDFPN	31
C5F6	CAPPDFPN	31
C5F7	XCAP	21
C5G1	CAPPDFPN	31
C5G2	CAPN	31
C5G3	CAPN	30
C5G4	CAPN	31
C5G5	CAPN	31
C5G7	CAPN	30
C5M1	CAPN	43
C5M2	CAPN	43
C5M3	CAP-P	42
C5M4	CAPN	41
C5M5	CAPN	41
C5M6	CAPN	40
C5N1	CAPN	41
C5N2	CAPN	41
C5N3	CAPN	41
C5N4	XCAP	20
C5N5	XCAP	20
C5N6	XCAP	20
C5N7	XCAP	21
C5N8	XCAP	21
C5P1	XCAP	20
C5P2	XCAP	11
C5P3	XCAP	20
C5P4	XCAP	20
C5P5	XCAP	20
C5P6	XCAP	20
C5P7	XCAP	21
C5R1	XCAP	20
C5R2	XCAP	21

C5T1	CAPN	22
C5T2	XCAP	20
C5T3	XCAP	20
C5T4	XCAP	20
C5T5	XCAP	21
C5T6	XCAP	21
C5T7	XCAP	21
C5T8	XCAP	21
C5U1	XCAP	20
C5U2	XCAP	20
C5U4	XCAP	21
C5V1	CAPN	30
C6A2	CAPN	33
C6A3	CAP-P	41
C6A4	CAP-P	38
C6A6	CAPN	40
C6A7	CAPN	38
C6A8	CAPN	38
C6A9	CAPN	40
C6A10	CAPN	38
C6A11	CAP-P	40
C6A12	CAP-P	40
C6A13	CAPN	40
C6A14	CAPN	47
C6B1	CAPN	40
C6B2	CAPN	40
C6B3	CAPN	38
C6B4	CAP-P	40
C6B5	CAPN	38
C6B6	CAP-P	40
C6B7	XCAP	20
C6B8	XCAP	20
C6B9	CAP-P	20
C6B10	XCAP	21
C6B11	XCAP	21
C6C1	CAPN	48
C6C2	CAPN	14
C6C3	CAPN	14
C6C4	CAPN	14
C6C5	XCAP	20
C6C6	XCAP	20
C6C7	XCAP	20
C6C8	XCAP	20
C6C9	XCAP	21
C6C10	XCAP	21
C6C11	XCAP	21
C6C12	XCAP	21
C6C13	XCAP	21
C6D1	XCAP	20
C6D2	XCAP	20
C6D3	CAPN	15
C6D4	XCAP	21
C6D5	XCAP	21
C6D6	XCAP	21
C6D7	XCAP	21
C6D8	XCAP	21
C6E1	CAPN	23
C6E2	CAP-P	23
C6E3	CAPN	33
C6E4	CAPN	23
C6E5	CAPN	23
C6F1	CAPN	36
C6F2	CAPN	36
C6F3	CAPN	33
C6F4	CAPN	24
C6F5	CAPN	24
C6F6	CAPN	34
C6G1	CAPPDFPN	33
C6G2	CAPPDFPN	31
C6G3	CAPN	31

C6G4	CAPN	31
C6G5	CAPN	31
C6G6	CAPPDFPN	31
C6M1	CAPN	43
C6M2	CAPN	40
C6M3	CAPN	40
C6M4	CAPN	38
C6M5	CAPN	38
C6N1	CAPN	40
C6N2	XCAP	20
C6N3	XCAP	20
C6N4	CAPN	20
C6N5	XCAP	21
C6N6	XCAP	21
C6N7	XCAP	21
C6N8	XCAP	21
C6P1	XCAP	20
C6P2	XCAP	20
C6P3	XCAP	20
C6P4	XCAP	20
C6P5	CAPN	20
C6P6	CAPN	15
C6P7	XCAP	21
C6P8	XCAP	21
C6P9	XCAP	21
C6R1	XCAP	20
C6R2	XCAP	20
C6R3	CAP-P	20
C6R4	CAPN	24
C6R5	XCAP	21
C6R6	XCAP	21
C6T1	CAPN	22
C6T2	CAPN	22
C6T3	CAPN	22
C6T4	CAPN	22
C6T5	CAPN	22
C6T6	CAPN	34
C6T7	CAPN	24
C6V1	CAPN	32
C6V2	CAPN	32
C7A2	CAPN	36
C7A3	CAPN	35
C7A4	CAPN	35
C7B1	CAPN	35
C7B3	CAP-P	35
C7B4	CAPN	33
C7B6	CAPN	33
C7B7	CAPPDFPN	33
C7B8	CAPN	35
C7B9	CAPN	35
C7C1	CAPN	29
C7C2	CAPN	29
C7C3	CAP-P	29
C7C4	CAPN	29
C7C5	CAPN	29
C7C6	XCAP	48
C7C7	XCAP	29
C7D1	CAPN	33
C7D2	CAPN	33
C7D3	CAPN	33
C7E1	CAPN	33
C7G1	CAP-P	28
C7G2	CAPN	30
C7G3	CAPN	30
C7G4	CAPN	30
C7G5	CAPPDFPN	33
C7G6	CAPN	33
C7G7	CAPN	28
C7G8	CAPN	28
C7G9	CAP-P	34

C7G10	CAP-P	34
C7M1	CAPN	36
C7N1	CAPN	29
C7N2	CAPN	29
C7P1	CAPN	29
C7P2	CAPN	29
C7P3	CAPN	29
C7P4	CAPN	29
C7P5	CAPN	29
C7P6	CAPN	29
C7P7	CAPN	33
C7P8	CAPN	29
C7P9	CAPN	29
C7P10	CAPN	29
C7R1	CAPN	33
C7R2	XCAP	23
C7R3	XCAP	24
C7T1	CAP-P	28
C7T2	CAPN	28
C7T3	CAPN	23
C7T4	CAP-P	28
C8A1	CAPN	33
C8A2	CAPN	33
C8A3	CAPN	48
C8A4	CAPN	33
C8A5	CAPN	48
C8A6	CAPN	36
C8B1	CAPN	35
C8B2	CAPN	35
C8B3	CAPN	35
C8B4	CAPN	37
C8B5	XCAP	35
C8C1	CAPN	33
C8C2	CAPN	37
C8C5	CAPN	33
C8E1	CAPN	28
C8E2	CAPN	33
C8E3	CAPN	28
C8E4	CAPPDFPN	33
C8E5	CAPN	28
C8E6	CAPN	28
C8F1	CAPN	33
C8F2	CAP-P	28
C8G1	CAP-P	28
C8N1	CAPN	35
C8P1	CAPN	29
C8P2	CAPN	32
C8R1	CAPN	32
C8R2	CAPN	33
C8T1	CAP-P	28
C8T2	CAP-P	28
CR4M1	DIOSOT23S	42
CR4M2	DIOSOT23S	42
CR4M3	DIOSOT23S	42
CR4M4	DIOSOT23S	42
CR5A1	DIOSOT23S	39
CR5M1	DIOSOT23A	41
CR6F1	DIODE	34
CR7A1	DIOSOT23S	43
CR7F1	DIODE	34
CR7F2	DIODE	34
CR7F3	DIODE	34
DB3B1	X_DBPAD	31
DB3E1	X_DBPAD	26
DB3F1	X_DBPAD	30
DB6F1	X_DBPAD	31
DB6F2	X_DBPAD	34
DB8E1	X_DBPAD	28
FB3B1	FERR_BD	42
FB4M1	FERR_BD	42

```
FB4P1 FERRITE   12
FB5A1 FERR_BD   40
FB5A2 FERR_BD   40
FB6E1 FERRITE   23
FB7A1 FERRITE   41
FB7A2 FERRITE   35
FB8C1 FERRITE   29
FP2G1 LPAK4L    46
FP5G1 LPAK4L    46
J1G1  2X6HDR    46
J2G1  1X12PWR   32
J2G2  2X5HDR10  48
J3A1  1X3HDR    48
J4G1  2X6HDR    46
J5A1  24P_AV_BEC 43
J6A1  1X3HDR    47
J7D1  2X8HDR4   23
J8A1  2X7HDR14  48
J8C1  2X20HDR20 37
JA7A1 RJ45_2LED_TABUP 36
L1F1  INDUCTOR  26
L1G1  INDUCTOR  26
L1R1  INDUCTOR  7
L4A1  INDUCTOR  42
L4A2  INDUCTOR  42
L4A3  INDUCTOR  42
L4A4  INDUCTOR  42
L5G1  INDUCTOR  30
L7F1  INDUCTOR  28
L7G1  INDUCTOR  28
L7M1  INDUCTOR  36
L7N1  INDUCTOR  36
LBBD1 LABEL     44
MTG1B1 MTGCNR_2_7 44
MTG1E1 STD_MTG_EDGE 44
MTG1F1 STD_MTG_EDGE 44
MTG3A1 SLOT_X    48
MTG3G1 SLOT_X    48
MTG4B1 STD_MTG_HOLE 44
MTG4E1 STD_MTG_HOLE 44
MTG6F1 STD_MTG_HOLE 44
MTG7C1 STD_MTG_HOLE 44
MTG8A1 STD_MTG_HOLE 44
MTG8G1 STD_MTG_HOLE 44
Q1F1  FET_VREG  26
Q2U1  FET_VREG  26
Q2V1  PNP       48
Q2V2  PNP       48
Q3F1  FET_VREG  30
Q3F2  NPN       23
Q3N1  BCP54     48
Q4G1  FET_VREG  30
Q5A1  NPN       39
Q5A2  NPN       39
Q5A3  NPN       39
Q5A4  PNP       39
Q5B1  MBT3904DUAL 48
Q5F1  MBT3904DUAL 16
Q5M2  NPN       41
Q5N1  NPN       41
Q5N2  FET       12
Q5N3  FET       42
Q6A1  PNP       43
Q6C1  MBT3904DUAL 14
Q6F1  FET       23
Q7A1  NPN       47
Q7A2  NPN       47
Q7B1  PNP       47
Q7E1  MBT3904DUAL 43
Q7F1  FET_VREG  28
```

```
Q7F2  PNP       34
Q7F3  PNP       34
Q7G1  NPN       34
Q7N1  NPN       42
Q7R1  MBT3904DUAL 25
Q7U1  FET       34
Q8E1  FET       34
Q8E2  NPN       28
Q8E3  PNP       28
R1B1  RESN      10
R1B2  RESN      10
R1B3  RESN      10
R1C1  RESN      6
R1C2  RESN      6
R1C3  RESN      7
R1C4  RESN      7
R1C5  RESN      6
R1C6  RESN      6
R1C7  RESN      7
R1C8  RESN      5
R1C9  RESN      6
R1C10 RESN      7
R1C11 RESN      5
R1C12 RESN      6
R1C13 RESN      5
R1C14 RESN      6
R1C15 RESN      6
R1C18 RESN      6
R1C19 RESN      6
R1D1  RESN      7
R1D2  RESN      7
R1D3  RESN      7
R1D4  RESN      6
R1D5  RESN      7
R1D6  RESN      6
R1D7  RESN      7
R1D8  RESN      7
R1D9  RESN      6
R1D10 RESN      6
R1E1  RESN      26
R1F1  RESN      26
R1G1  RESN      46
R1P1  RESN      7
R1P2  RESN      5
R1R1  RESN      26
R1U1  RESN      26
R2B1  RESN      10
R2D1  RESN      6
R2D2  RESN      26
R2D3  RESN      26
R2D4  RESN      26
R2D5  RESN      26
R2D6  RESN      26
R2D7  RESN      26
R2E1  RESN      26
R2E2  RESN      26
R2E3  RESN      26
R2E4  RESN      26
R2E5  RESN      26
R2E6  RESN      26
R2E7  RESN      26
R2G1  RESN      46
R2G2  RESN      46
R2G3  RESN      46
R2G4  RESN      46
R2G5  RESN      46
R2G6  RESN      46
R2G7  RESN      46
R2G8  RESN      46
R2G9  RESN      48
```

```
R2G10 RESN      48
R2G11 RESN      46
R2R1  RESN      26
R2R2  RESN      26
R2U1  RESN      26
R3A1  RESN      48
R3B1  RESN      48
R3B2  RESN      48
R3B3  RESN      48
R3B4  RESN      11
R3B5  RESN      31
R3C1  XRES      6
R3F1  RESN      30
R3F2  RESN      23
R3F3  RESN      23
R3G1  RESN      48
R3G2  RESN      48
R3G3  RESN      48
R3G4  RESN      48
R3P1  RESN      11
R3P2  RESN      11
R3R3  RESN      11
R3R4  XRES      6
R3R5  XRES      6
R3R6  RESN      11
R3U1  RESN      17
R3V1  RESN      48
R3V2  RESN      48
R3V3  RESN      48
R3V4  RESN      48
R4A1  RESN      48
R4A2  RESN      42
R4B1  RESN      42
R4B2  RESN      42
R4B3  RESN      42
R4B4  RESN      12
R4B5  RESN      13
R4B6  RESN      12
R4B7  RESN      13
R4B8  RESN      13
R4B9  RESN      13
R4B10 RESN      13
R4B11 RESN      13
R4B12 RESN      13
R4B13 RESN      13
R4F1  RESN      16
R4G1  RESN      30
R4G2  RESN      30
R4G3  RESN      30
R4G4  RESN      30
R4G5  RESN      46
R4G6  RESN      46
R4M3  RESN      42
R4M4  RESN      42
R4M5  RESN      42
R4M6  RESN      42
R4M7  RESN      42
R4N1  RESN      42
R4N2  RESN      42
R4N5  RESN      42
R4N6  RESN      13
R4N7  RESN      13
R4N8  RESN      13
R4N9  RESN      13
R4N10 RESN      13
R4N11 RESN      13
R4N12 RESN      13
R4N13 RESN      13
R4R1  RESN      12
R4R3  XRES      12
```

```
R4R4  XRES      12
R4V1  RESN      30
R5A1  RESN      40
R5A2  RESN      40
R5A3  RESN      40
R5A4  RESN      40
R5A5  RESN      39
R5A6  RESN      39
R5A7  RESN      39
R5B1  RESN      39
R5B2  RESN      48
R5B3  RESN      48
R5B4  RESN      48
R5F1  RESN      16
R5F2  RESN      16
R5F3  RESN      16
R5F4  RESN      16
R5F5  RESN      16
R5G1  RESN      46
R5G2  RESN      46
R5G3  RESN      46
R5G4  RESN      46
R5G5  RESN      46
R5G6  RESN      46
R5G7  RESN      46
R5G8  RESN      46
R5G9  RESN      31
R5M5  RESN      40
R5M6  RESN      41
R5M7  RESN      41
R5M8  RESN      41
R5M9  RESN      41
R5M10 RESN      43
R5N1  RESN      41
R5N2  RESN      40
R5N3  RESN      41
R5N4  RESN      40
R5N5  RESN      41
R5N7  RESN      12
R5N8  RESN      12
R5P3  XRES      11
R5P4  XRES      11
R5R1  RESN      12
R6A1  RESN      40
R6A2  RESN      25
R6A3  RESN      40
R6A4  RESN      47
R6A5  RESN      43
R6A6  RESN      43
R6B1  RESN      40
R6B2  RESN      38
R6B3  RESN      40
R6B4  RESN      40
R6B5  RESN      38
R6B6  RESN      38
R6B7  RESN      38
R6B8  RESN      14
R6C1  RESN      14
R6C2  RESN      14
R6C3  RESN      14
R6C4  RESN      14
R6C5  RESN      14
R6C6  RESN      15
R6D1  XRES      23
R6D3  XRES      24
R6E1  RESN      24
R6E2  RESN      23
R6E3  XRES      25
R6E4  XRES      25
R6E5  XRES      25
```

R6F1	RESN	37
R6F2	XRES	34
R6F4	RESN	24
R6F5	RESN	24
R6F6	XRES	25
R6F7	XRES	25
R6F8	XRES	25
R6M1	RESN	23
R6M2	RESN	41
R6M3	RESN	41
R6N1	RESN	40
R6R1	XRES	25
R6T1	RESN	11
R6T2	RESN	37
R6T3	XRES	23
R6U1	RESN	37
R6U2	RESN	23
R6U3	RESN	23
R7A1	RESN	25
R7A2	RESN	47
R7A3	RESN	47
R7A4	RESN	47
R7A5	RESN	43
R7B1	RESN	36
R7B2	RESN	36
R7B3	RESN	36
R7B4	RESN	36
R7B5	RESN	36
R7B6	RESN	36
R7B7	RESN	36
R7B8	RESN	23
R7B9	RESN	35
R7B10	RESN	48
R7B11	RESN	48
R7B12	RESN	43
R7B13	RESN	43
R7B14	RESN	43
R7B15	RESN	48
R7B16	RESN	47
R7B17	RESN	47
R7B18	RESN	47
R7B19	RESN	47
R7B20	RESN	42
R7C1	RESN	36
R7C2	RESN	29
R7C3	RESN	29
R7C4	RESN	29
R7C5	RESN	29
R7C6	RESN	29
R7C7	XRES	29
R7C8	XRES	29
R7C9	RESN	29
R7D1	RESN	45
R7D2	XRES	45
R7D3	XRES	45
R7D4	XRES	25
R7D5	XRES	25
R7D6	XRES	25
R7E1	RESN	43
R7E2	RESN	23
R7E3	RESN	23
R7E4	RESN	43
R7E5	RESN	23
R7E6	RESN	23
R7E7	RESN	23
R7E8	RESN	24
R7E9	RESN	24
R7E10	RESN	23
R7F1	RESN	28
R7F2	XRES	25

R7F3	XRES	25
R7F4	XRES	25
R7F5	XRES	25
R7F6	RESN	34
R7F7	RESN	34
R7G1	RESN	34
R7G2	RESN	34
R7G3	RESN	34
R7M1	RESN	36
R7M2	RESN	36
R7M3	RESN	36
R7M4	RESN	43
R7N1	RESN	43
R7N2	RESN	43
R7N3	RESN	43
R7N4	RESN	29
R7N5	RESN	48
R7N6	RESN	36
R7N7	RESN	42
R7N8	RESN	42
R7P1	RESN	29
R7R1	RESN	45
R7R2	RESN	23
R7R3	XRES	45
R7R4	XRES	45
R7R5	RESN	25
R7R7	RESN	24
R7R8	XRES	25
R7R9	XRES	25
R7R10	XRES	23
R7T1	RESN	43
R7T2	RESN	43
R7T3	RESN	43
R7T4	XRES	25
R7U1	RESN	34
R7U2	RESN	34
R7U5	RESN	34
R7U6	RESN	34
R7U7	RESN	34
R7U8	RESN	34
R7U9	RESN	34
R7U10	RESN	34
R7U11	RESN	34
R7U12	XRES	34
R7U13	RESN	34
R7U14	RESN	34
R8A1	RESN	35
R8A2	RESN	35
R8B1	RESN	36
R8B2	RESN	35
R8B4	RESN	23
R8B5	RESN	37
R8B6	RESN	35
R8C1	RESN	37
R8C2	RESN	37
R8C3	RESN	37
R8C4	RESN	37
R8D1	RESN	37
R8E1	RESN	28
R8E2	RESN	28
R8E3	RESN	28
R8E4	RESN	28
R8E5	RESN	23
R8E6	RESN	23
R8E7	RESN	28
R8E8	RESN	28
R8E9	RESN	28
R8E10	RESN	28
R8E11	RESN	28
R8E12	RESN	28

R8N2	RESN	23
R8N3	RESN	37
R8N4	RESN	23
R8N5	RESN	23
R2416	GND_ISOLATION	26
R2417	GND_ISOLATION	26
R2418	GND_ISOLATION	26
RP3E1	RPAK4C-4R	18 19
RP3E2	RPAK4C-4R	18 19
RP3E3	RPAK4C-4R	19
RP3F1	RPAK4C-4R	19
RP3F2	RPAK4C-4R	19
RP4E1	RPAK4C-4R	19
RP4E2	RPAK4C-4R	18 19
RP4E3	RPAK4C-4R	19
RP4F1	RPAK4C-4R	19
RP4F2	RPAK4C-4R	19
RP4T1	RPAK4C-4R	19
RP4T2	RPAK4C-4R	18 19
RP4T3	RPAK4C-4R	19
RP4T4	RPAK4C-4R	19
RP4U1	RPAK4C-4R	19
RP5C1	RPAK4C-4R	18
RP5C2	RPAK4C-4R	18
RP5D1	RPAK4C-4R	18
RP5D2	RPAK4C-4R	18
RP5N1	RPAK4C-4R	18
RP5N2	RPAK4C-4R	18
RP5P1	RPAK4C-4R	18
RP5P2	RPAK4C-4R	18
RP5T1	RPAK4C-4R	19
RP5T2	RPAK4C-4R	18 19
RP5T3	RPAK4C-4R	19
RP5U1	RPAK4C-4R	19
RP5U2	RPAK4C-4R	19
RP6C1	RPAK4C-4R	18
RP6C2	RPAK4C-4R	18
RP6C3	RPAK4C-4R	18
RP6D1	RPAK4C-4R	18
RP6D2	RPAK4C-4R	18
RP6D3	RPAK4C-4R	18
RP6E1	RPAK4C-4R	37
RP6E2	RPAK4C-4R	37
RP6N1	RPAK4C-4R	18
RP6N2	RPAK4C-4R	18
RP6N3	RPAK4C-4R	18
RP6P1	RPAK4C-4R	18
RP6P2	RPAK4C-4R	18
RP6P3	RPAK4C-4R	18
RP6T1	RPAK4C-4R	37
RP6T2	RPAK4C-4R	37
RP6T3	RPAK4C-4R	37
RP7E1	RPAK4C-4R	37
RP7T1	RPAK4C-4R	37
RP8B1	RPAK4C-4R	35
RP8B2	RPAK4C-4R	35
RT2V1	THERMISTOR	46
RT3G1	THERMISTOR	46
RT3V1	THERMISTOR	46
RT3V2	THERMISTOR	46
RT6M1	THERMISTOR	43
U2D1	PBGA2_495	5 6 7
U2T1	SC1186	26
U3B1	LM358	48
U3B2	FET_VREG	31
U3C1	NV2A	11 12
U3E1	DDR_SDRAM2MX32	17
U3R1	CY2305	6
U3T1	DDR_SDRAM2MX32	17
U4B1	CX25871	42

U4G1	SC1110	30
U5B1	MC78M09	41
U5F1	DDR_SDRAM2MX32	16
U5G1	PHB21N06LT	31
U5U1	DDR_SDRAM2MX32	16
U6A1	LF353	40
U6B1	WM9709	38
U6B2	DDR_SDRAM2MX32	14
U6D1	DDR_SDRAM2MX32	15
U6E1	MCPX	23 24
U6F1	ADM1032	36
U6N1	DDR_SDRAM2MX32	14
U6R1	DDR_SDRAM2MX32	15
U7B1	ICS1893AF	35
U7B2	PIC16LC63A	48
U7C1	ICS_XCLK	29
U7C2	AT24C02	36
U7C3	ICS331	29
U7D1	29F080	45
U7P1	CY24240	29
U8E1	SC1103	28
U8U1	MBRD1035CTL	28
U8U2	PHB21N03LT	28
Y6F1	XTAL4P	23
Y6F2	CRYSTAL	23
Y7B1	XTAL4P	29
Y7B2	CRYSTAL	29