

# GREYBULL

## REV 1.0

### FAB M

### RETAIL

PAGE	CONTENTS
[1]	COVER PAGE
[2]	SOC, PCIE X + CLOCKS + VIDEO
[3]	SOC POWER, MEM+CPUCORE+MEMCORE+NBCORE+MISC
[4]	SOC POWER, V_GFXCORE + VSS
[5]	SOC, MEMOERY PARTITION C + D
[6]	SOC, MEMORY PARTITION A + B
[7]	SOC, VSS + SPARE
[8]	SOC, DEBUG + SB SIGNALS
[9]	SOC, DECOUPLING
[10]	SOC, DECOUPLING
[11]	SOC, DECOUPLING
[12]	MEMORY CHANNEL D
[13]	MEMORY CHANNEL D
[14]	MEMORY CHANNEL D, DECOUPLING
[15]	MEMORY CHANNEL C
[16]	MEMORY CHANNEL C
[17]	MEMORY CHANNEL C, DECOUPLING
[18]	MEMORY CHANNEL B
[19]	MEMORY CHANNEL B
[20]	MEMORY CHANNEL B, DECOUPLING
[21]	MEMORY CHANNEL A
[22]	MEMORY CHANNEL A
[23]	MEMORY CHANNEL A, DECOUPLING
[24]	KIC, USB
[25]	KIC, PCIE X + SATA + VIDEO
[26]	KIC, SMC
[27]	KIC, FACET
[28]	KIC, POWER
[29]	KIC, CLOCKS + STRAPPING + POR
[30]	KIC, POWER
[31]	KIC, DECOUPLING
[32]	CONTROLLER, ETHERNET
[33]	EMMC
[34]	CONN, RJ45 + TOSLINK
[35]	CONN, USB
[36]	CONN, USB
[37]	CONN, HDMI IN

[38]	CONN, HDMI OUT
[39]	CONN, ODD + HDD
[40]	CONN, LITHIUM + FAN
[41]	CONN, PWR
[42]	VREGS, BLEEDERS
[43]	VREGS, INPUT + OUTPUT FILTERS
[44]	VREGS, CPUCORE
[45]	VREGS, GFXCORE
[46]	VREGS, GFXCORE OUTPUT PHASE 1 & 2
[47]	VREGS, GFXCORE OUTPUT PHASE 3 & 4
[48]	VREGS, CPUCORE OUTPUT PHASE
[49]	VREGS, VTT TERMINATION
[50]	VREGS, NBCORE
[51]	VREGS, MEMCORE
[52]	VREGS, MEMIOCD
[53]	VREGS, MEMIOAB
[54]	VREGS, V5P0
[55]	VREGS, V5P0 DUAL
[56]	VREGS, V3P3
[57]	VREGS, VSOCPHY
[58]	VREGS, VSOCPLL + VBURN + VFUSE + VBAT
[59]	VREGS, VSB2P5
[60]	VREGS, VSB1P8PLL + VSB1P8IO + VSBCORE + VSB1P1PLL
[61]	VREGS, STANDBY SWITCHERS 3P3
[62]	VREGS, STANDBY SWITCHERS 1P1 + 1P8
[63]	IR BLASTER
[64]	I2C
[65]	FACET, FTDI
[66]	FACET, FTDI + MISC
[67]	CONN, SWITCHES
[68]	CONN, HDT
[69]	DEBUG, VR HEADERS AND TEST POINTS
[70]	DEBUG, CONNECTORS
[71]	DEBUG, ENET EEPROM + MISC
[72]	LABELS AND MOUNTING

RULES: (APPLIED WHEN POSSIBLE)

- 1.) MSB TO LSB IS TOP TO BOTTOM
- 2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
- 3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
- 4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
- 5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
- 6.) TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
- 7.) SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
- 8.) SUFFIX DP AND DN ARE USED FOR DIFFERENTIAL PAIRS
- 9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
- 10.) SUFFIX N FOR ACTIVE LOW OR N JUNCTION
- 11.) SUFFIX P FOR P JUNCTION
- 12.) SUFFIX EN FOR ENABLE
- 13.) SUFFIX EN FOR ENABLE
- 14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
- 15.) PWRGD FOR POWER GOOD
- 16.) REV AND FAB ARE SET USING CUSTOM VARIABLES

TOOLS>OPTIONS>VARIABLES

[PAGE\_TITLE=COVER PAGE]

D

C

B

A

D

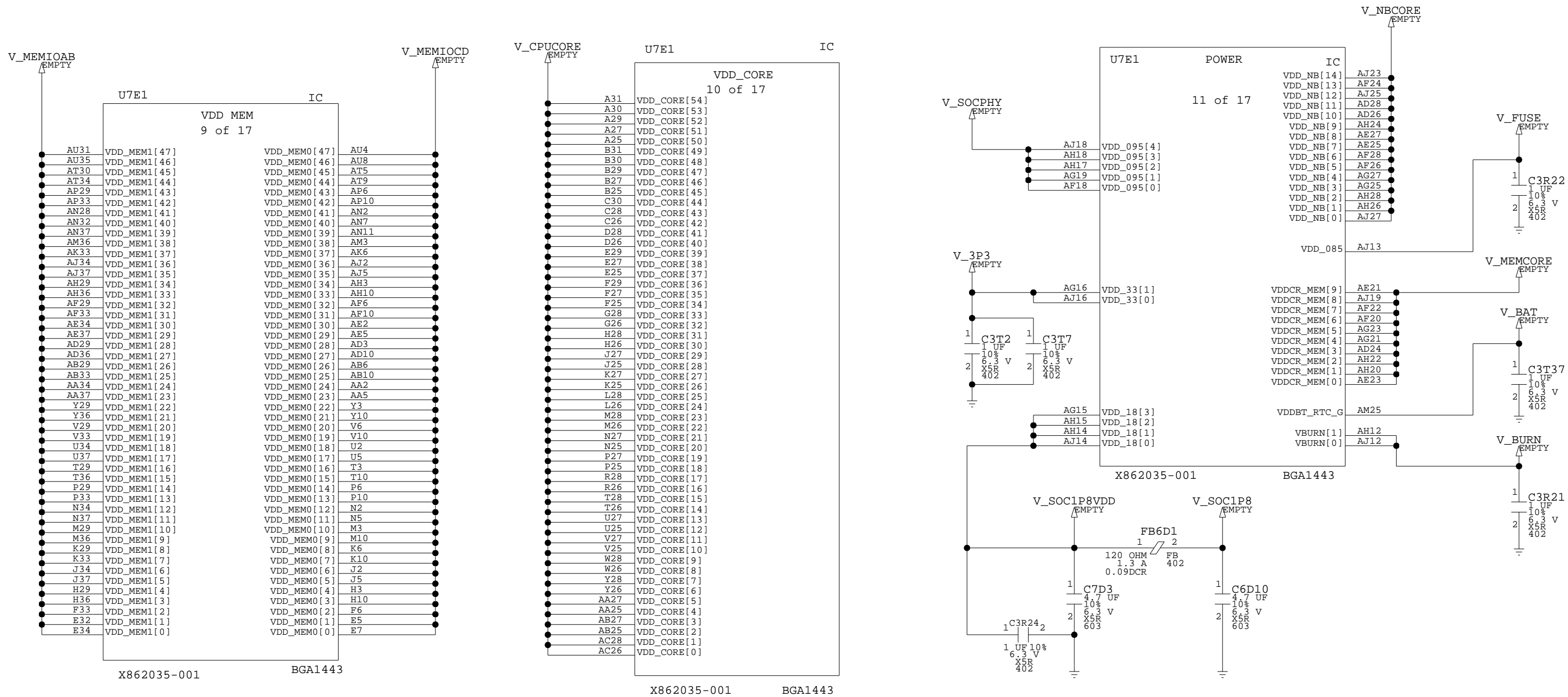
C

B

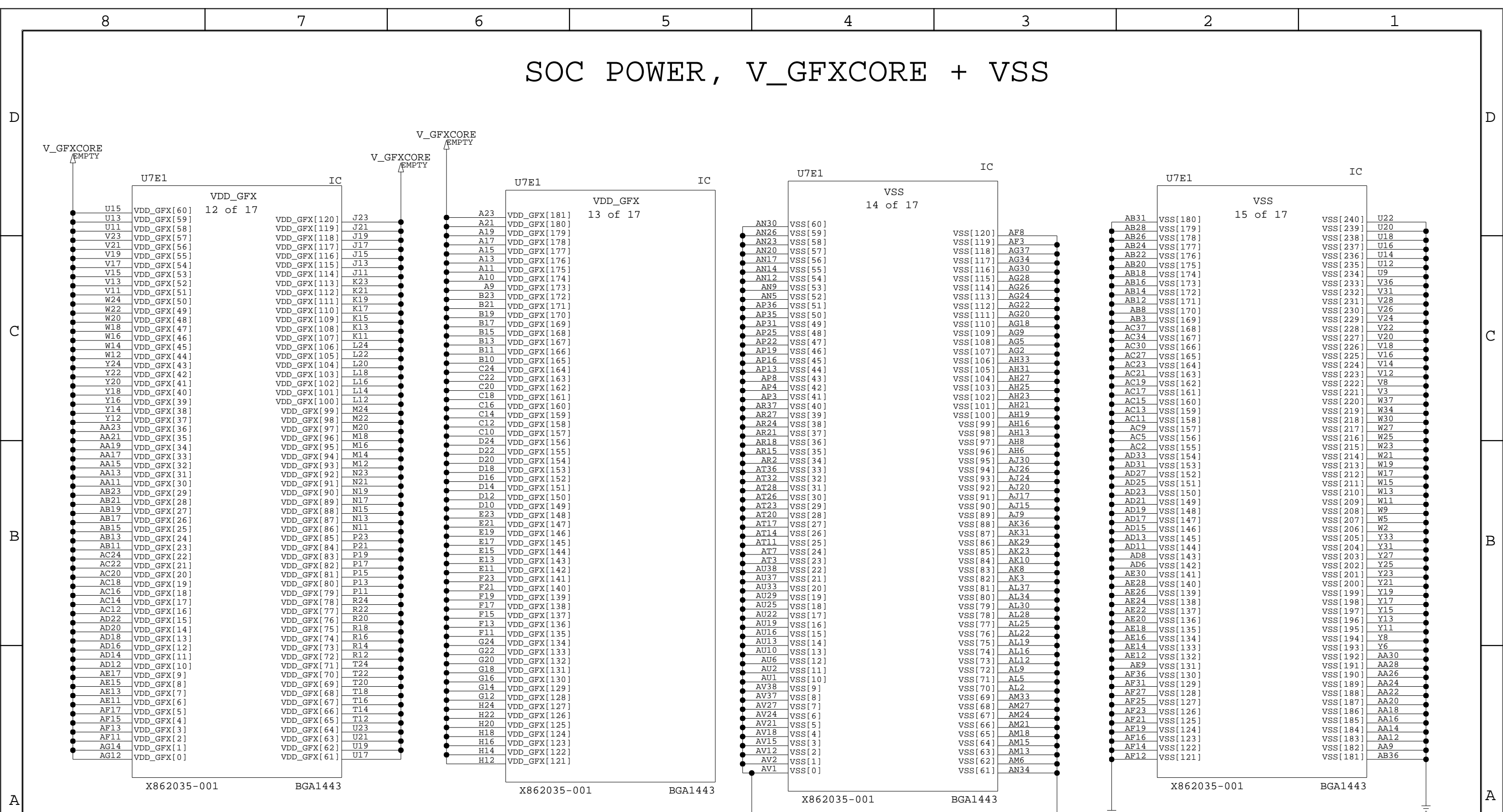
A



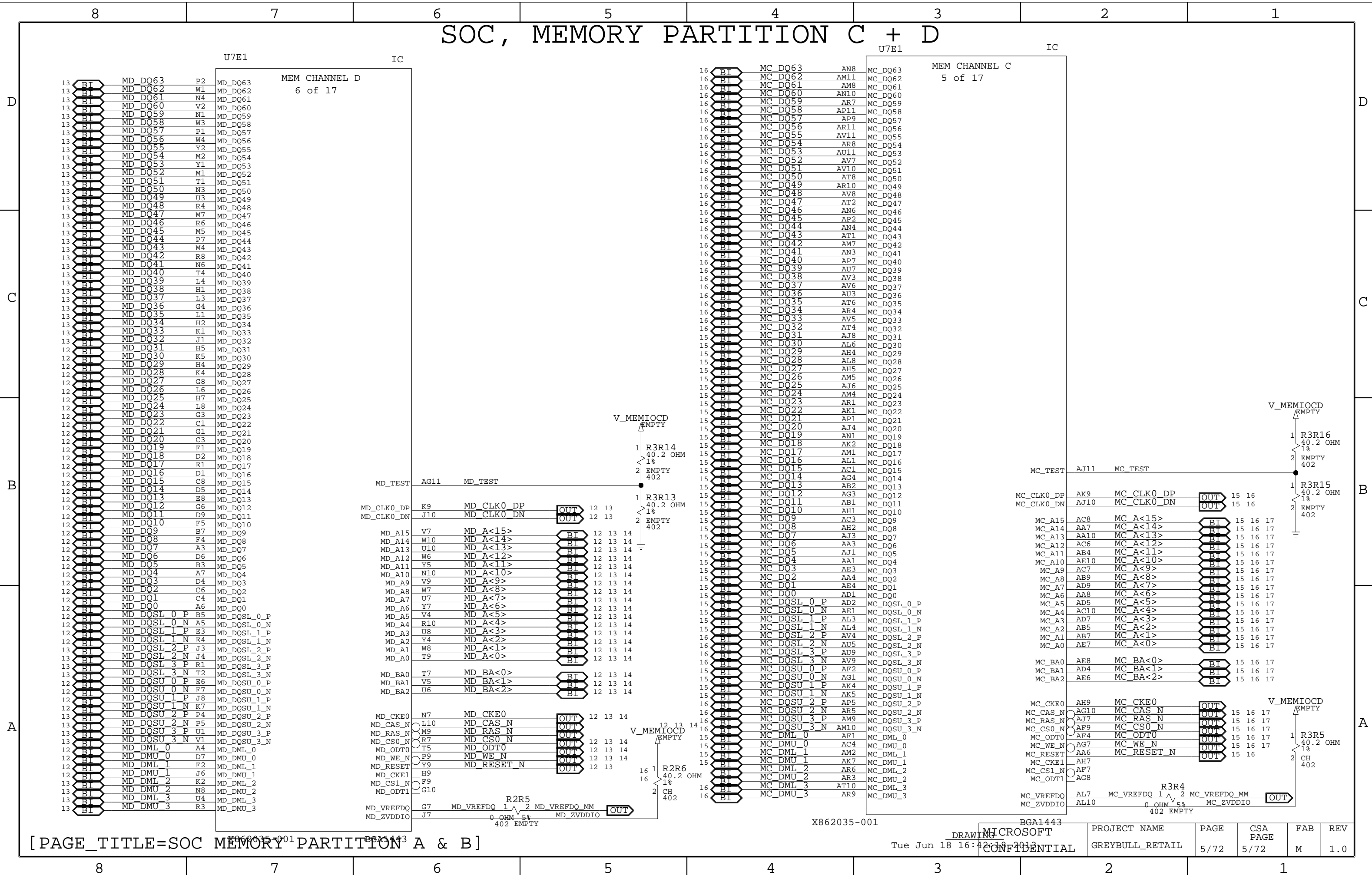
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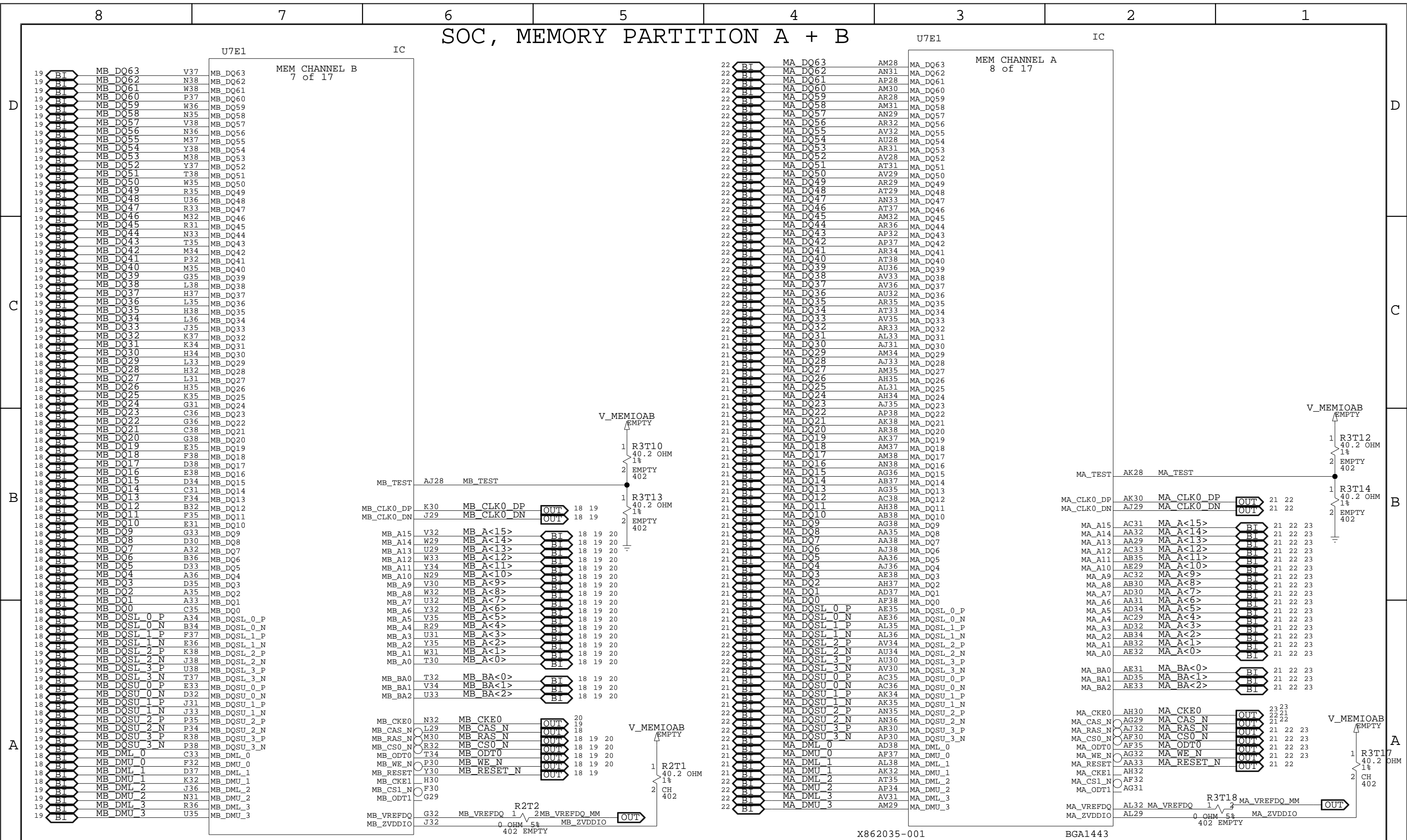
# SOC POWER, V\_GFXCORE + VSS



# SOC, MEMORY PARTITION C + D



# SOC, MEMORY PARTITION A + B



X862035-001

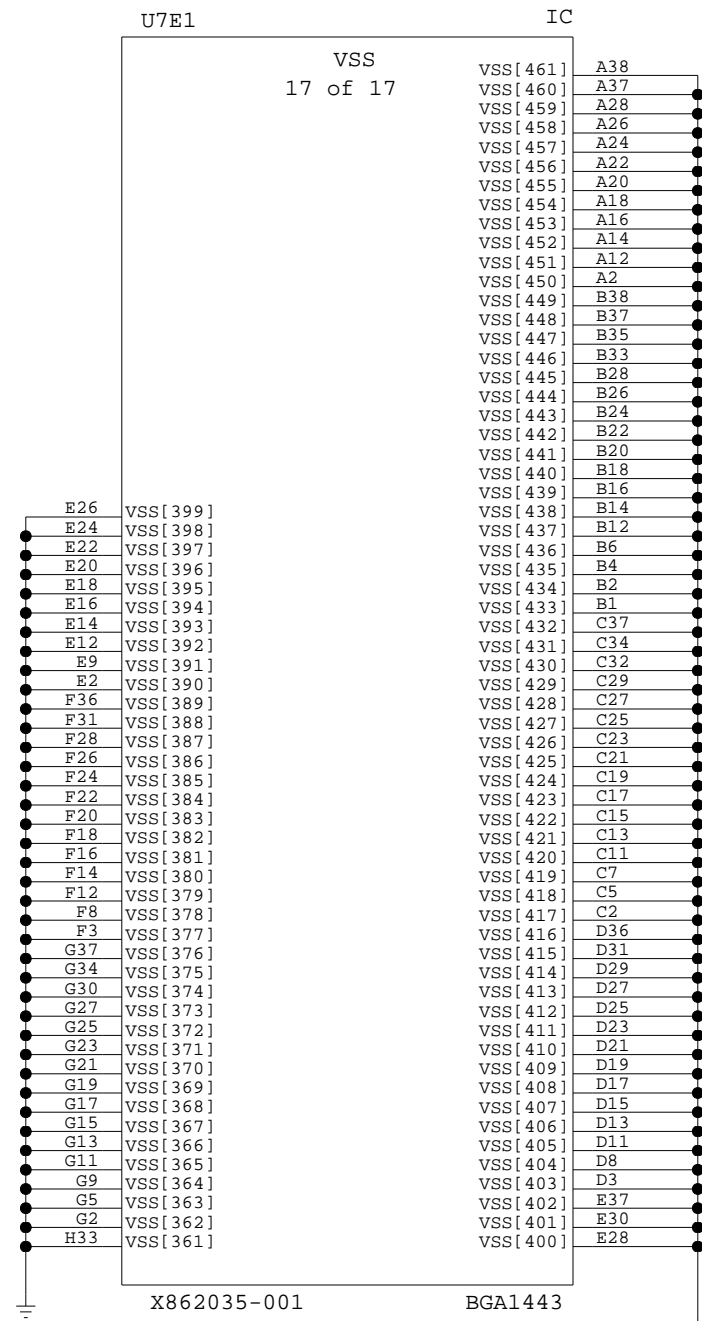
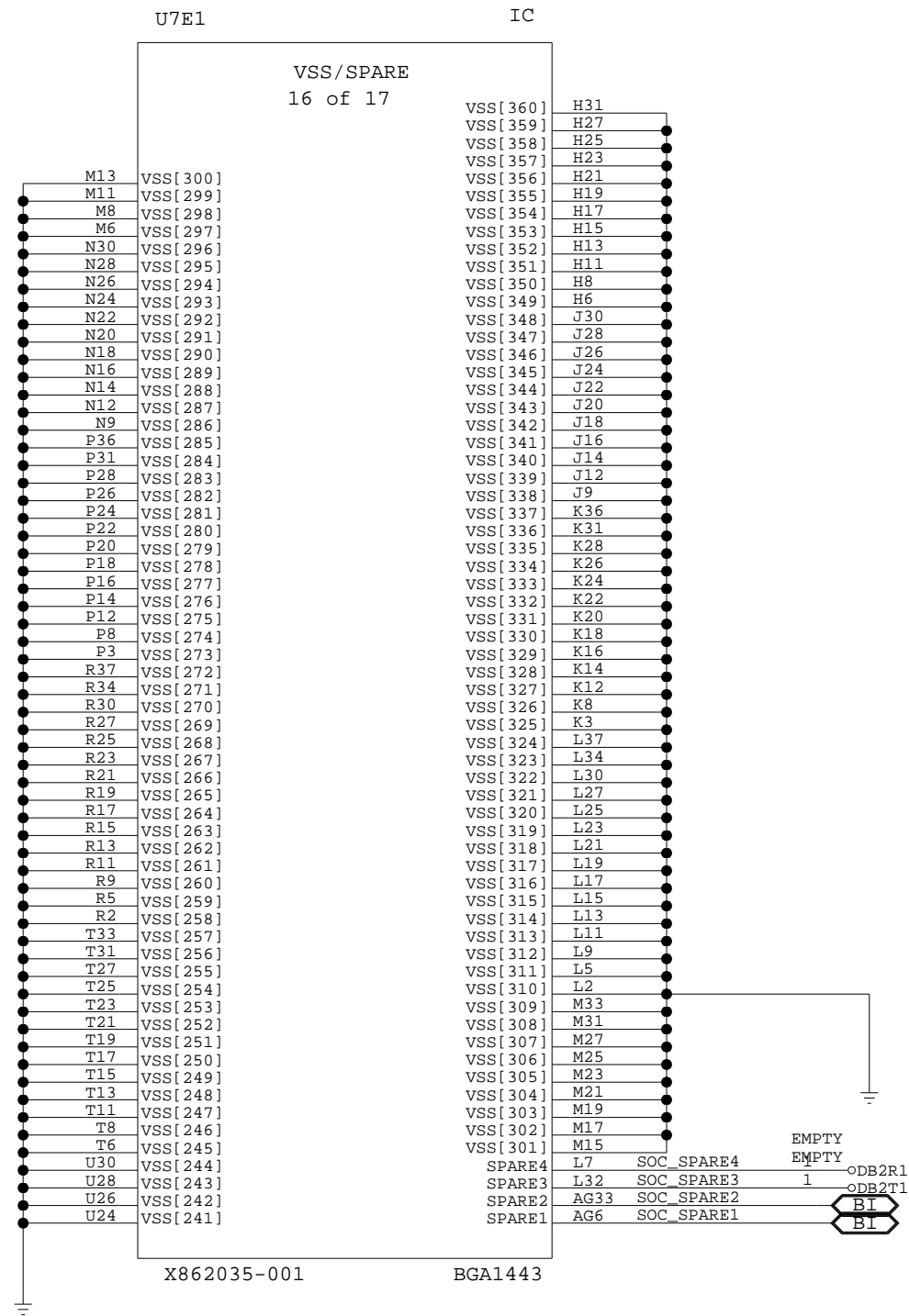
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X862035-001

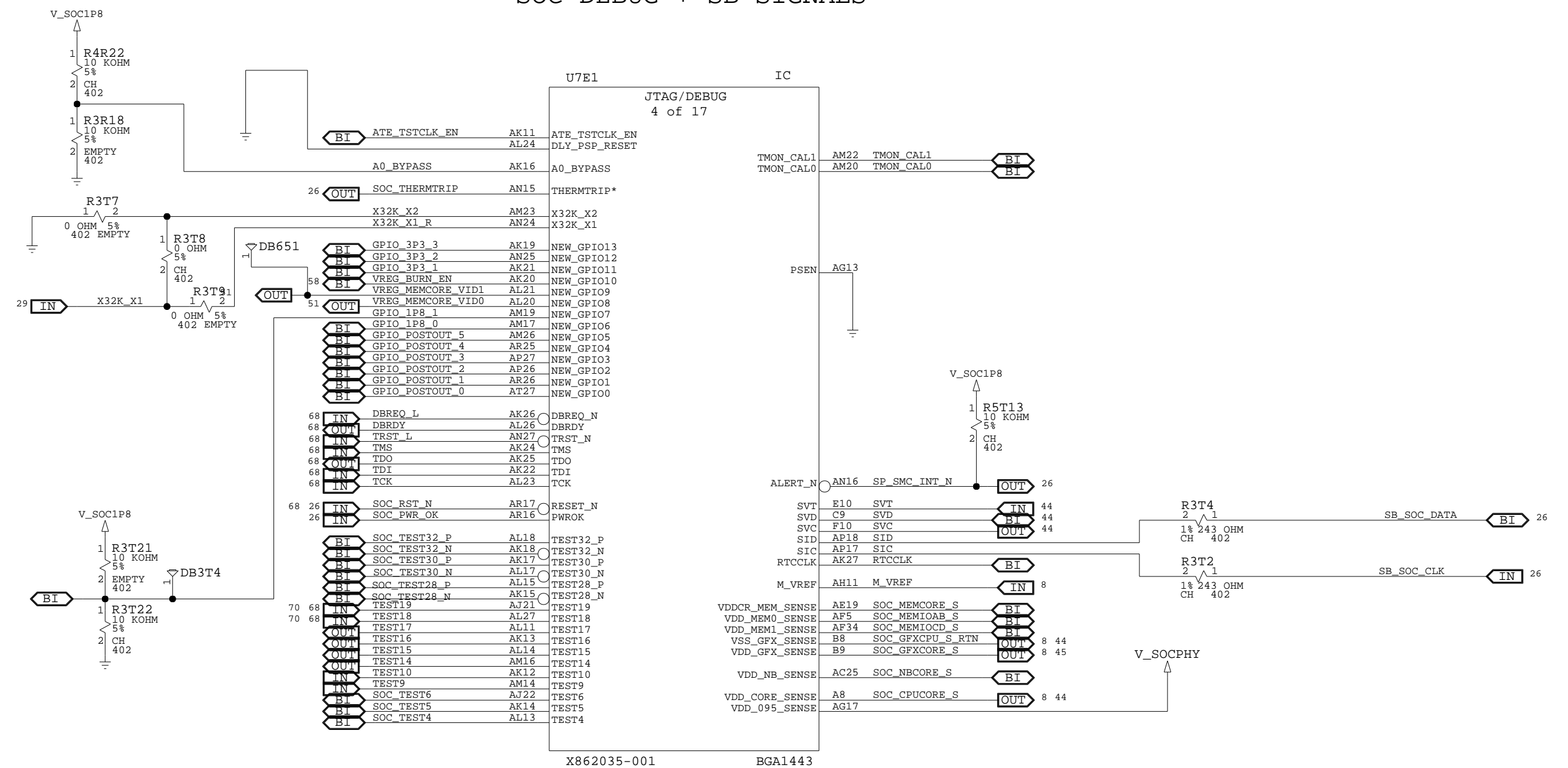
BGA1443

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 6/72	CSA PAGE 6/72	FAB M	REV 1.0
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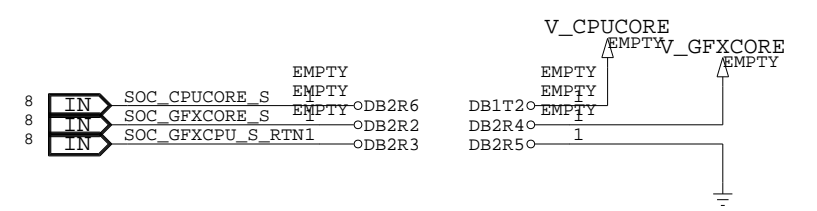
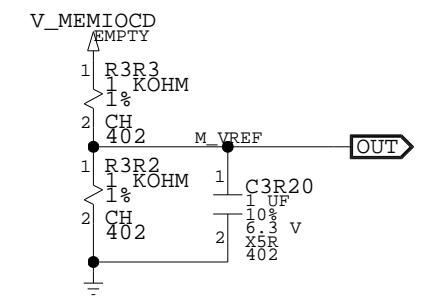
SOC VSS + SPARE



# SOC DEBUG + SB SIGNALS



X862035-001 BGA1443

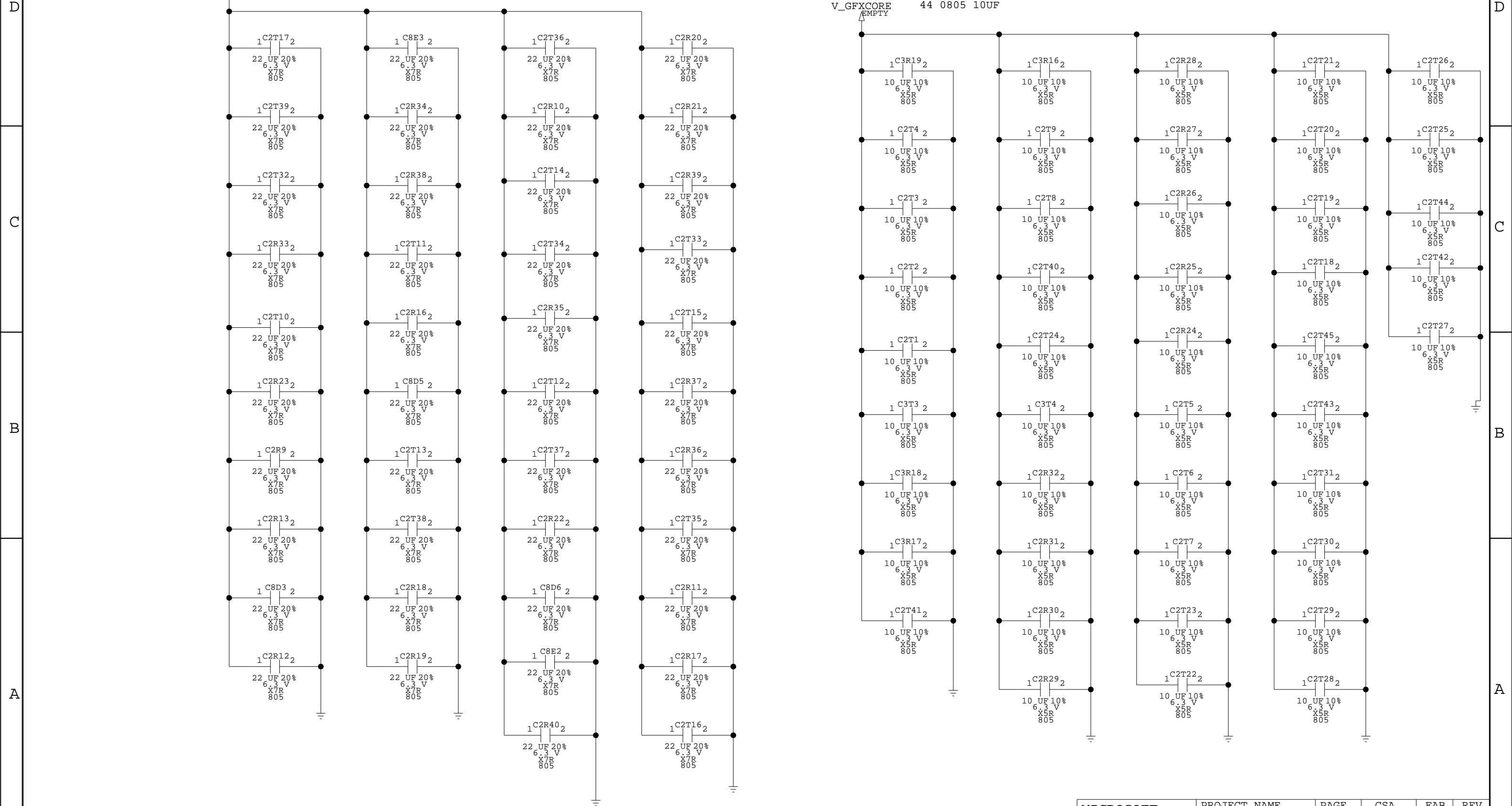




# SOC, DECOUPLING

V\_GFXCORE 42 0805 22UF  
EMPTY

V\_GFXCORE 44 0805 10UF  
EMPTY



[PAGE\_TITLE=GCPU, DECOUPLING]

DRAWING  
Tue Jun 18 16:42:26

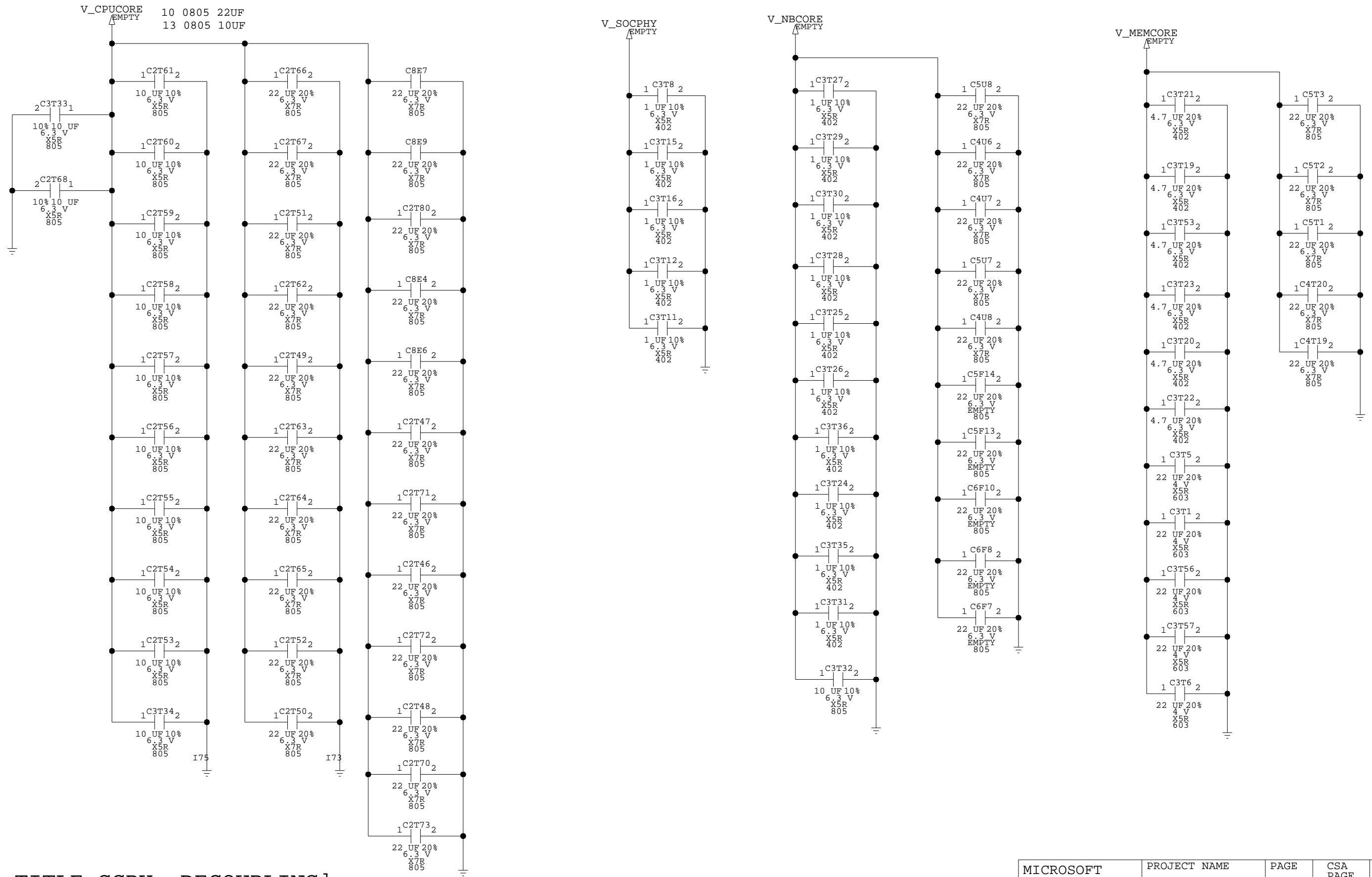
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	REV
CONFIDENTIAL	GREYBULL_RETAIL	9/72	9/72	M	1.0

# SOC, DECOUPLING

8                      7                      6                      5                      4                      3                      2                      1

D  
C  
B  
A

D  
C  
B  
A

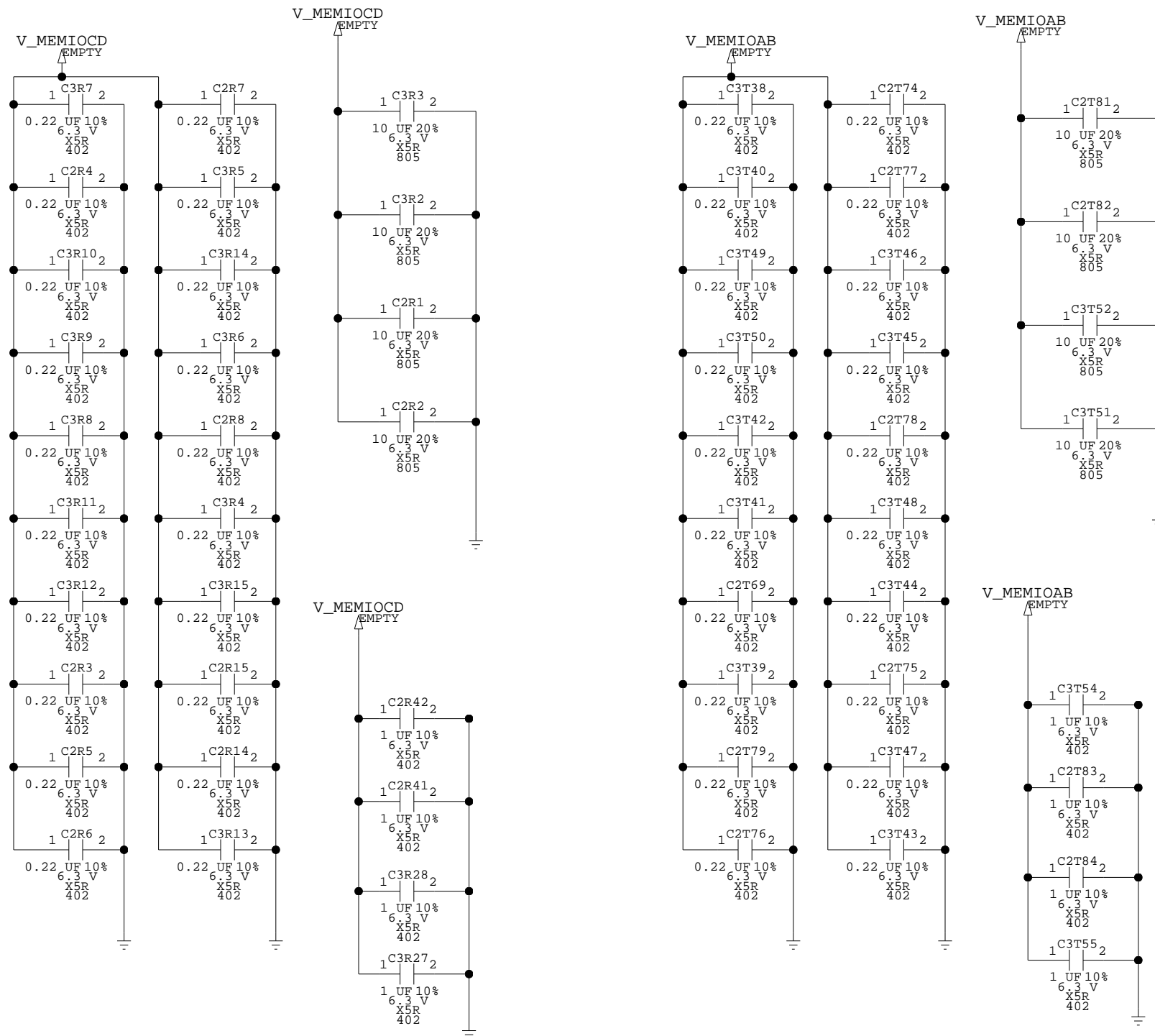


[PAGE\_TITLE=GCPU, DECOUPLING]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 10/72	CSA PAGE 10/72	FAB M	REV 1.0
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8                      7                      6                      5                      4                      3                      2                      1

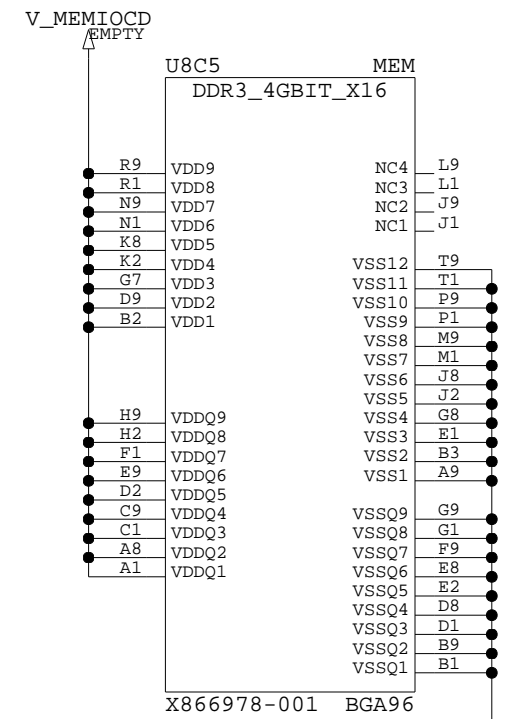
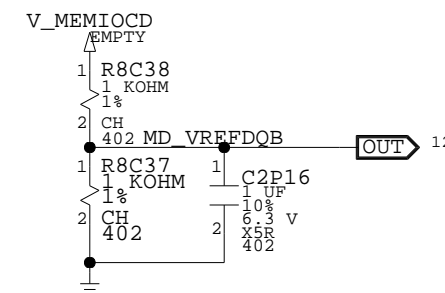
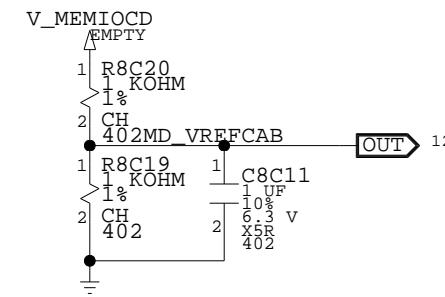
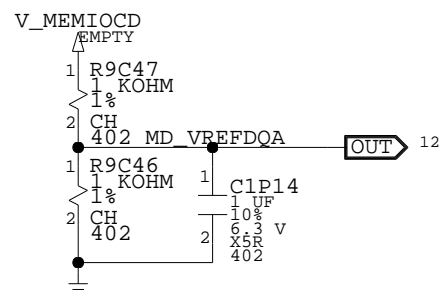
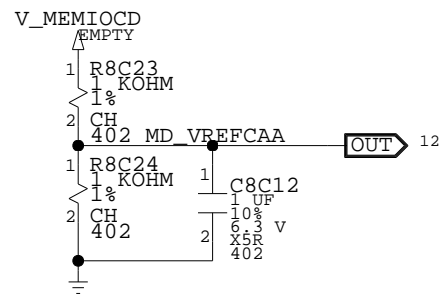
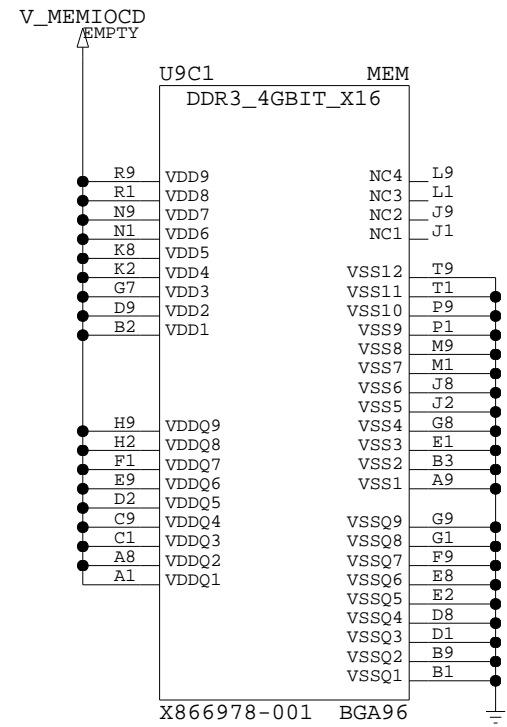
# SOC, DECOUPLING



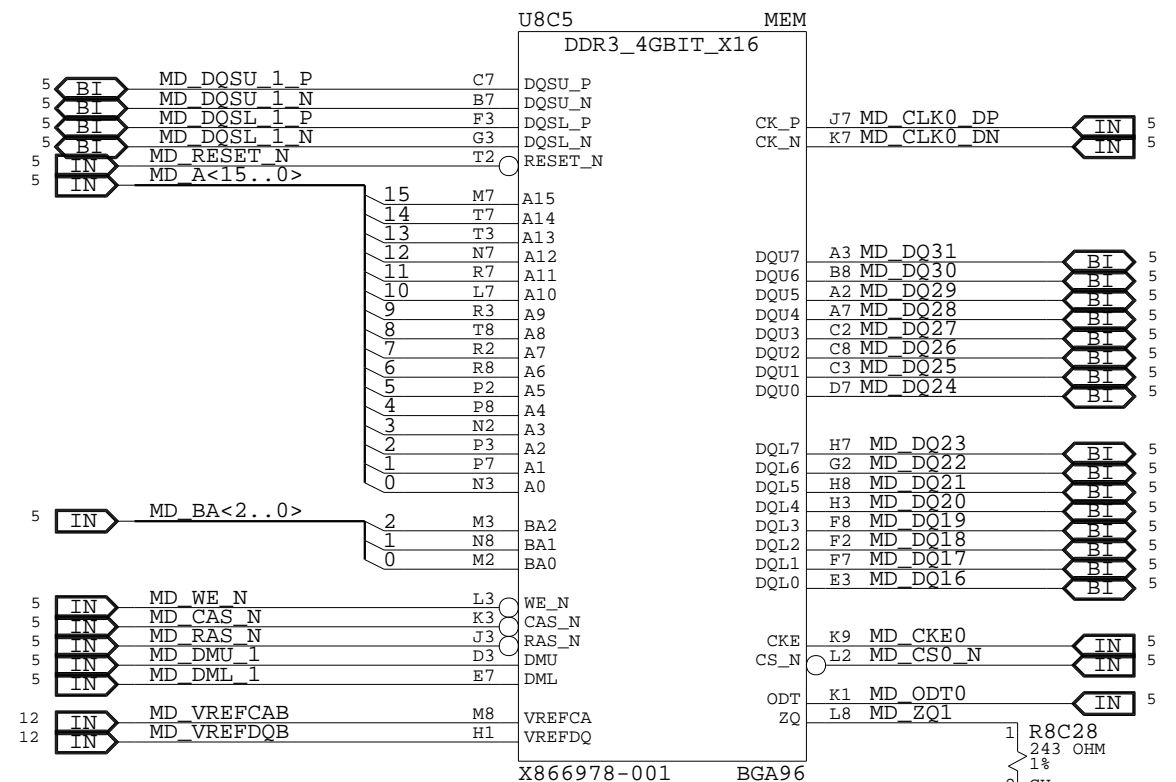
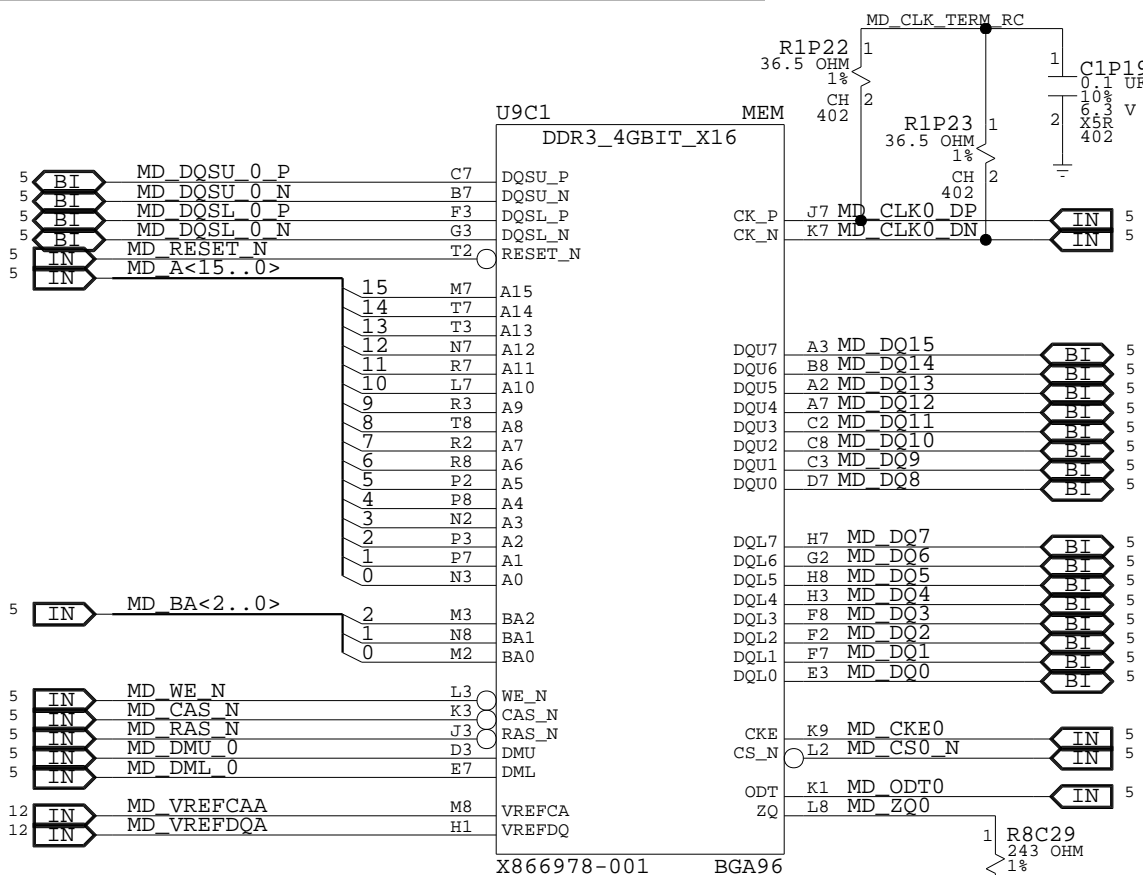
# MEMORY CHANNEL D

BYTE LANE 0  
BYTE LANE 1

BYTE LANE 2  
BYTE LANE 3



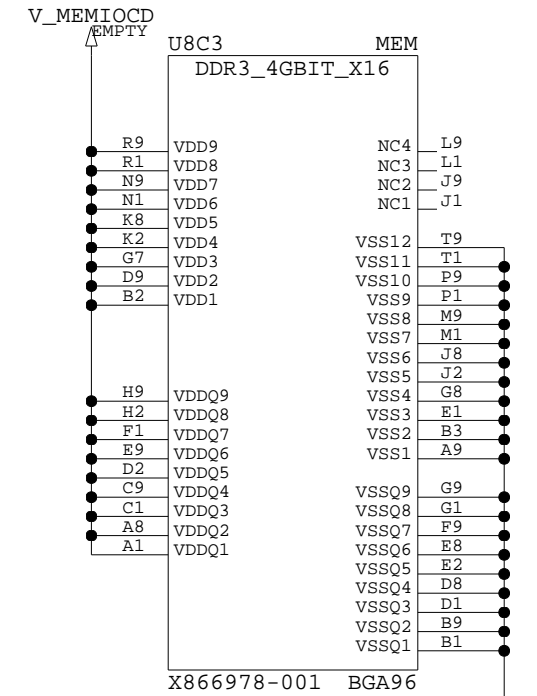
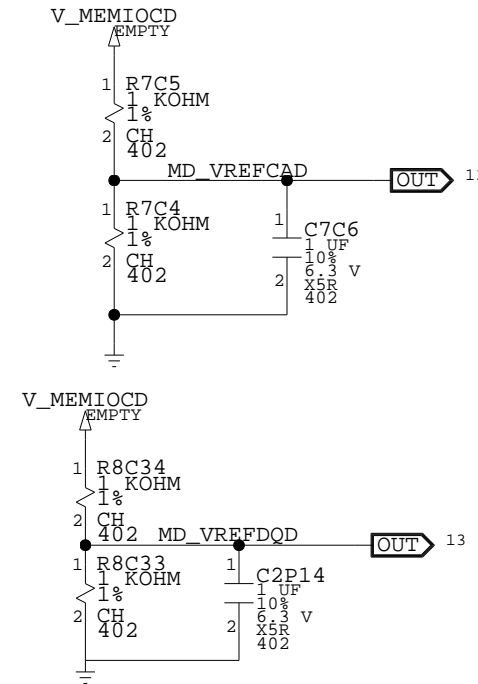
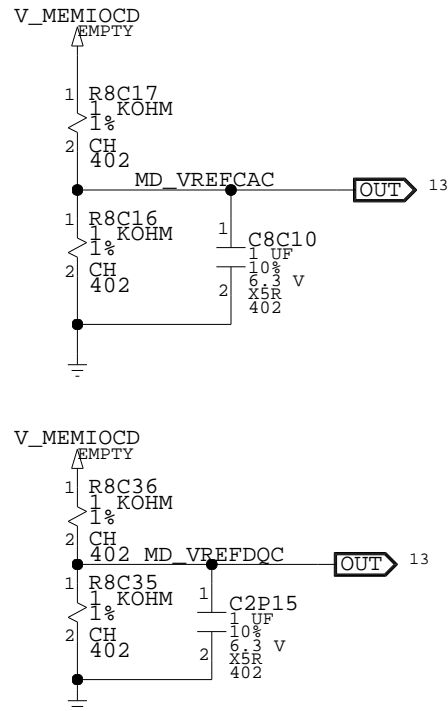
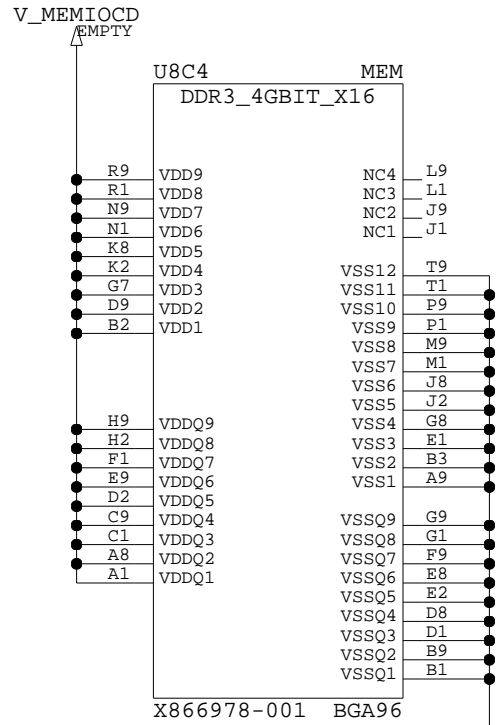
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U9C1,U8C5	EMPTY	EMPTY		DUMMY_BOM		



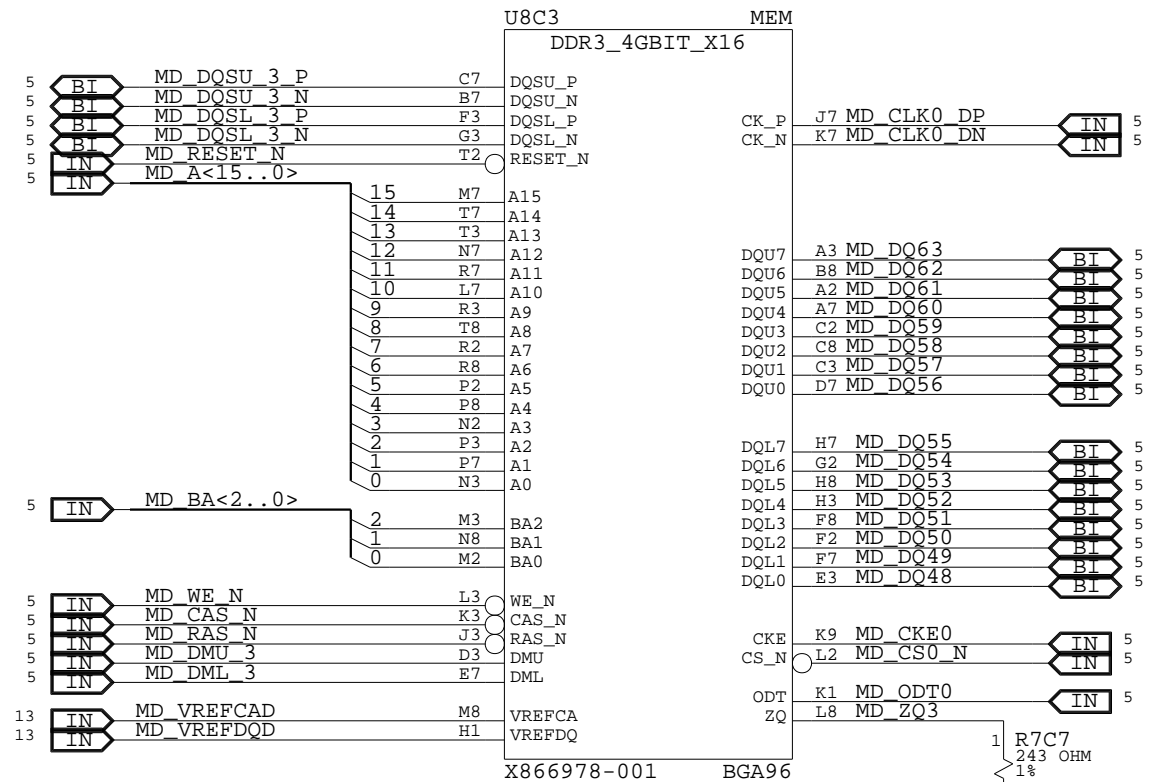
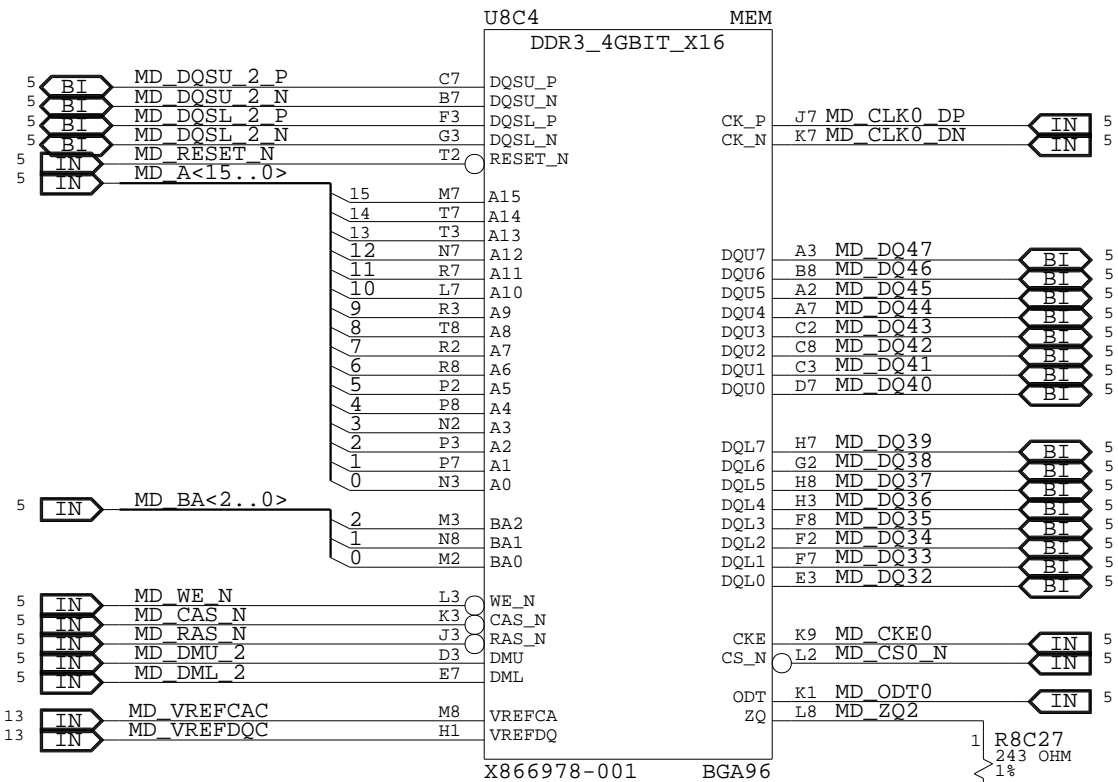
# MEMORY CHANNEL D

BYTE LANE 4  
BYTE LANE 5

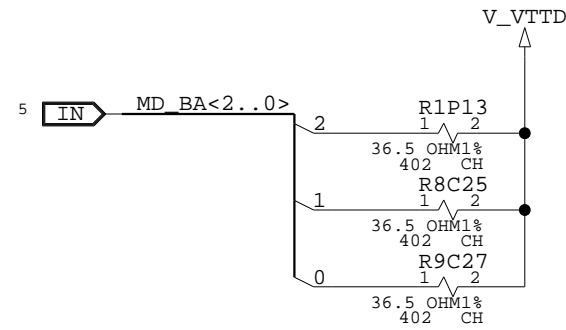
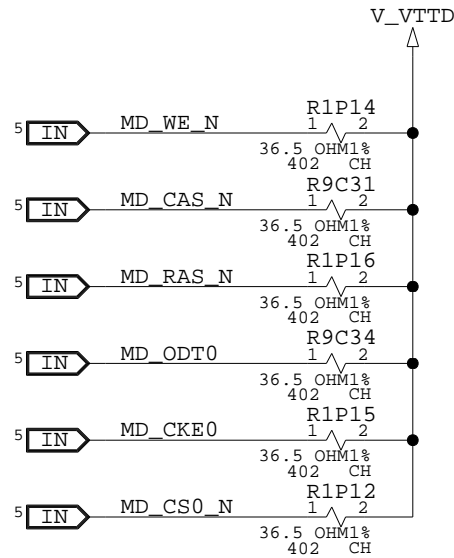
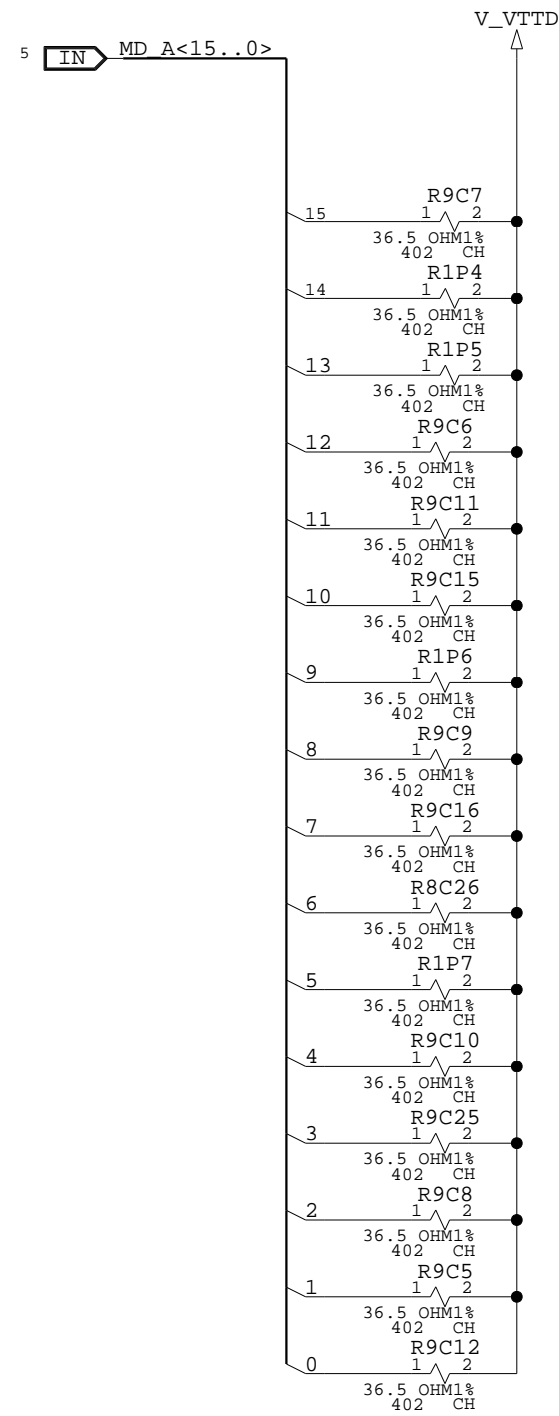
BYTE LANE 6  
BYTE LANE 7



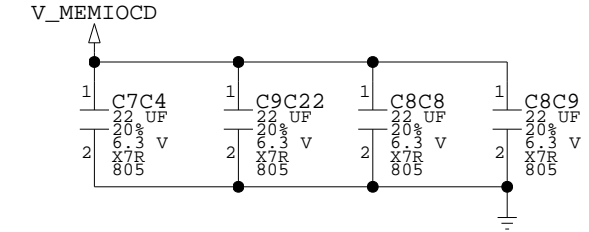
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U8C4,U8C3	EMPTY	EMPTY	MEMORY	DUMMY_BOM



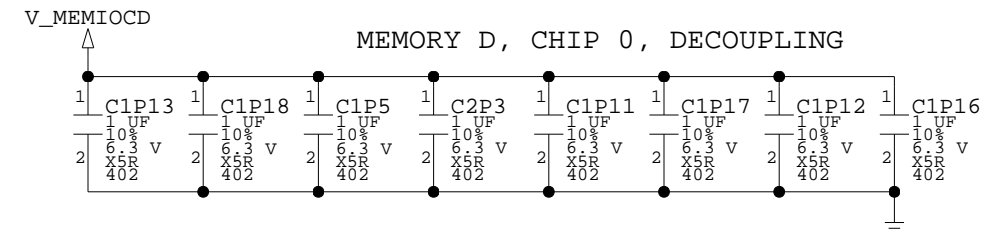
# MEMORY CHANNEL D, DECOUPLING + TERMINATION



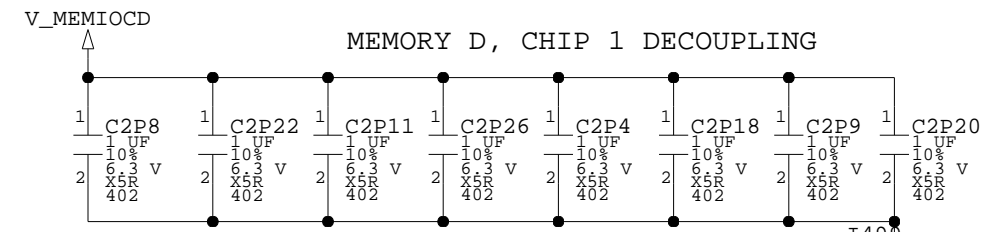
PARTITION D DECOUPLING



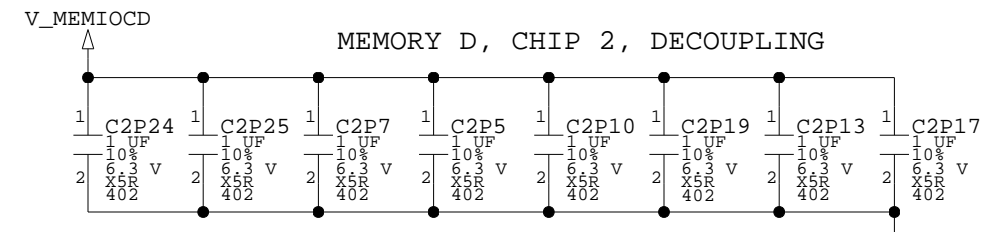
MEMORY D, CHIP 0, DECOUPLING



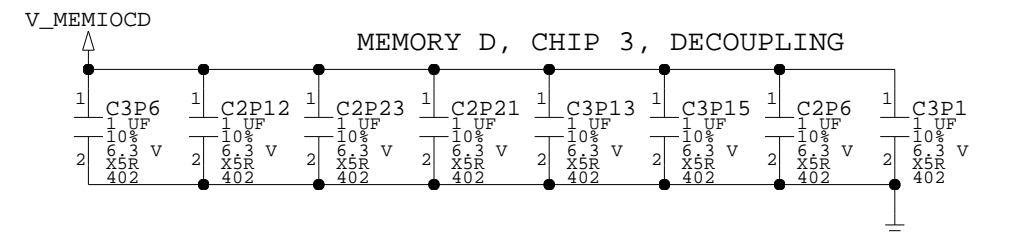
MEMORY D, CHIP 1 DECOUPLING



MEMORY D, CHIP 2, DECOUPLING



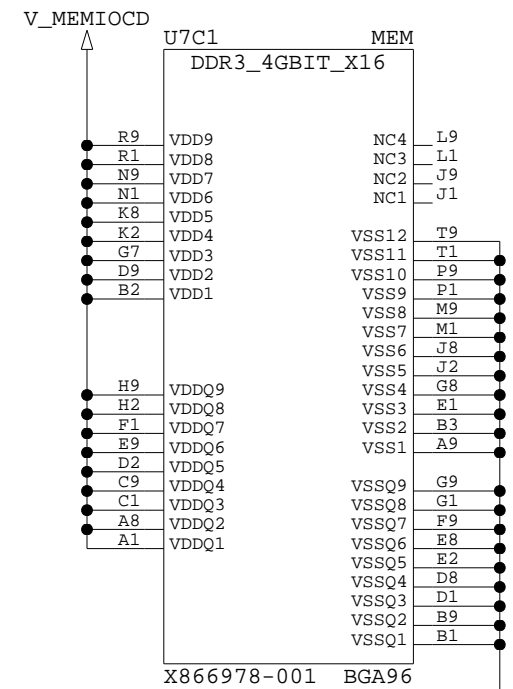
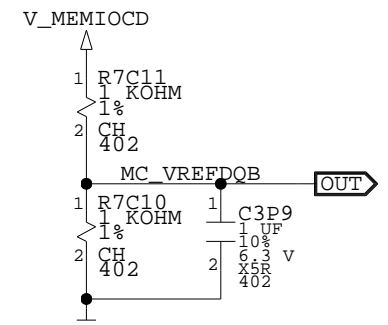
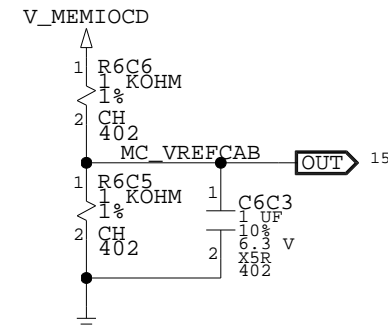
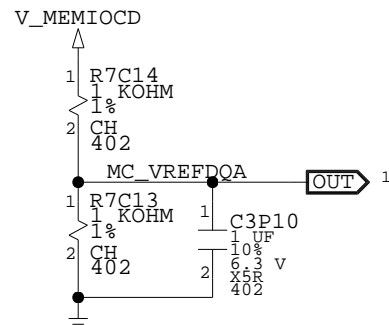
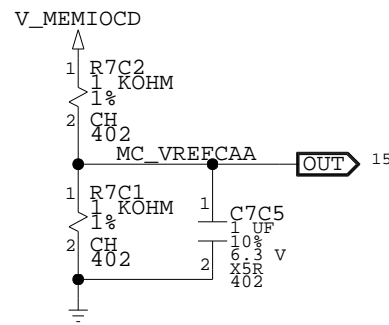
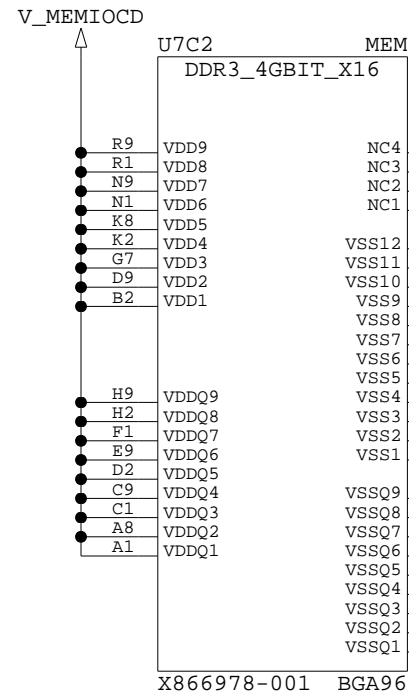
MEMORY D, CHIP 3, DECOUPLING



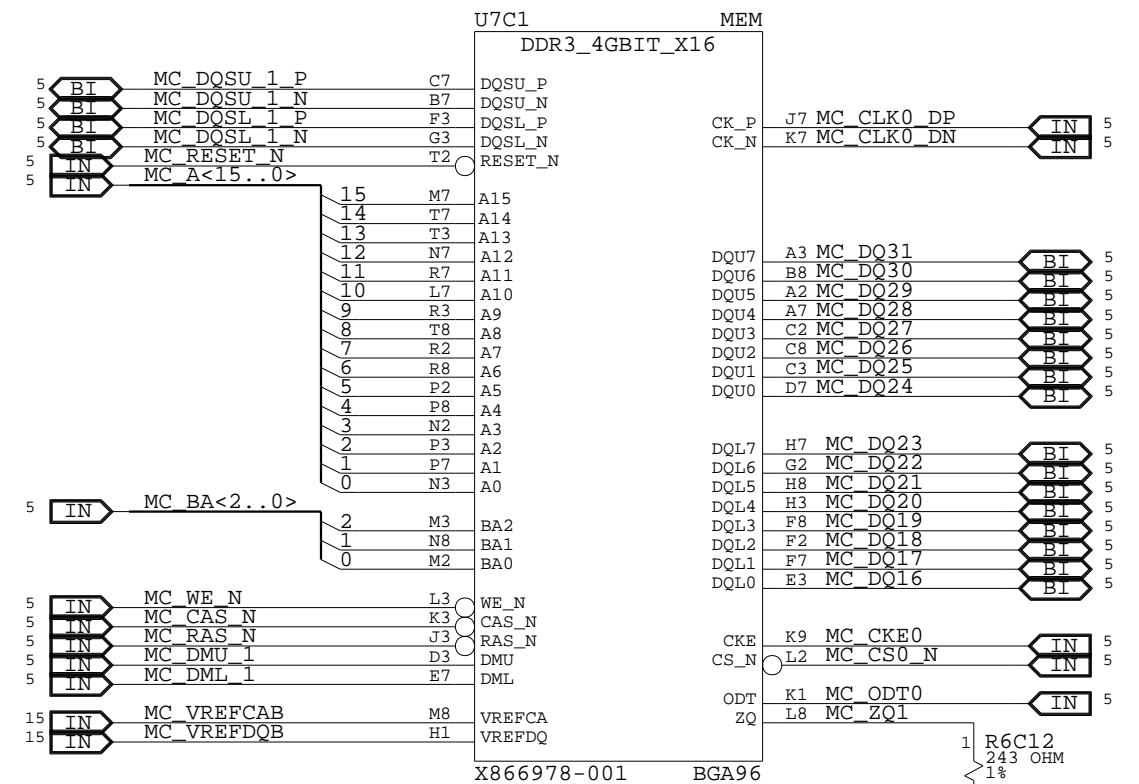
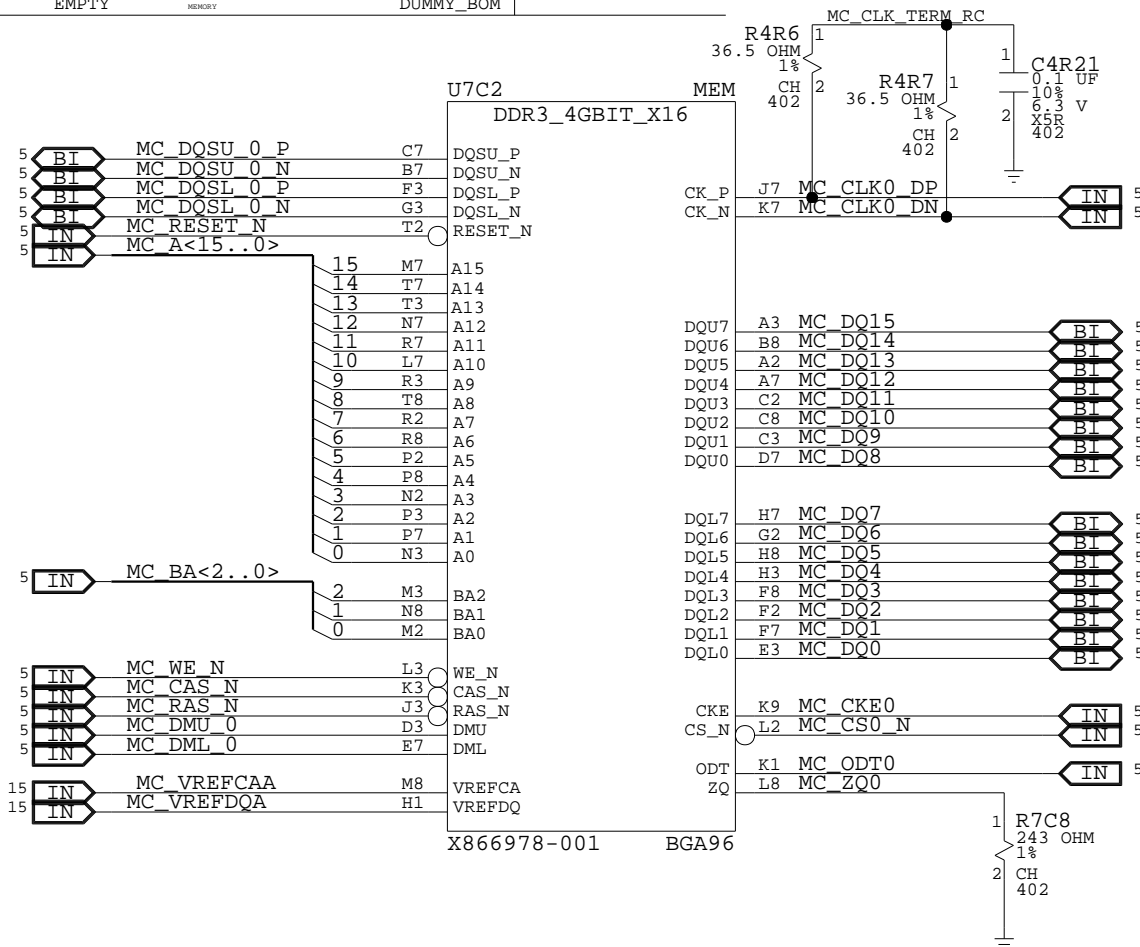
# MEMORY CHANNEL C

BYTE LANE 0  
BYTE LANE 1

BYTE LANE 2  
BYTE LANE 3



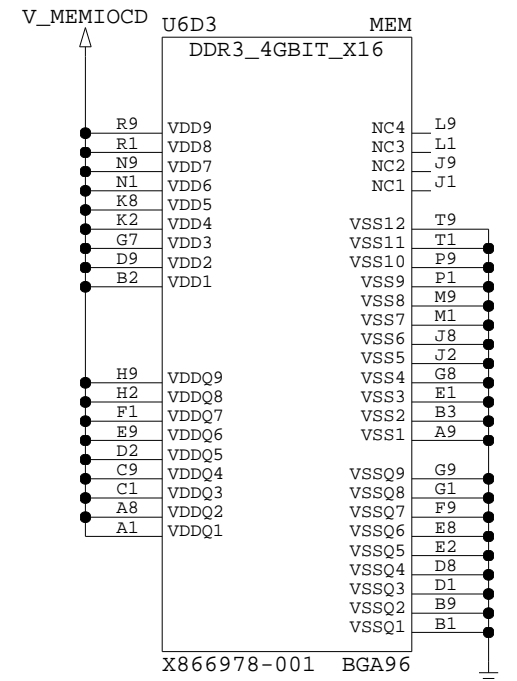
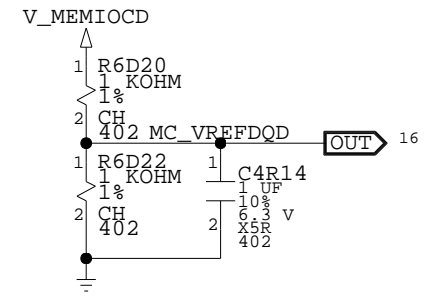
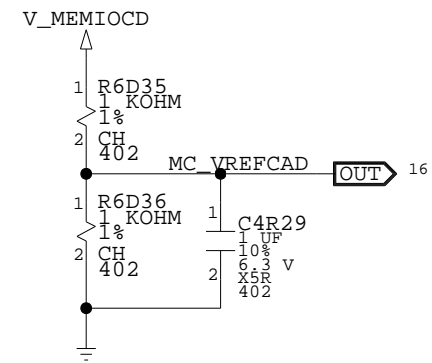
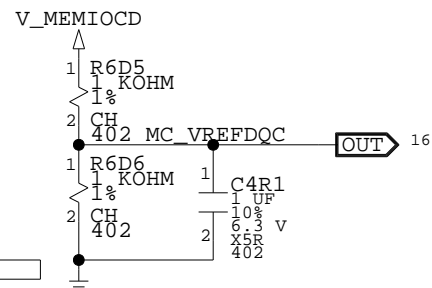
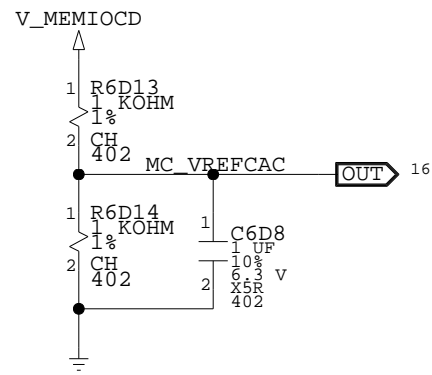
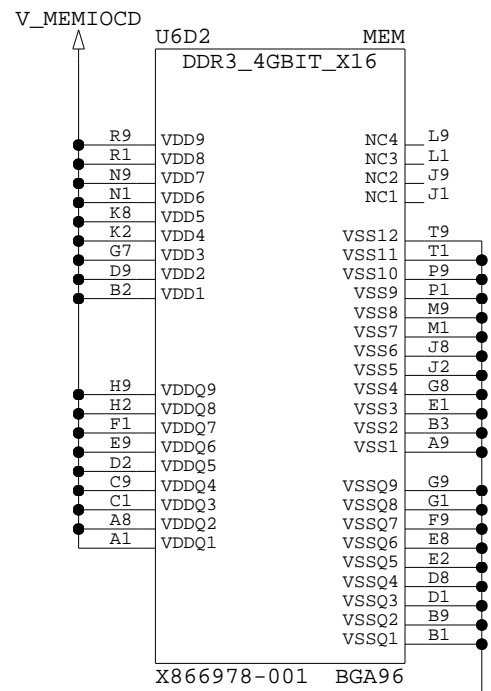
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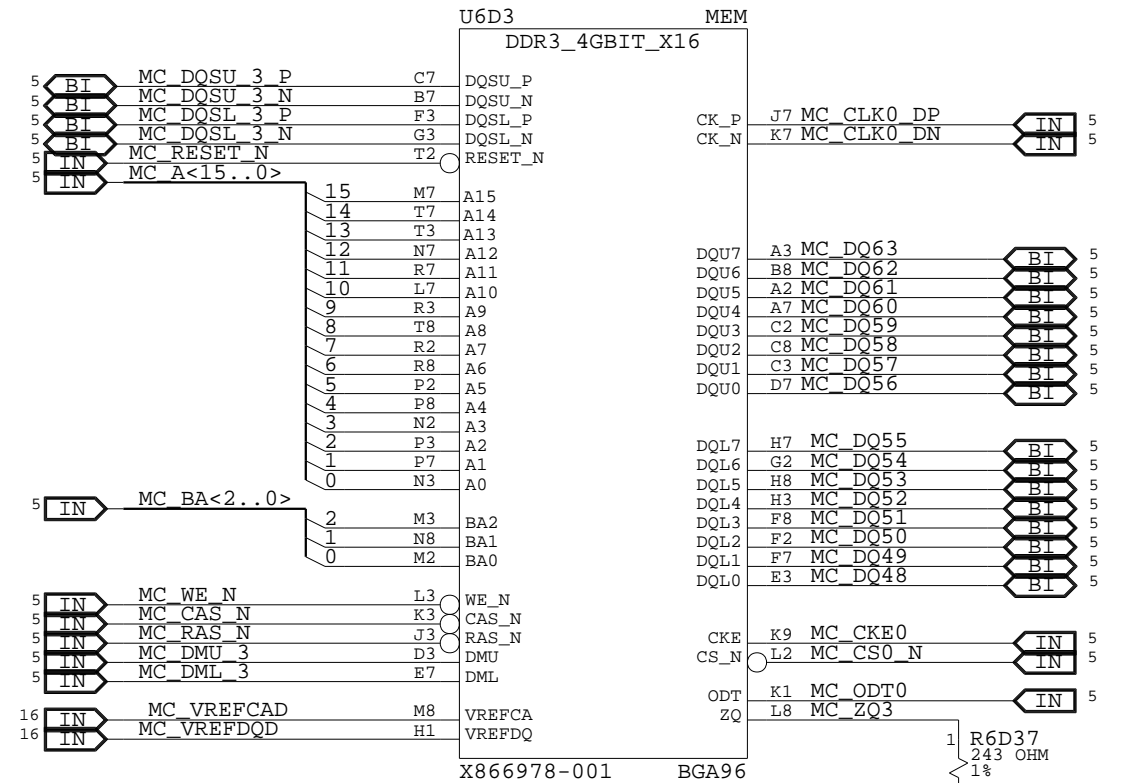
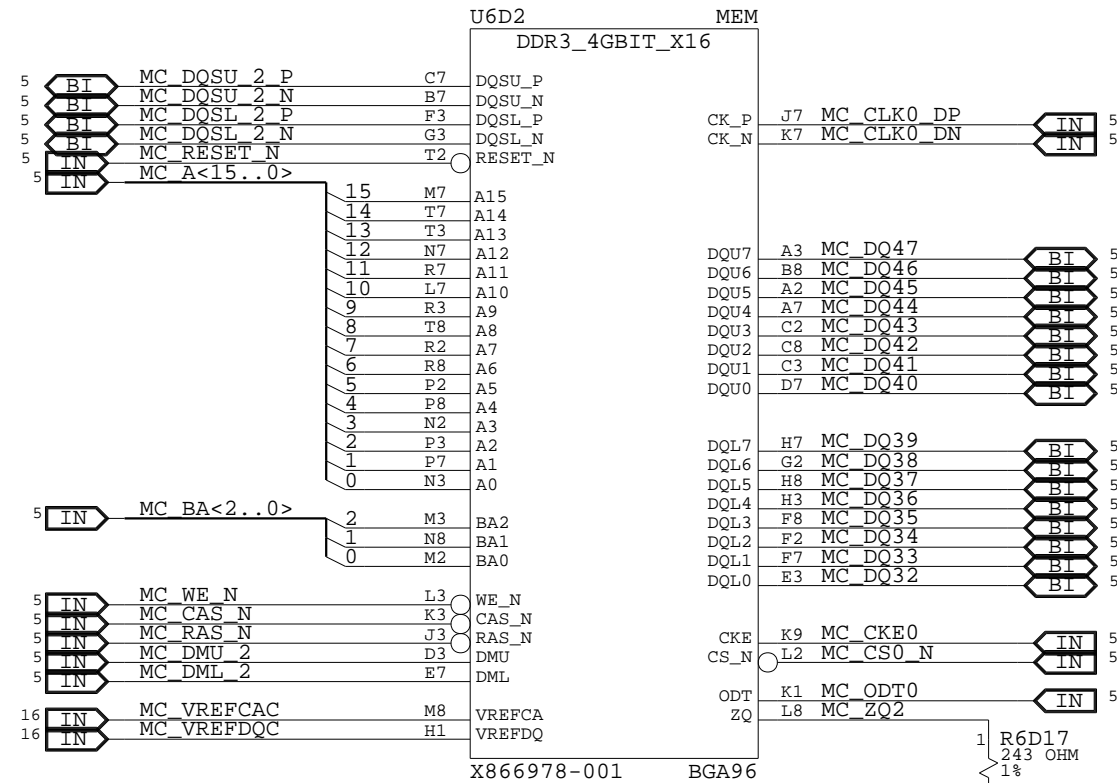
# MEMORY CHANNEL C

BYTE LANE 4  
BYTE LANE 5

BYTE LANE 6  
BYTE LANE 7

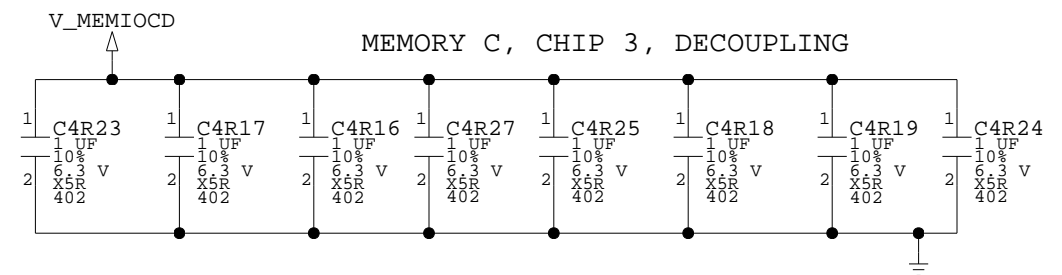
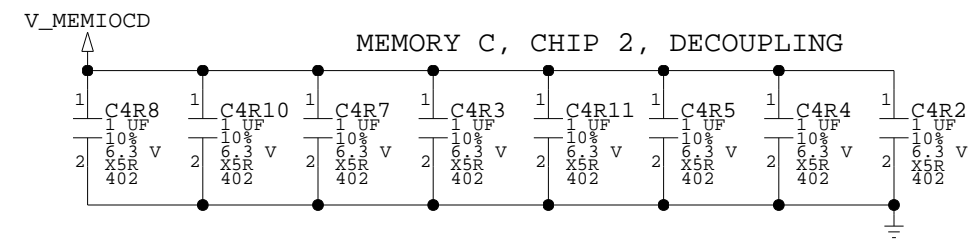
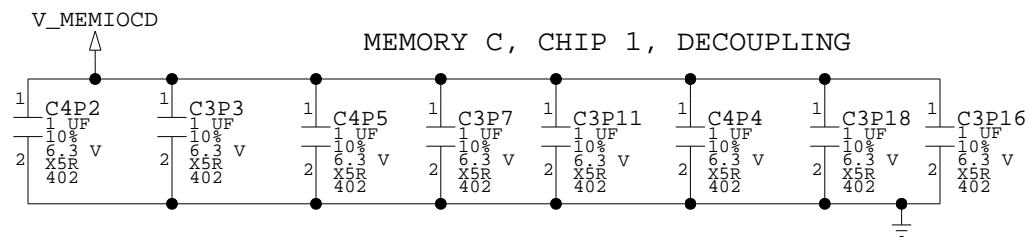
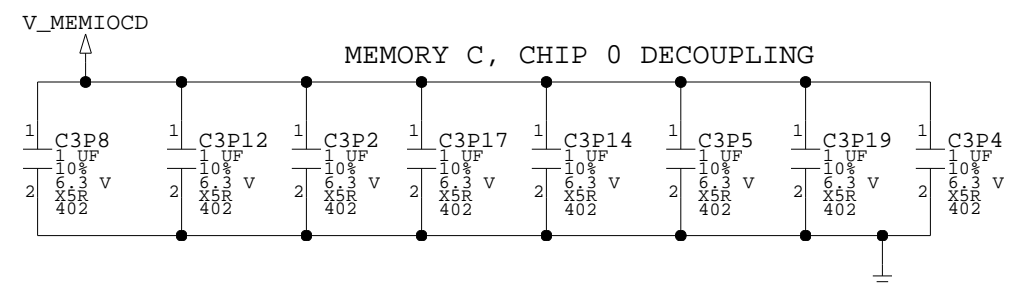
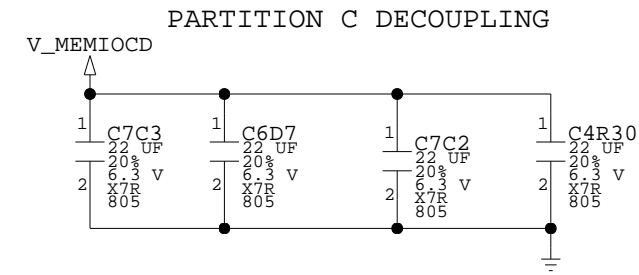
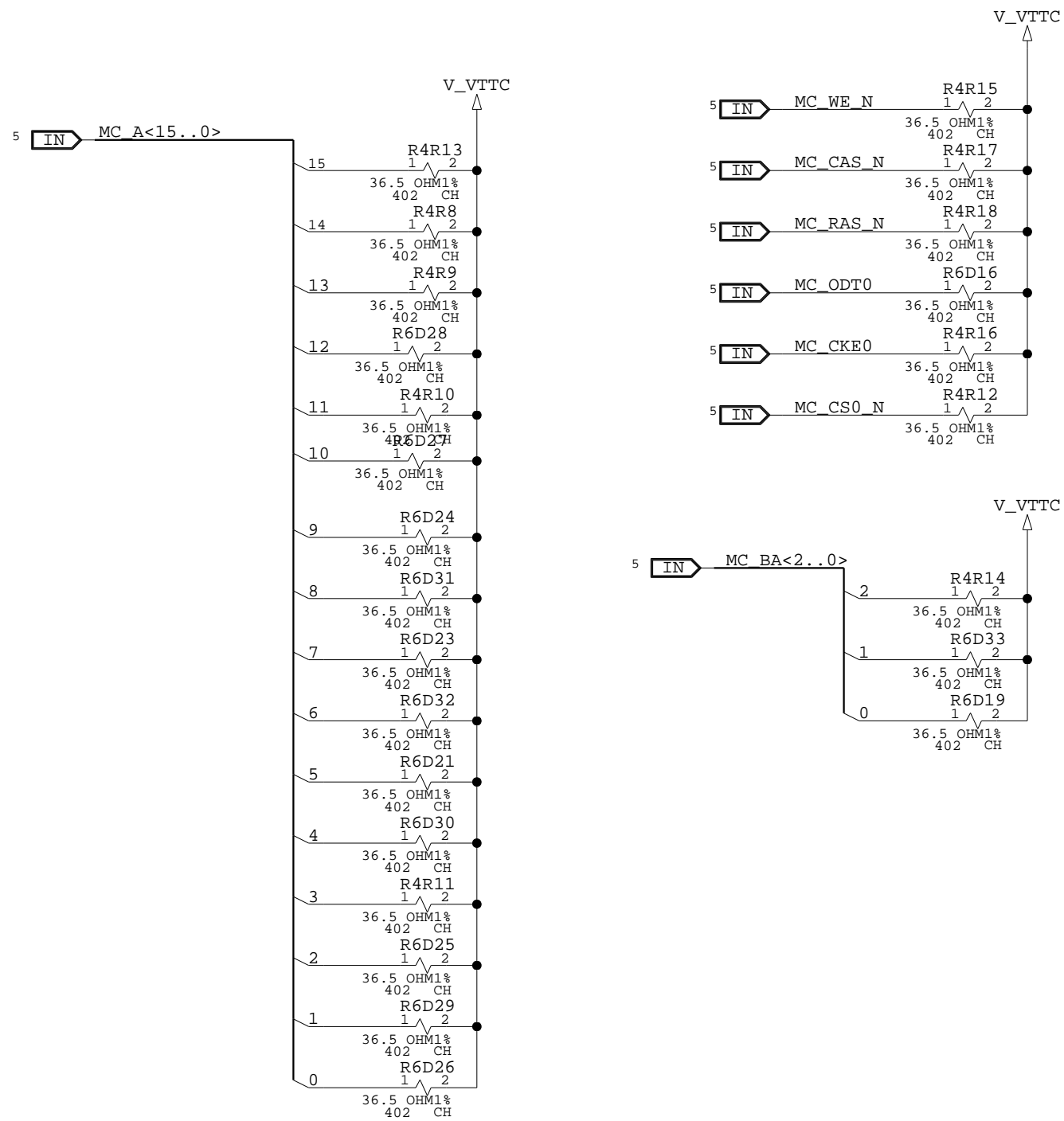


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U6D2, U6D3	EMPTY	EMPTY		DUMMY_BOM	





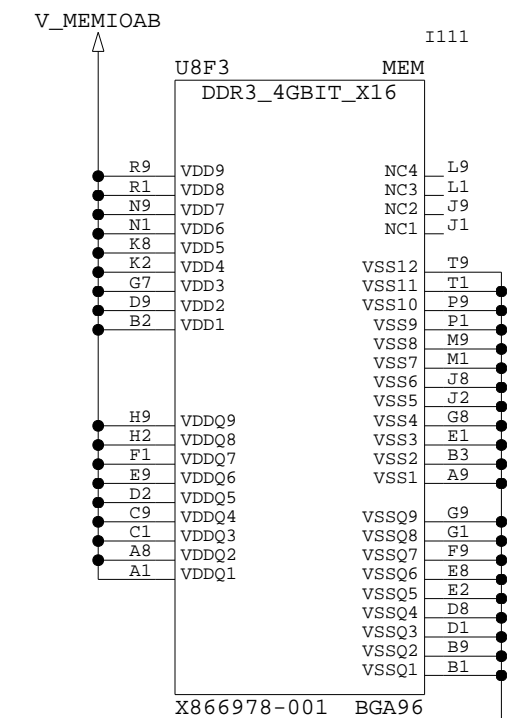
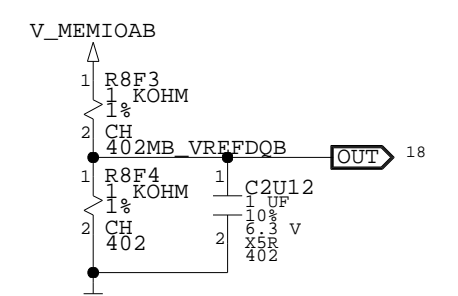
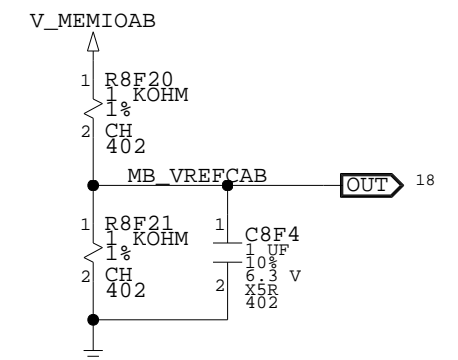
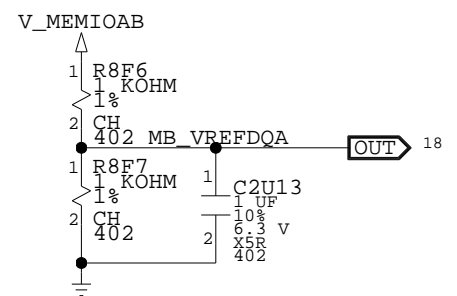
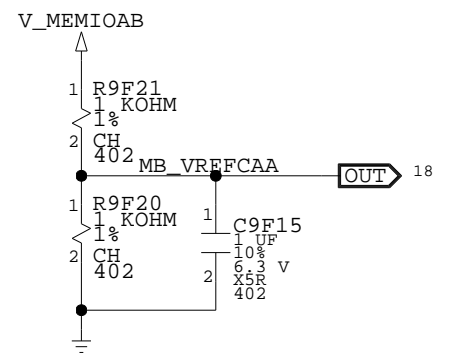
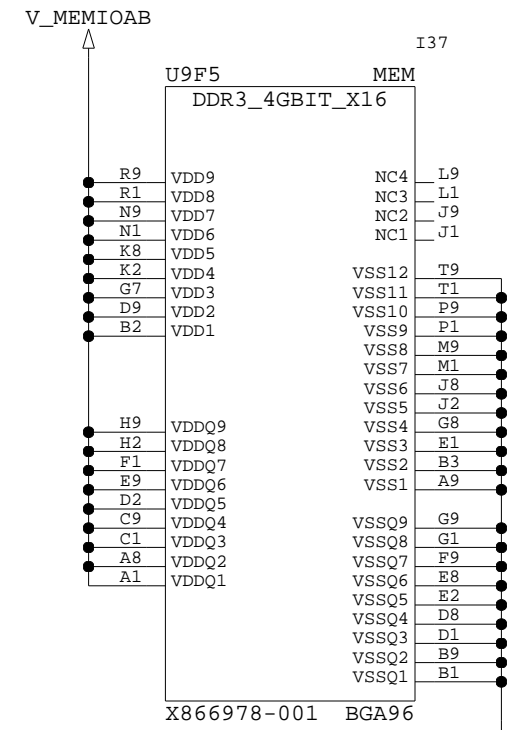
# MEMORY CHANNEL C, DECOUPLING + TERMINATION



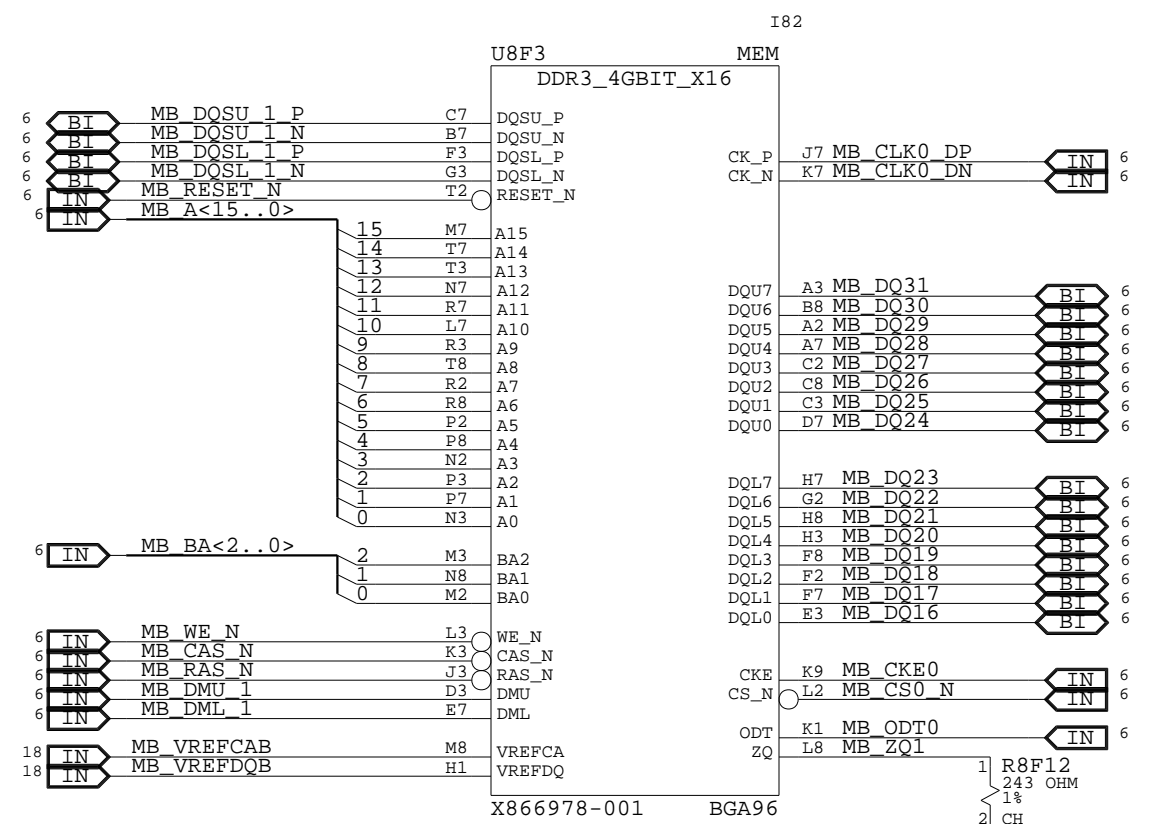
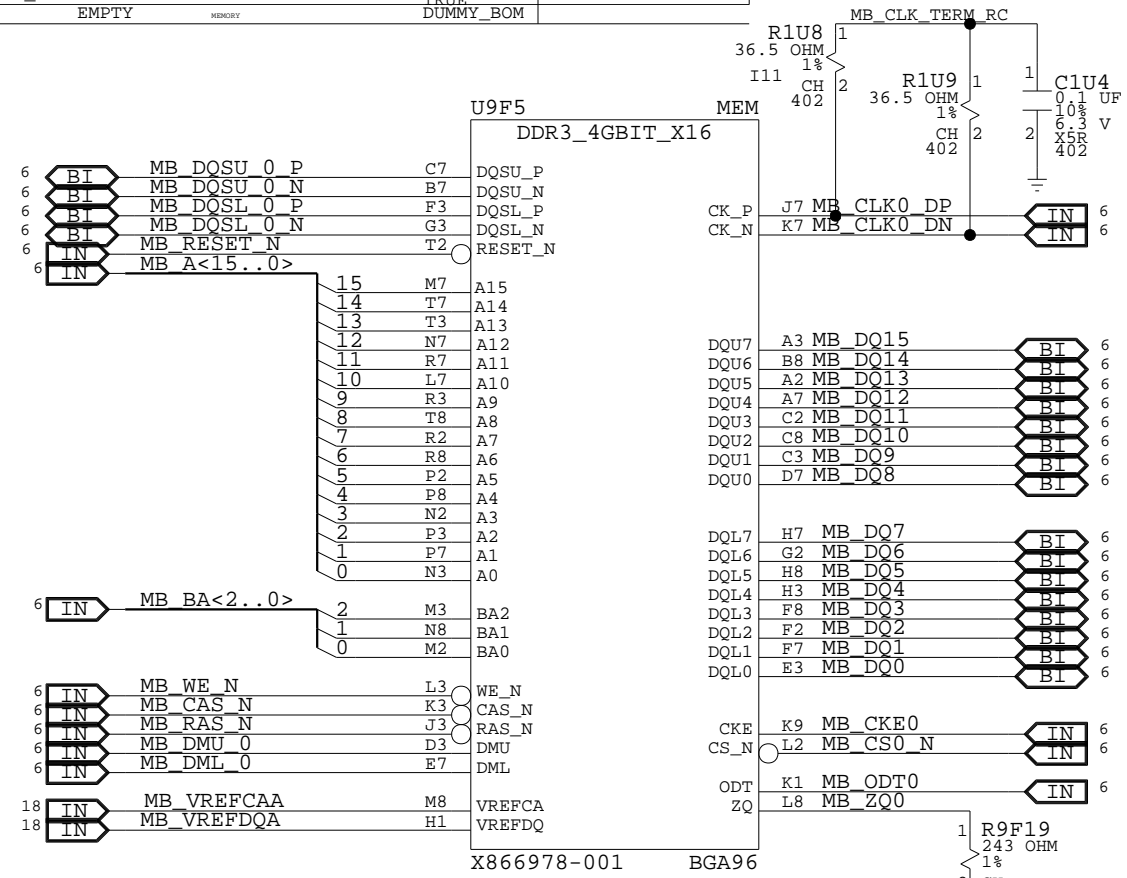
# MEMORY CHANNEL B

BYTE LANE 0  
BYTE LANE 1

BYTE LANE 2  
BYTE LANE 3



MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
U9F5,U8F3	EMPTY	EMPTY		MEMORY	

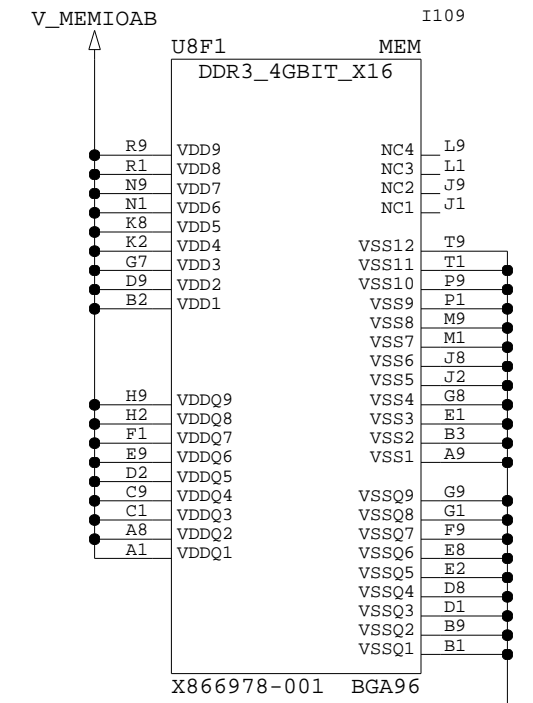
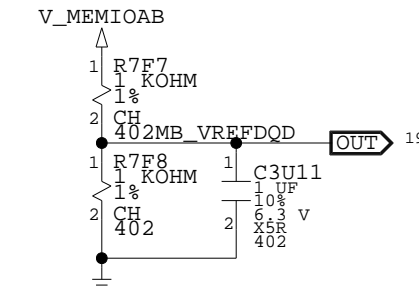
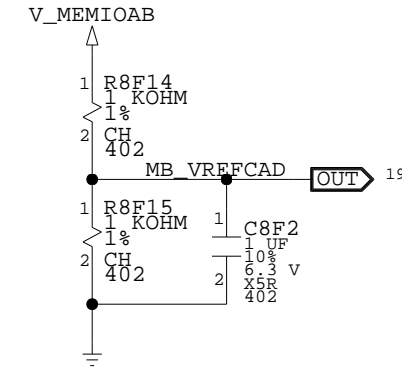
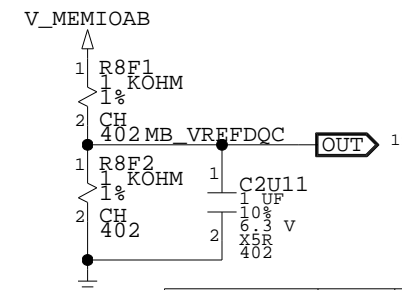
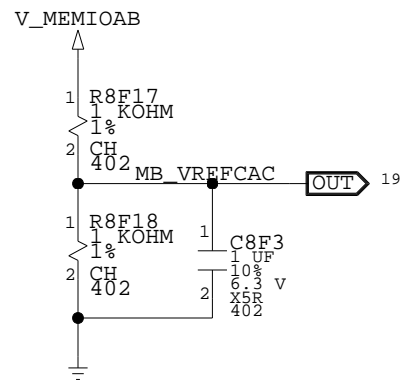
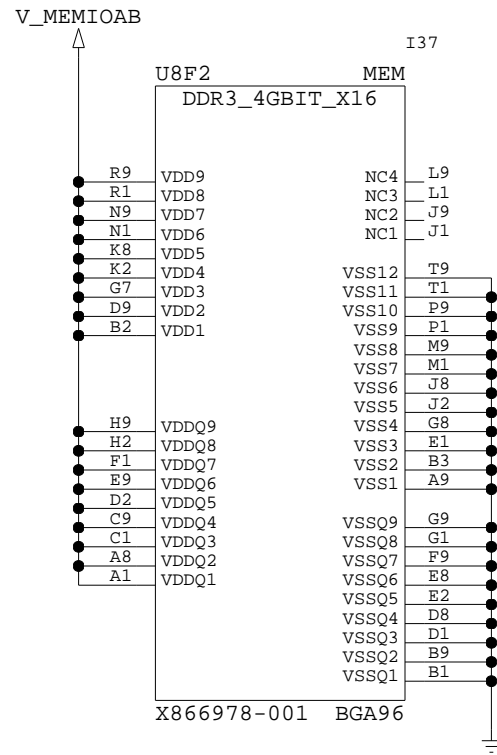


[PAGE\_TITLE=MEMORY PARTITION C, LOW]

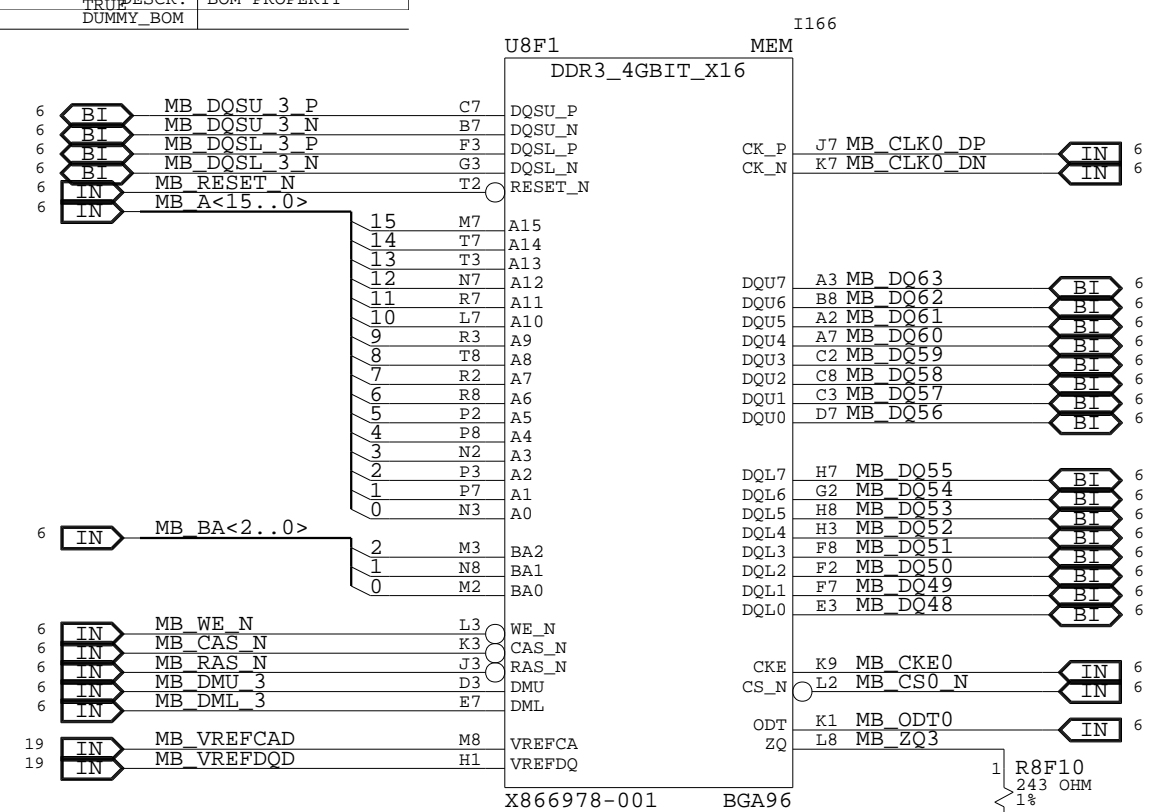
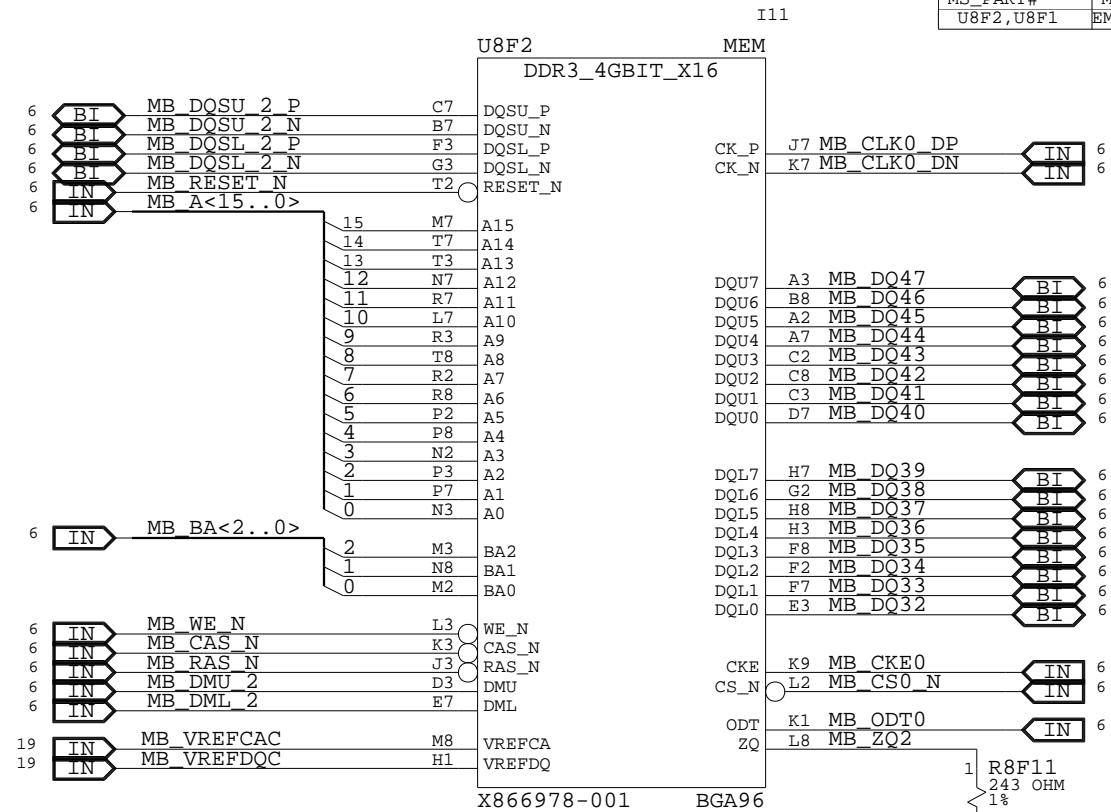
# MEMORY CHANNEL B

BYTE LANE 4  
BYTE LANE 5

BYTE LANE 6  
BYTE LANE 7



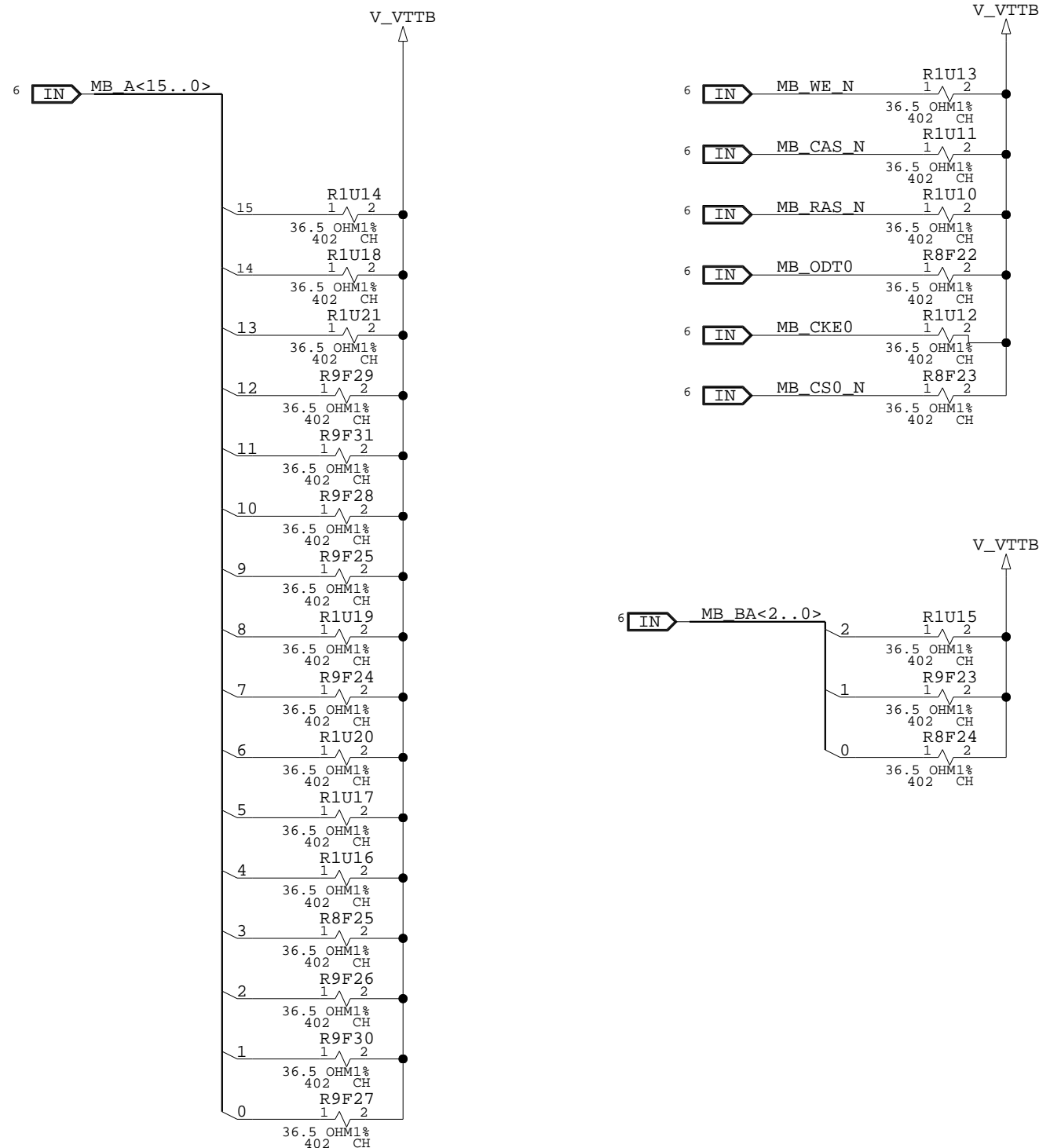
MS_PART#	MATL	REF_DES	TRUP	DESCR.	BOM	PROPERTY
U8F2, U8F1	EMPTY	EMPTY	MEMORY	DUMMY_BOM		



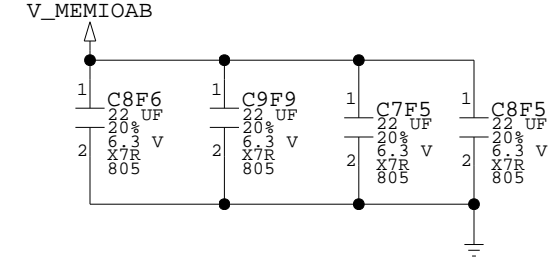
[PAGE\_TITLE=MEMORY PARTITION C, HIGH]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 19/72	CSA PAGE 19/72	FAB M	REV 1.0
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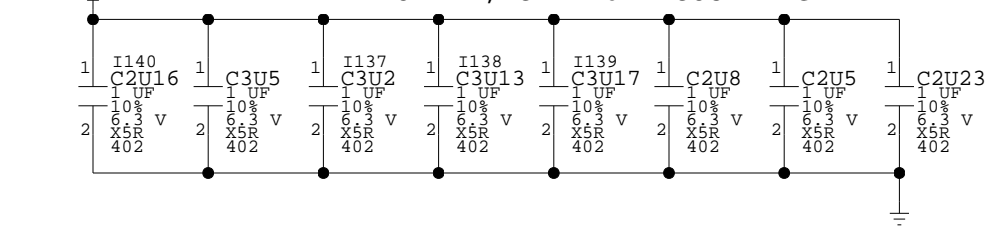
# MEMORY CHANNEL B, DECOUPLING + TERMINATION



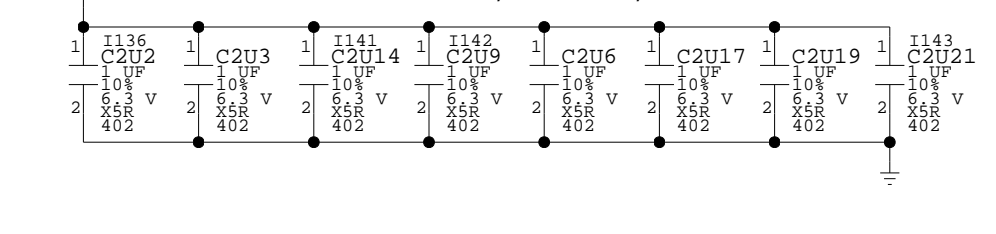
PARTITION B DECOUPLING



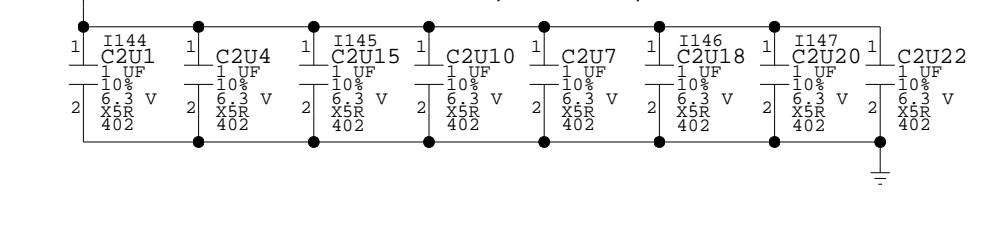
MEMORY B, CHIP 0 DECOUPLING



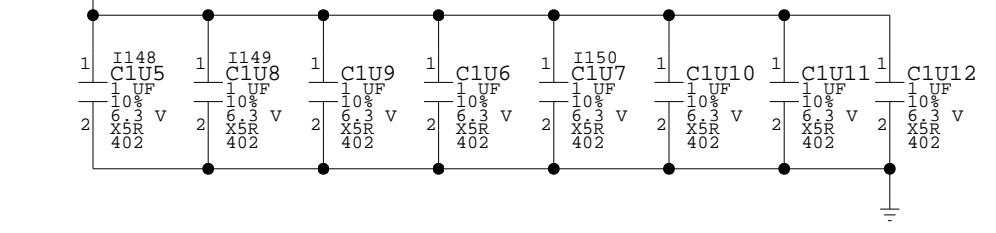
MEMORY B, CHIP 1, DECOUPLING



MEMORY B, CHIP 2, DECOUPLING



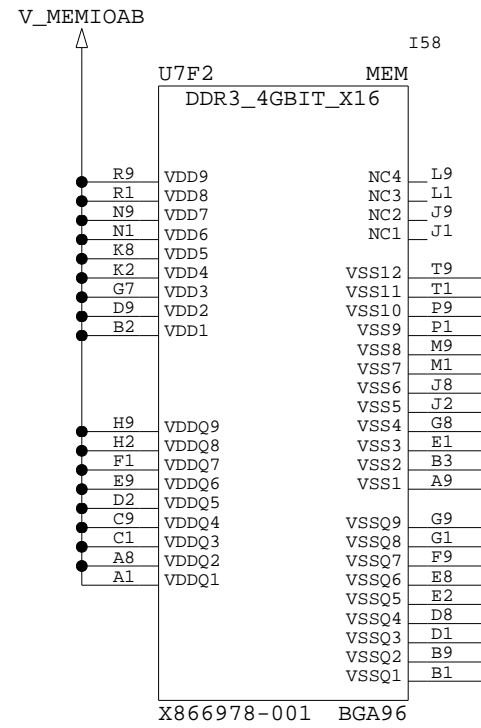
MEMORY B, CHIP 3, DECOUPLING



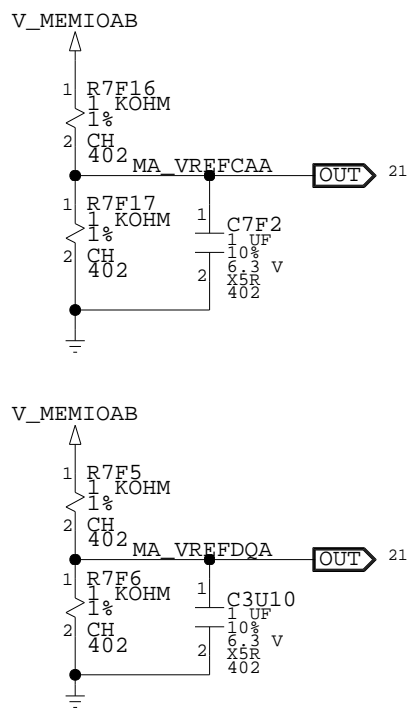
[PAGE\_TITLE=MEMORY PARTITION C, DECOUPLING, TERMINATION]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 20/72	CSA PAGE 20/72	FAB M	REV 1.0
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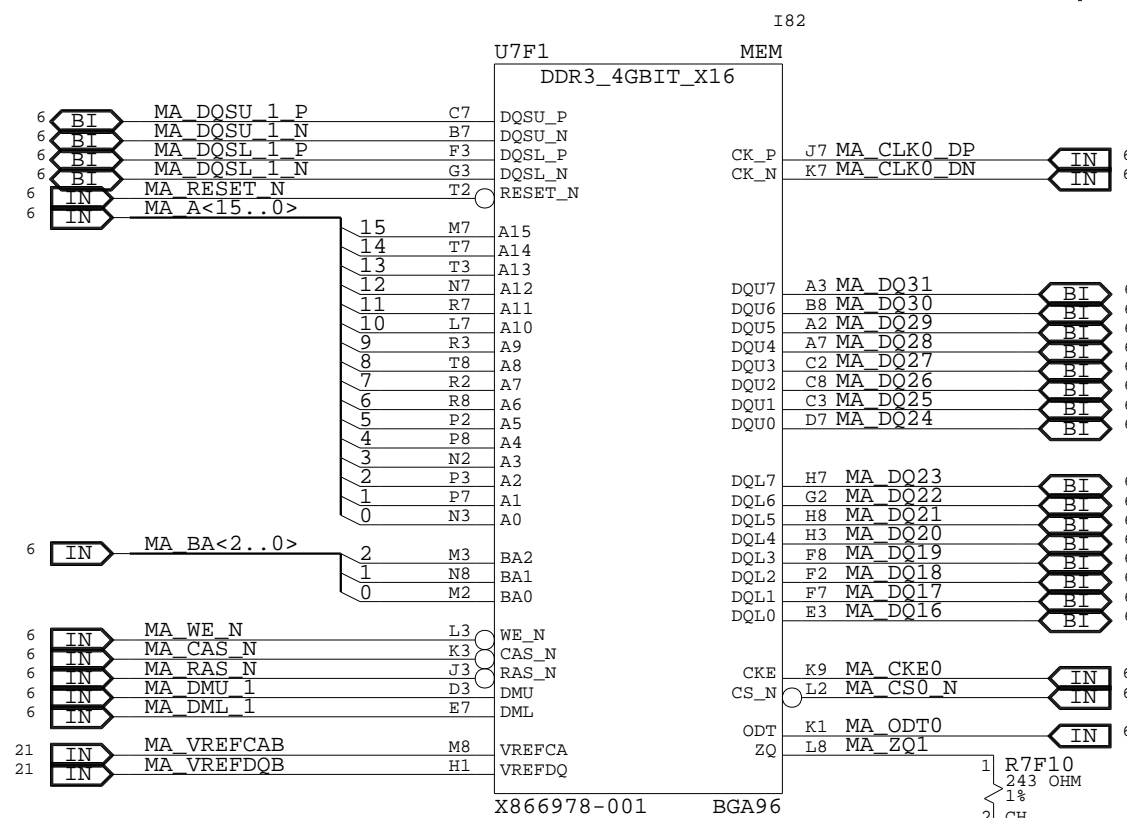
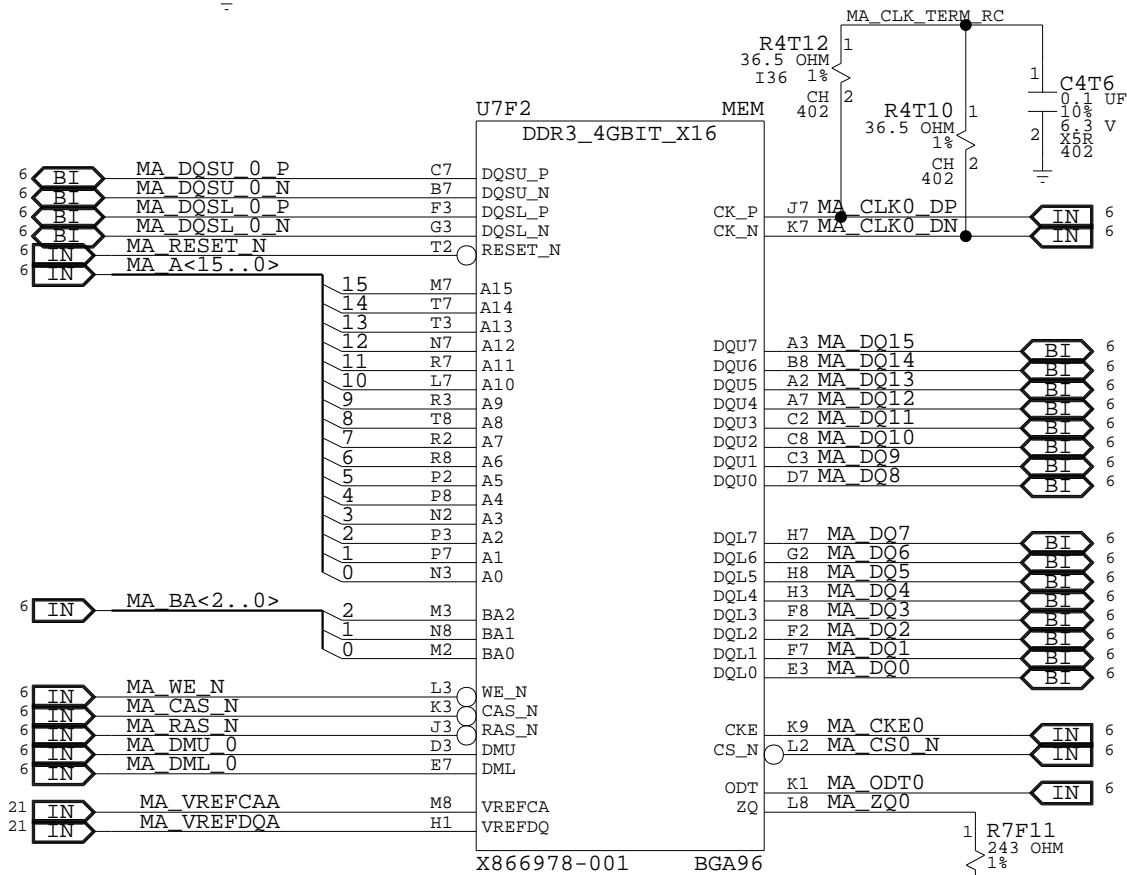
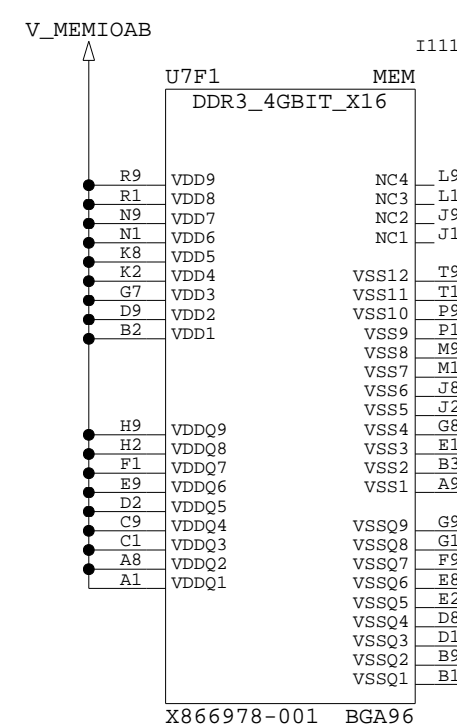
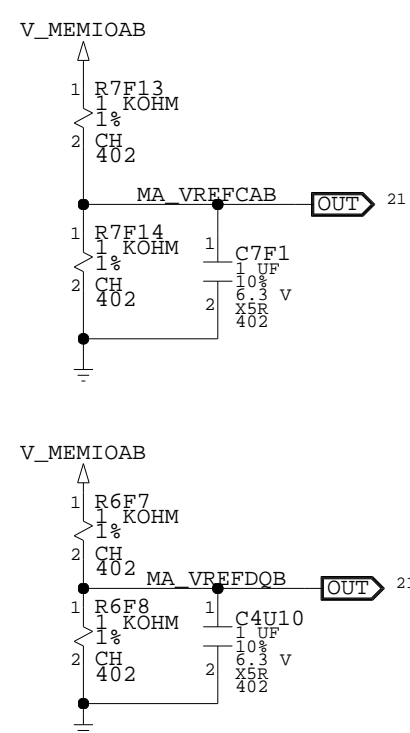
# MEMORY CHANNEL A



BYTE LANE 0  
BYTE LANE 1



BYTE LANE 2  
BYTE LANE 3



MS_PART#	MATL	REF_DES	TRUP_DESCR.	BOM_PROPERTY
U7F2,U7F1	EMPTY	EMPTY	MEMORY	DUMMY_BOM

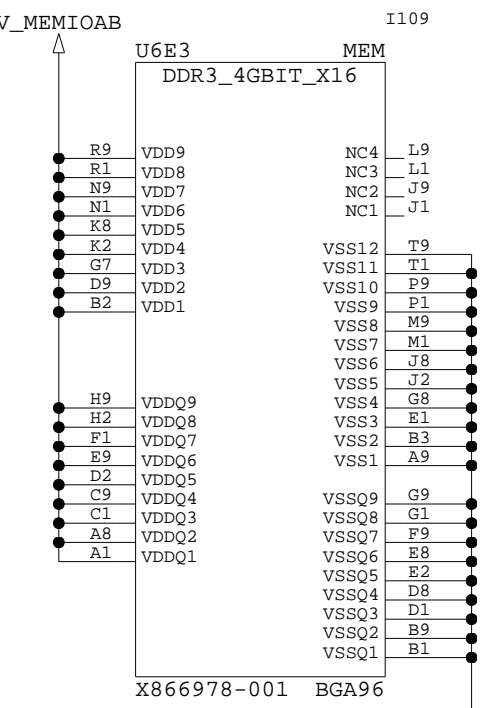
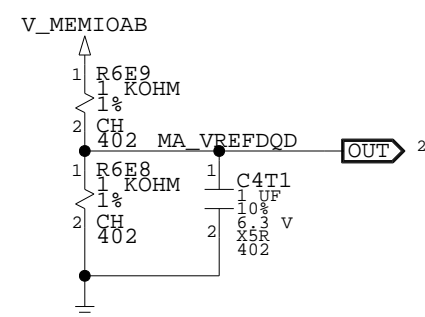
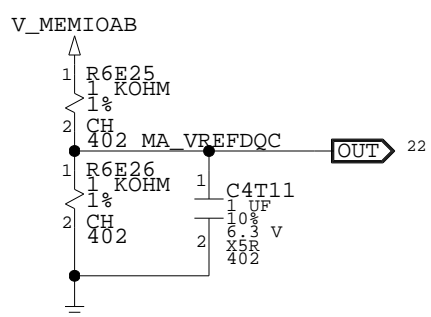
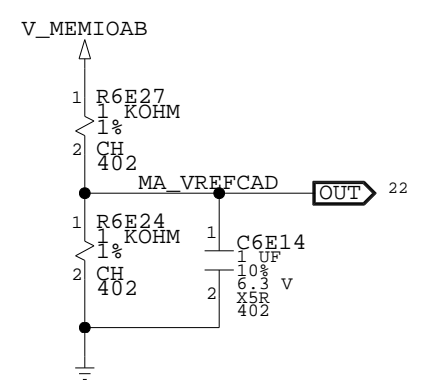
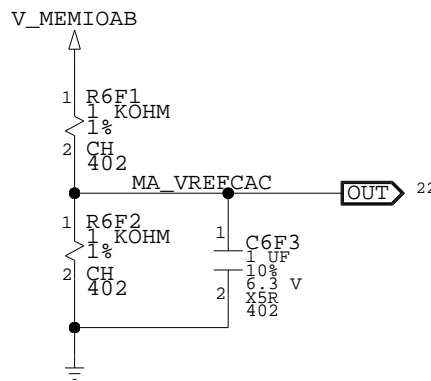
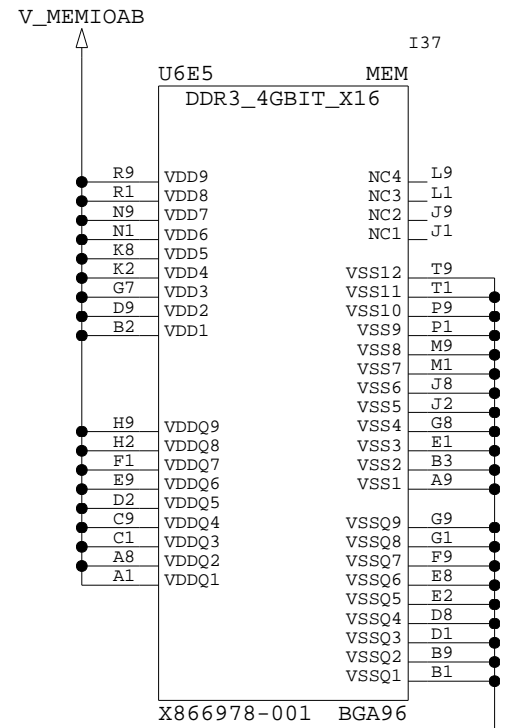
[PAGE\_TITLE=MEMORY PARTITION D, LOW]

MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	GREYBULL_RETAIL	21/72	21/72	M	1.0

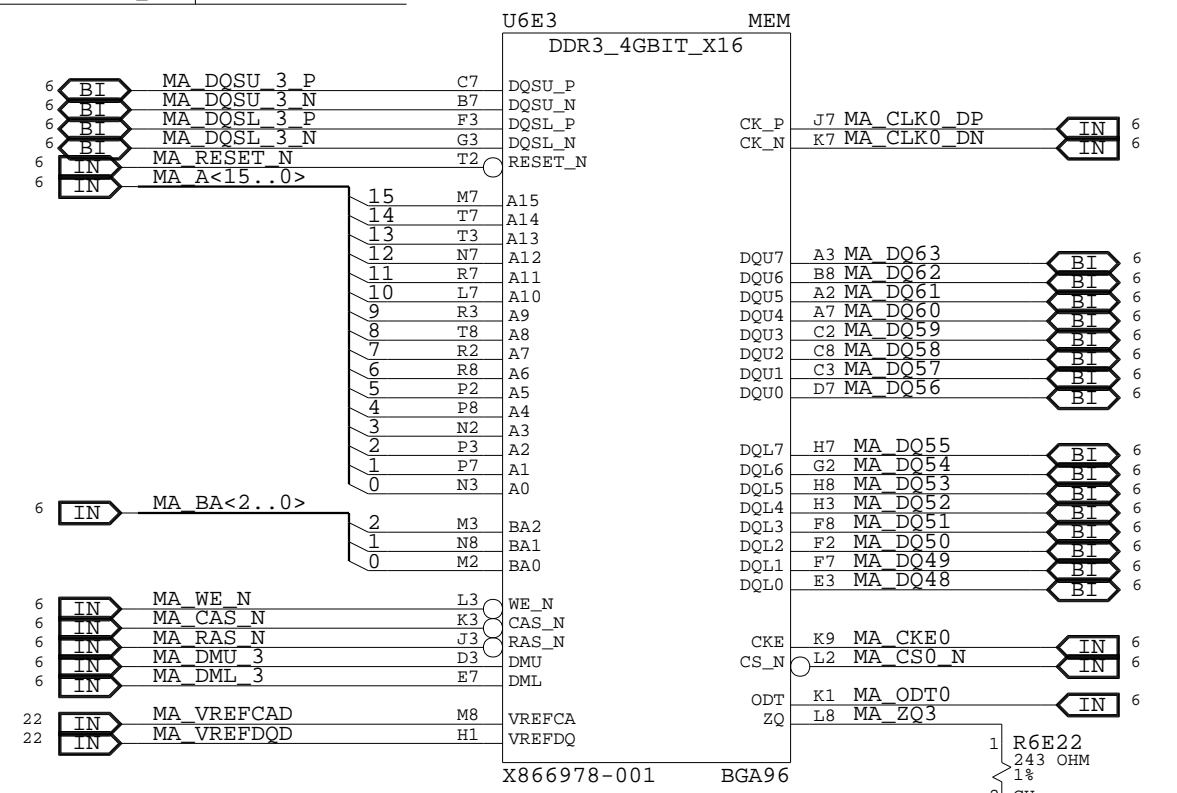
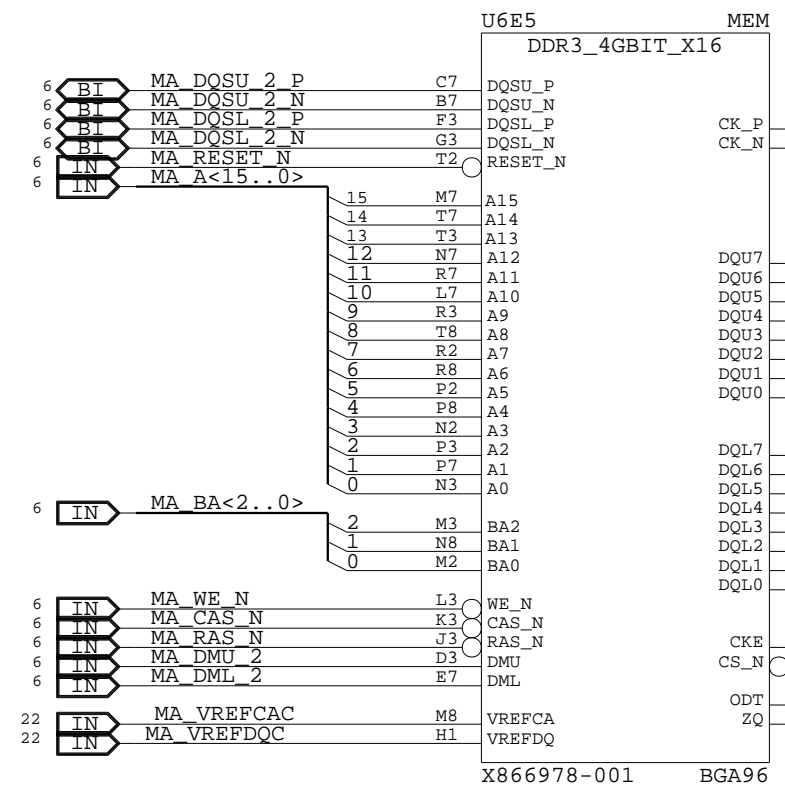
# MEMORY CHANNEL A

BYTE LANE 4  
BYTE LANE 5

BYTE LANE 6  
BYTE LANE 7

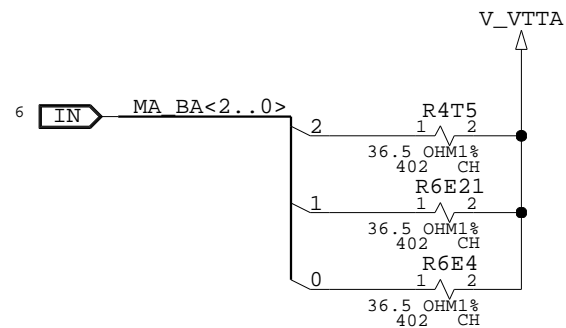
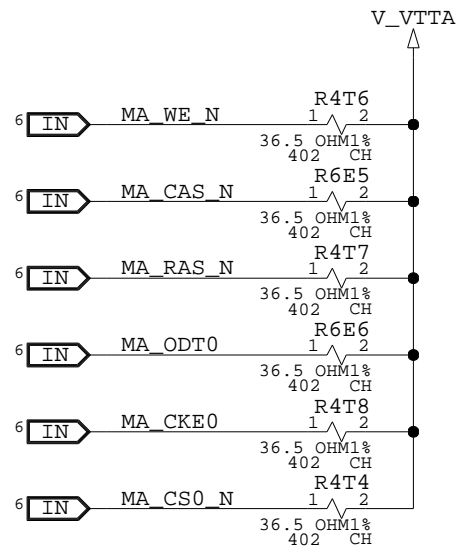
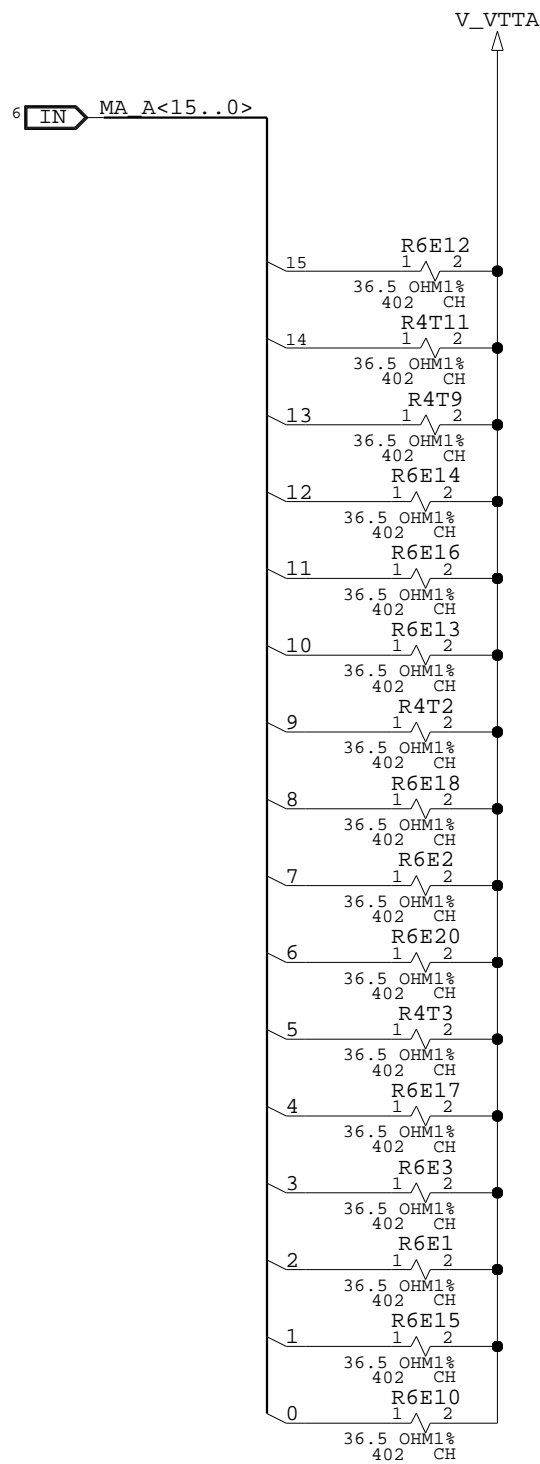


MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
U6E5, U6E3	EMPTY	EMPTY	MEMORY	DUMMY_BOM	

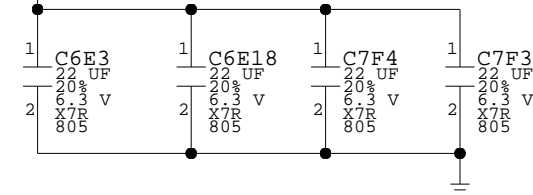


[PAGE\_TITLE=MEMORY PARTITION D, HIGH]

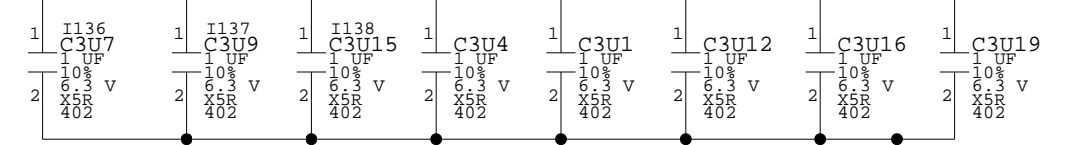
# MEMORY CHANNEL A, DECOUPLING + TERMINATION



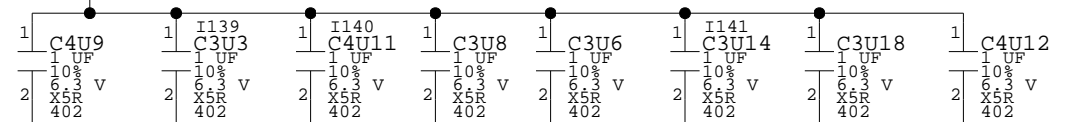
PARTITION A DECOUPLING  
V\_MEMIOAB



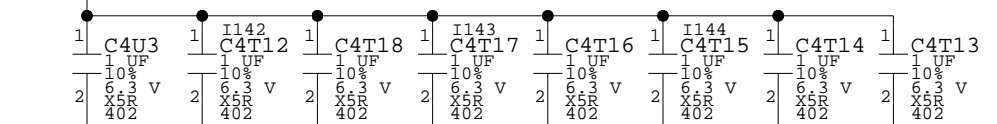
V\_MEMIOAB MEMORY A, CHIP 0 DECOUPLING



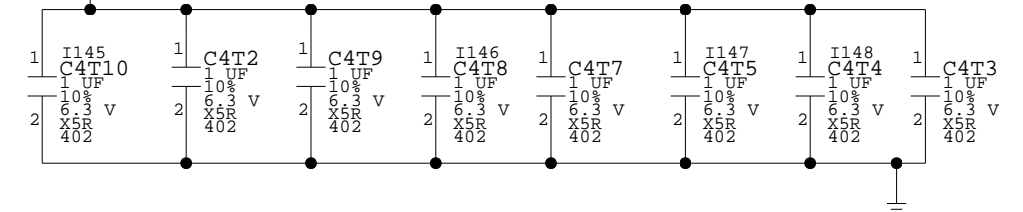
V\_MEMIOAB MEMORY A, CHIP 1, DECOUPLING



V\_MEMIOAB MEMORY A, CHIP 2, DECOUPLING



V\_MEMIOAB MEMORY A, CHIP 3, DECOUPLING



[PAGE\_TITLE=MEMORY PARTITION D, DECOUPLING, TERMINATION]

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 23/72	CSA PAGE 23/72	FAB M	REV 1.0
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# KIC, USB

D

C

B

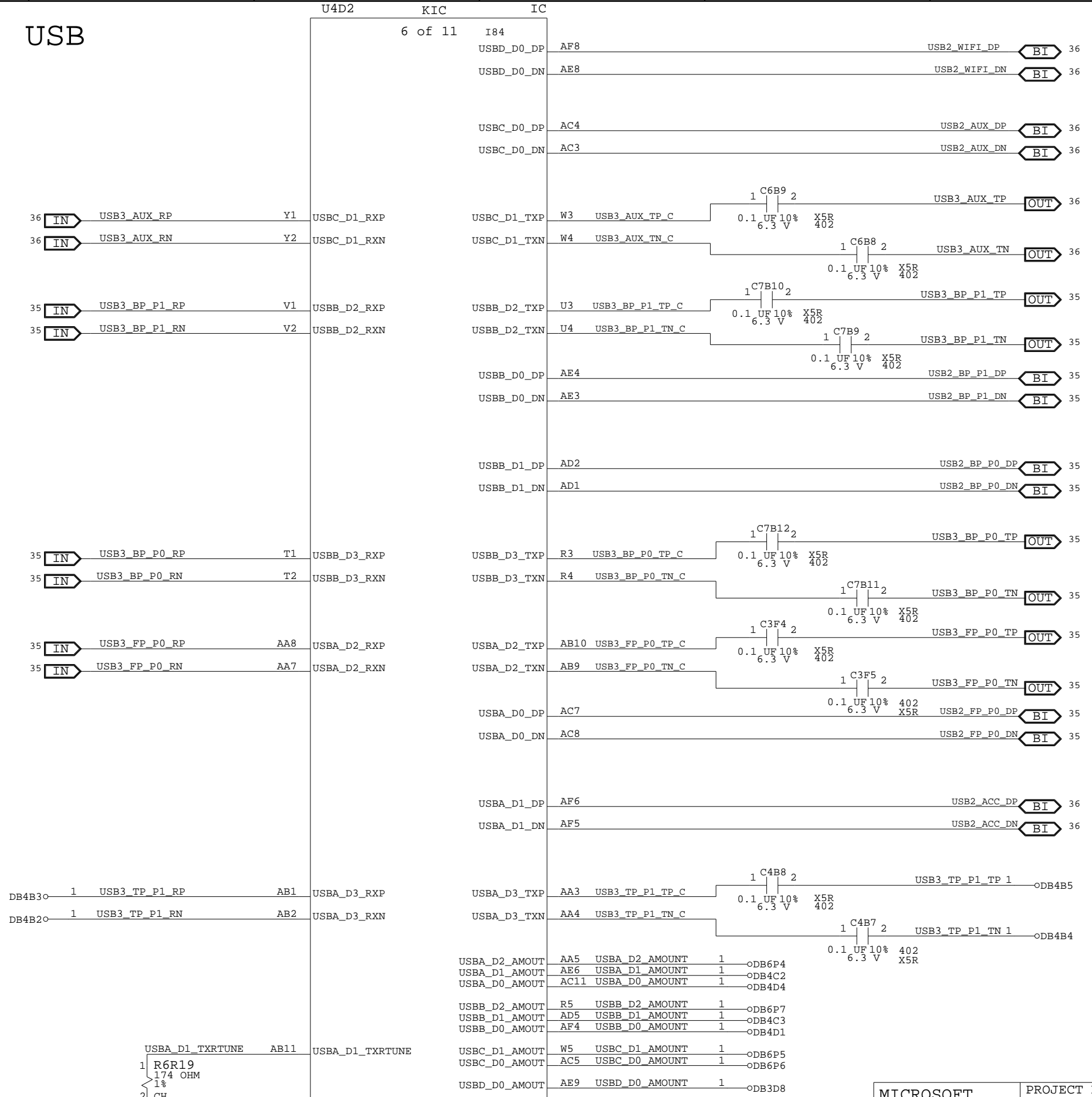
A

D

C

B

A

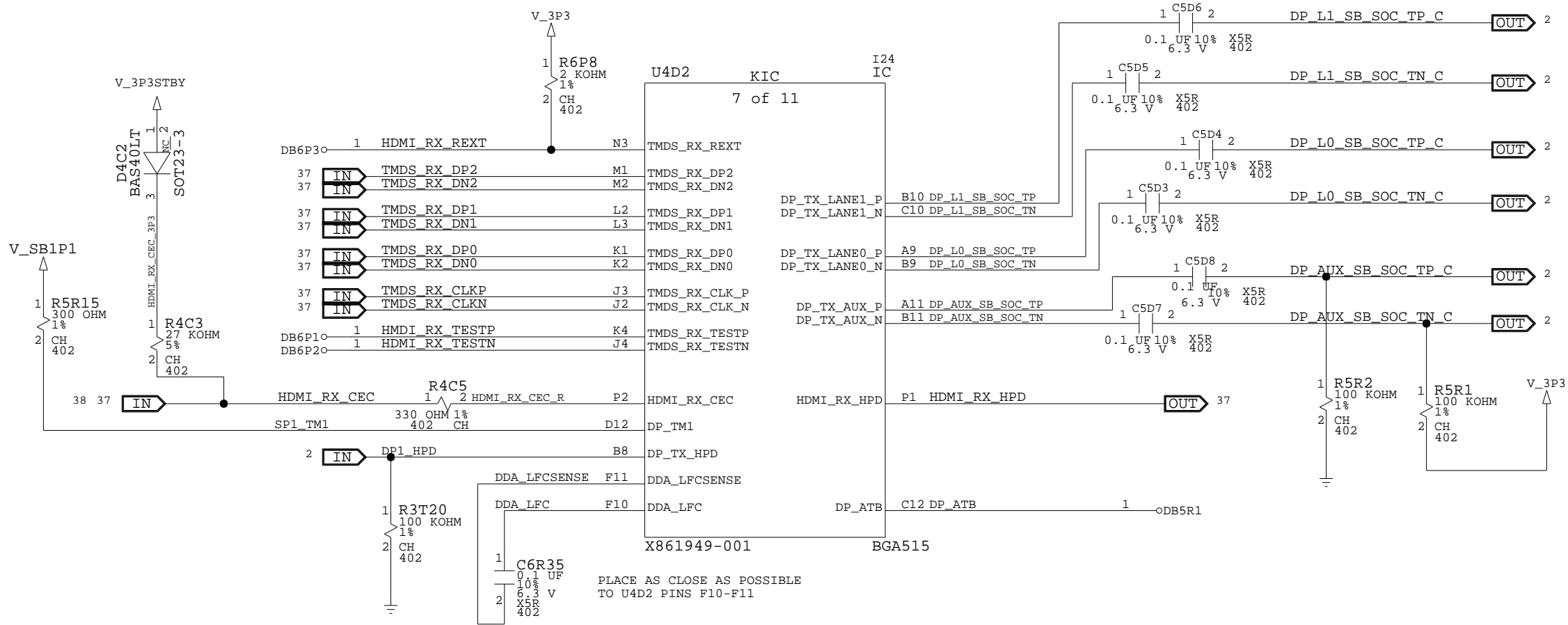
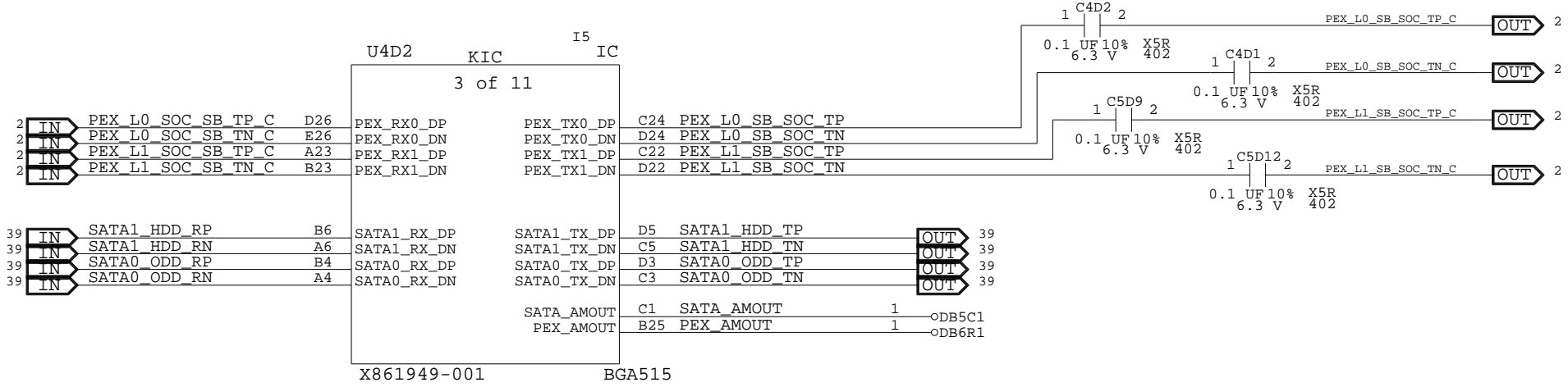


X861949-001 BGA515

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 24/72	CSA PAGE 24/72	FAB M	REV 1.0
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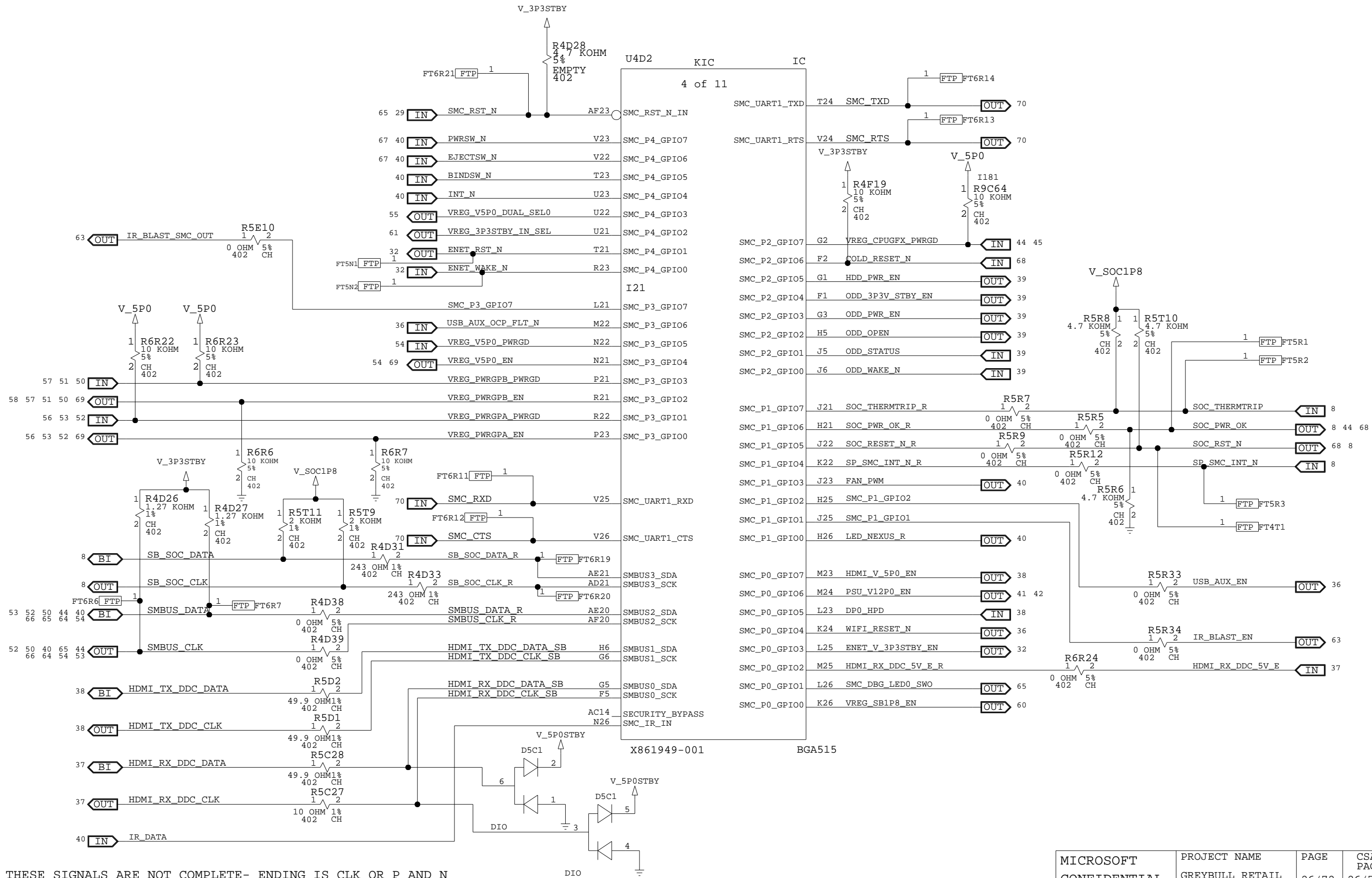


# KIC, PCIE X + SATA + VIDEO



MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
U4D2	EMPTY	EMPTY	***	DUMMY_BOM	

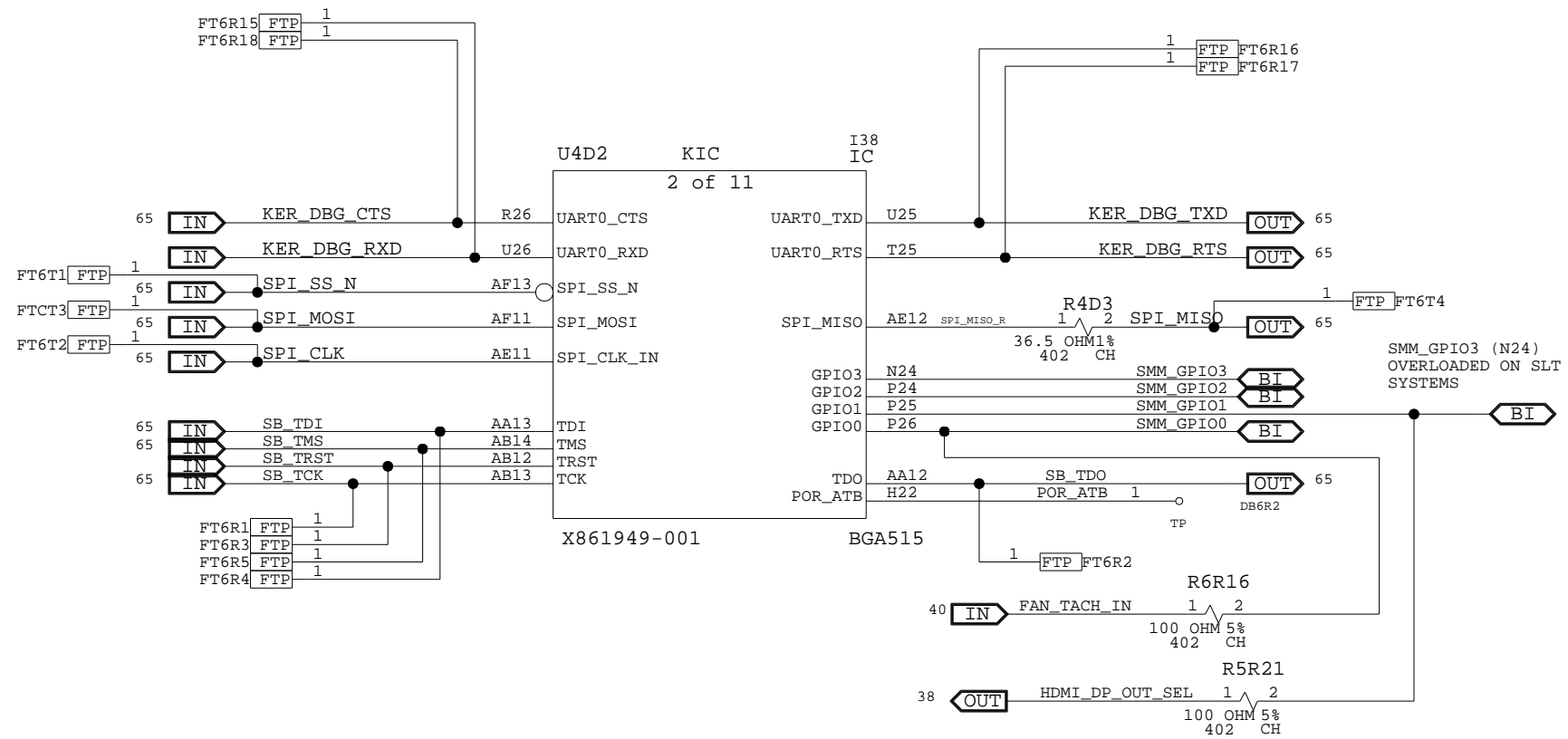
# KIC, SMC



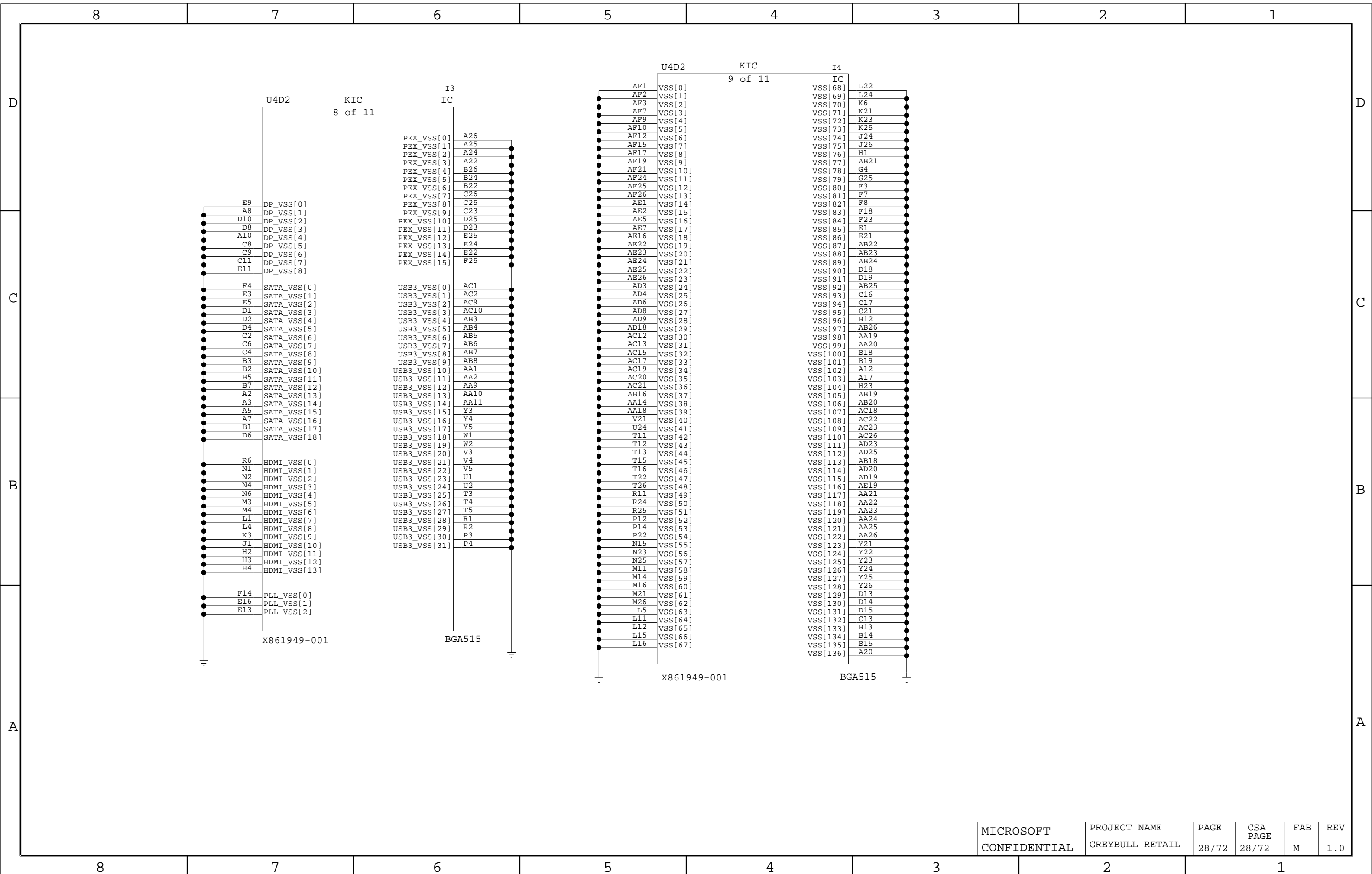
THESE SIGNALS ARE NOT COMPLETE- ENDING IS CLK OR P AND N

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 26/72	CSA PAGE 26/72	FAB M	REV 1.0
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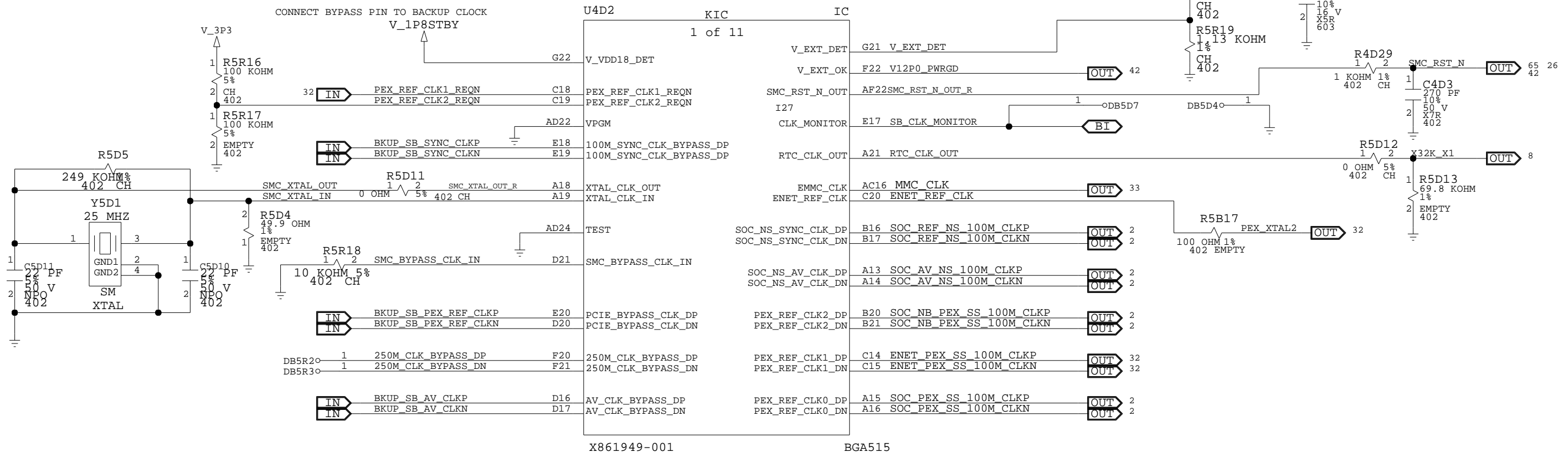
# KIC, FACET



MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 27/72	CSA PAGE 27/72	FAB M	REV 1.0
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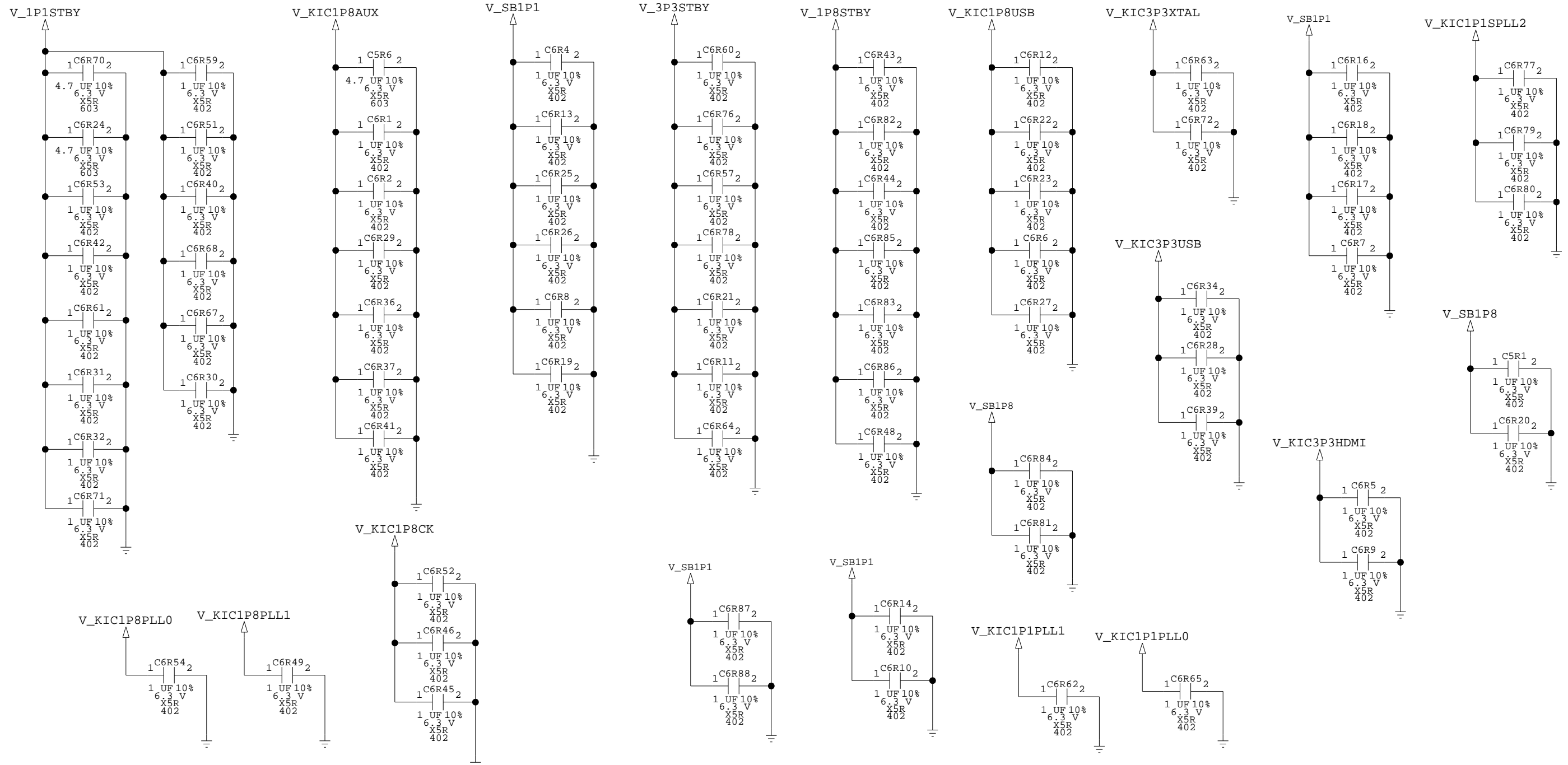


# KIC, CLOCKS + STRAPPING + POR



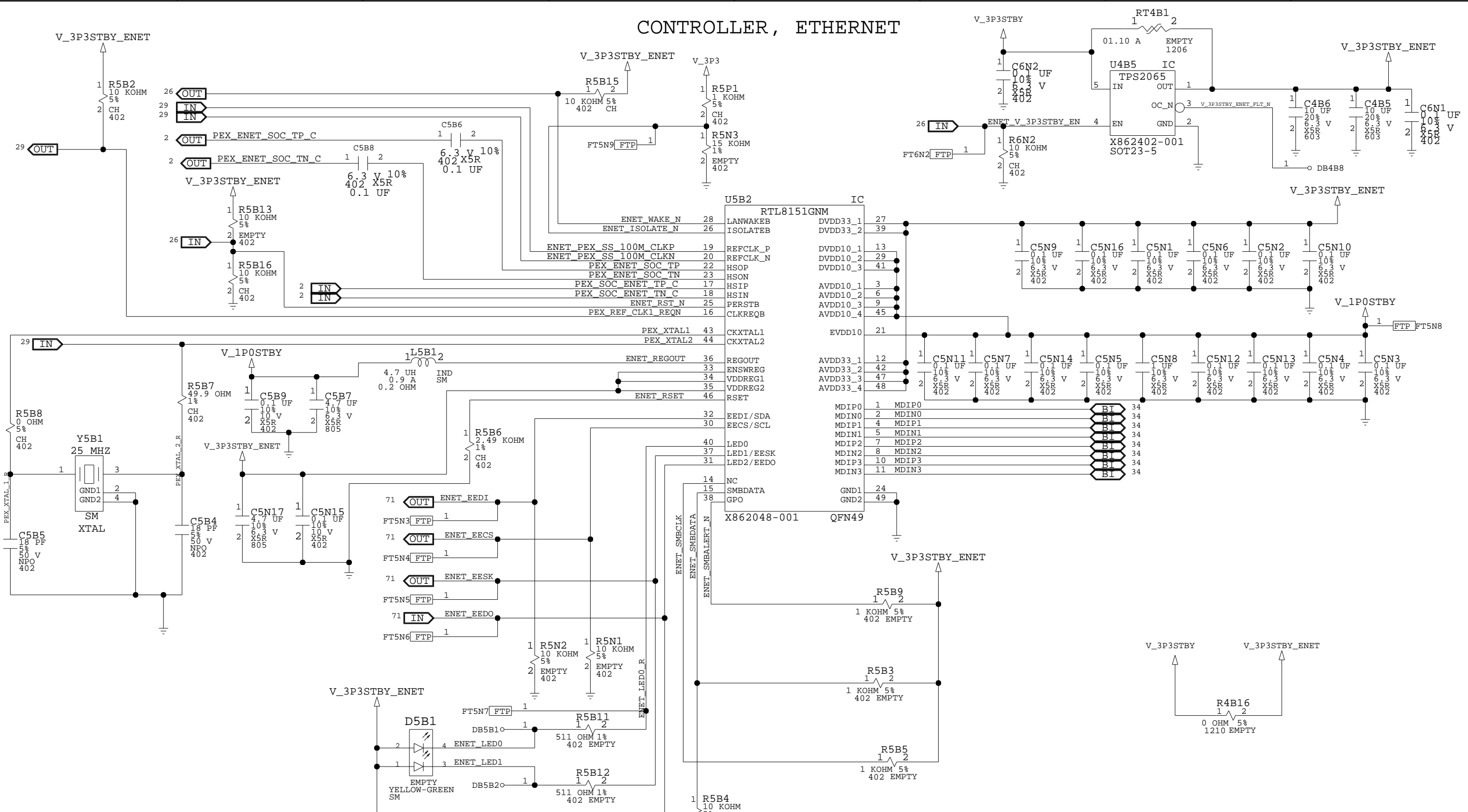


# KIC, DECOUPLING



MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	REV
CONFIDENTIAL	GREYBULL_RETAIL	31/72	PAGE	M	1.0

# CONTROLLER, ETHERNET

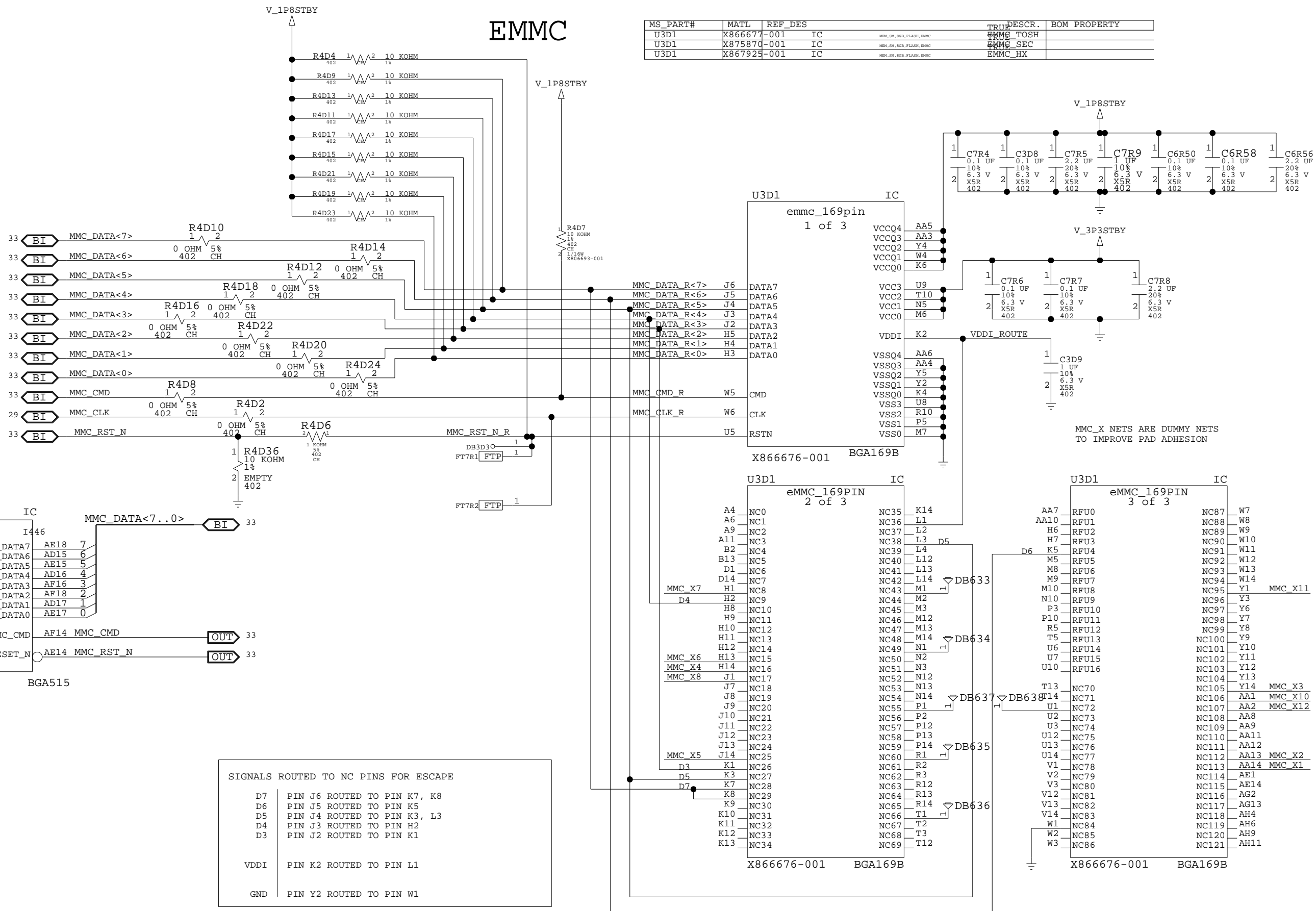


EEPROM CONFIG (93C66)	CHIPSET	U5B1	C5B3	R5B3	R5B4	R5N2	R5B9	R5B5
GREYBULL WITH EEPROM	RTL8151GNM	STUFF	STUFF	STUFF	EMPTY	STUFF	EMPTY	EMPTY
GREYBULL W/O EEPROM	RTL8151GNM	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

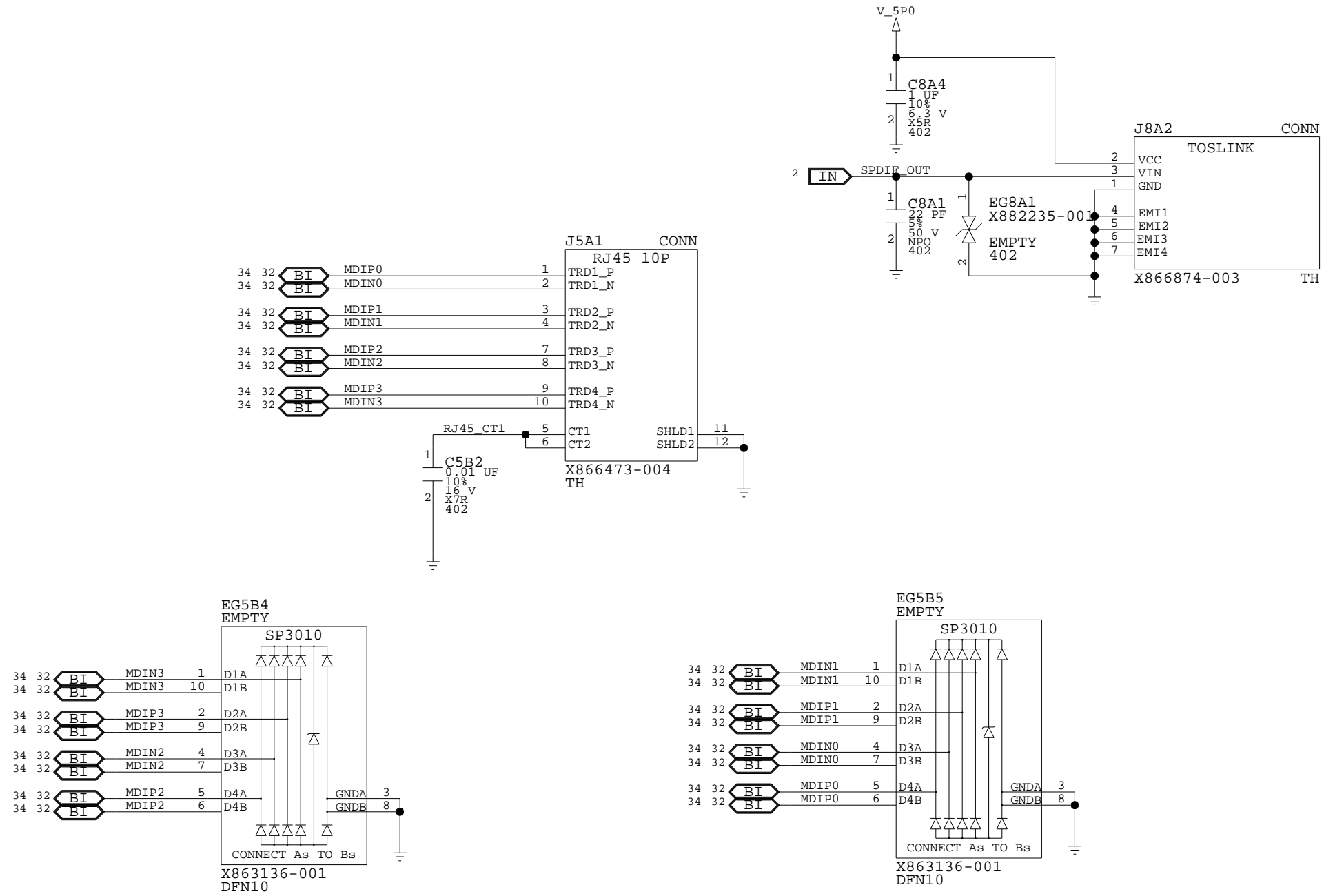


# EMMC

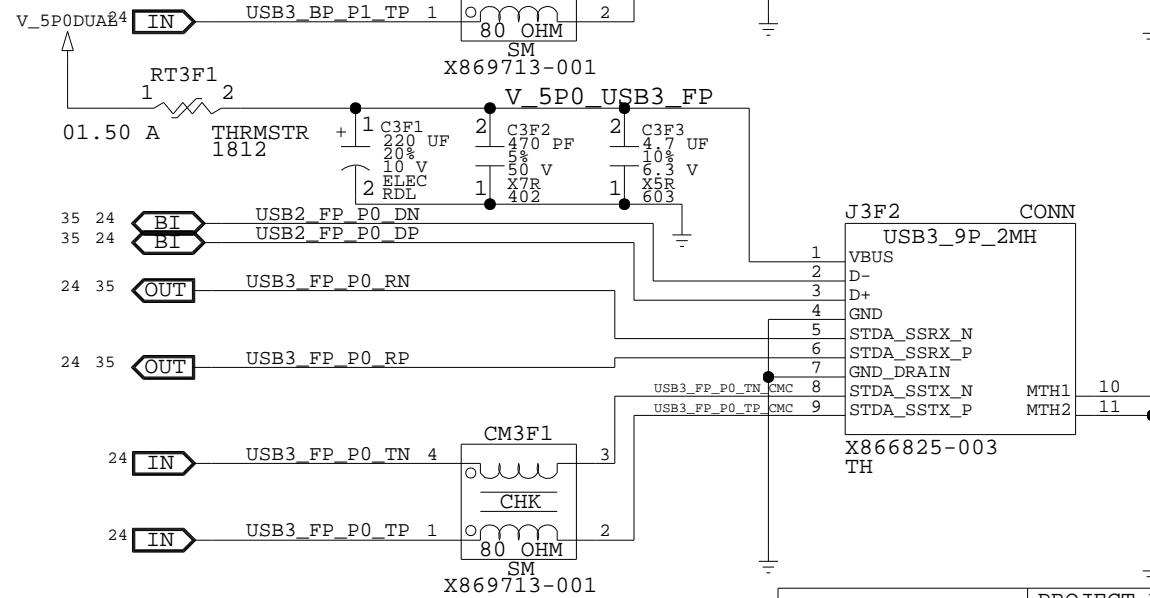
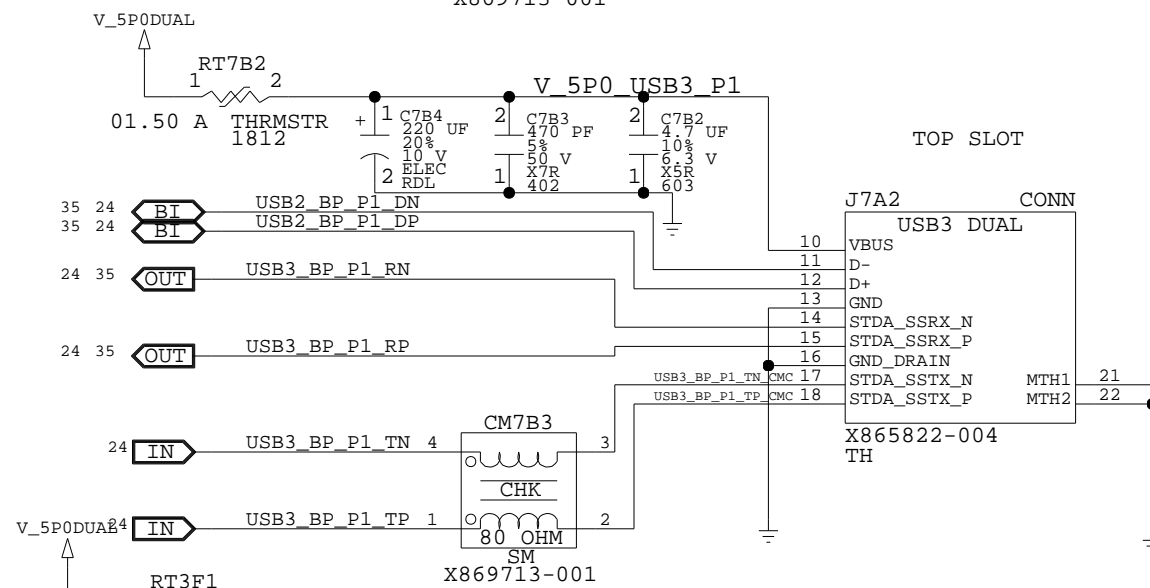
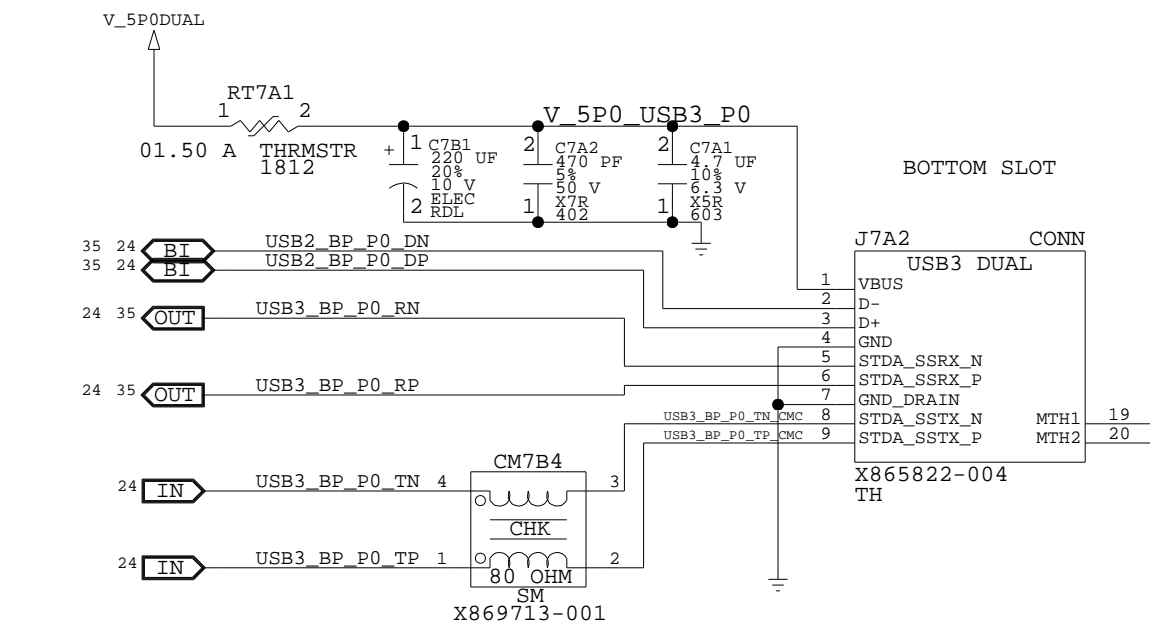
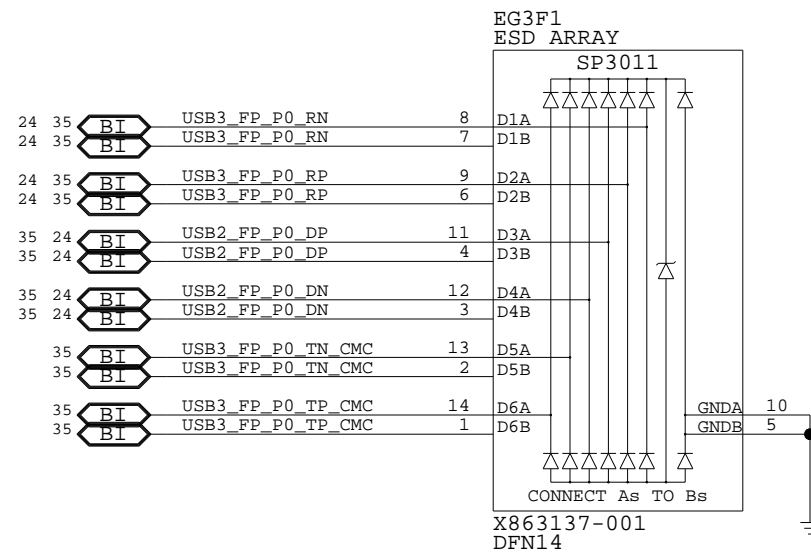
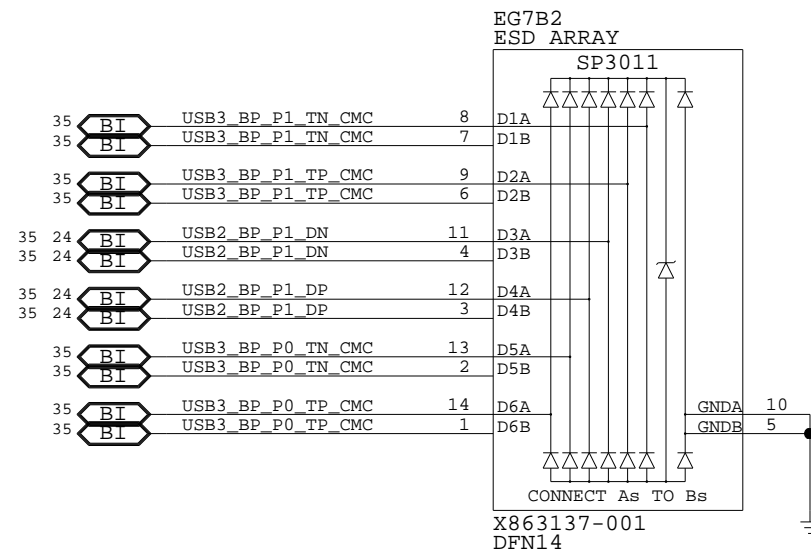
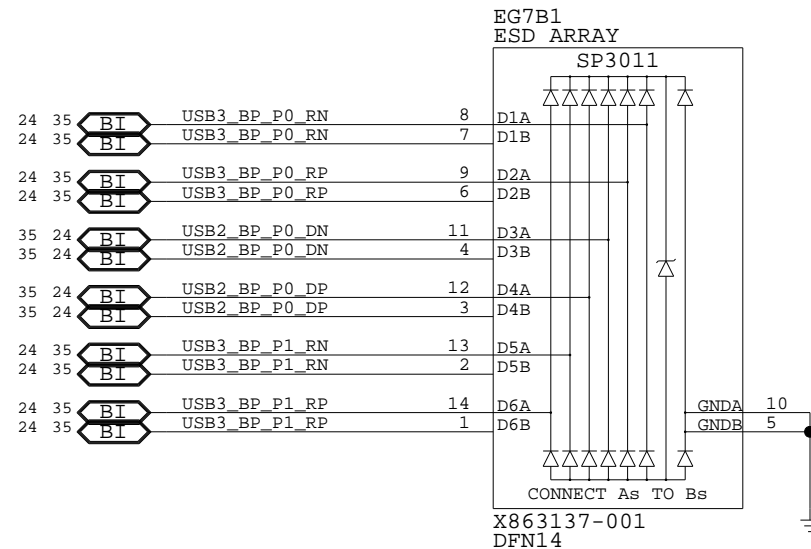
MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
U3D1	X866677-001	IC	EMMC_TOSH		
U3D1	X875870-001	IC	EMMC_SEC		
U3D1	X867925-001	IC	EMMC_HX		



# CONN, RJ45 + TOSLINK

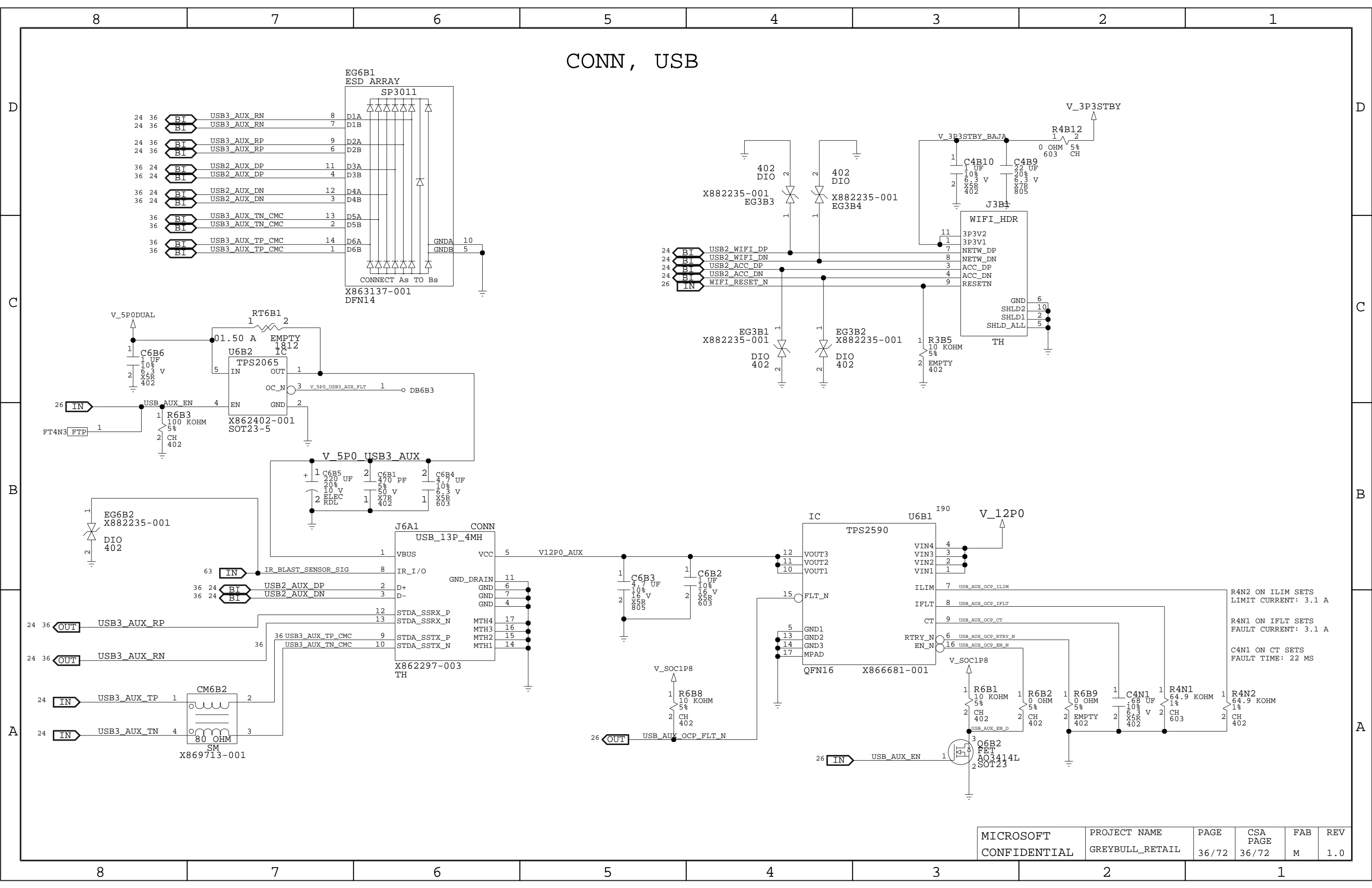


# CONN, USB



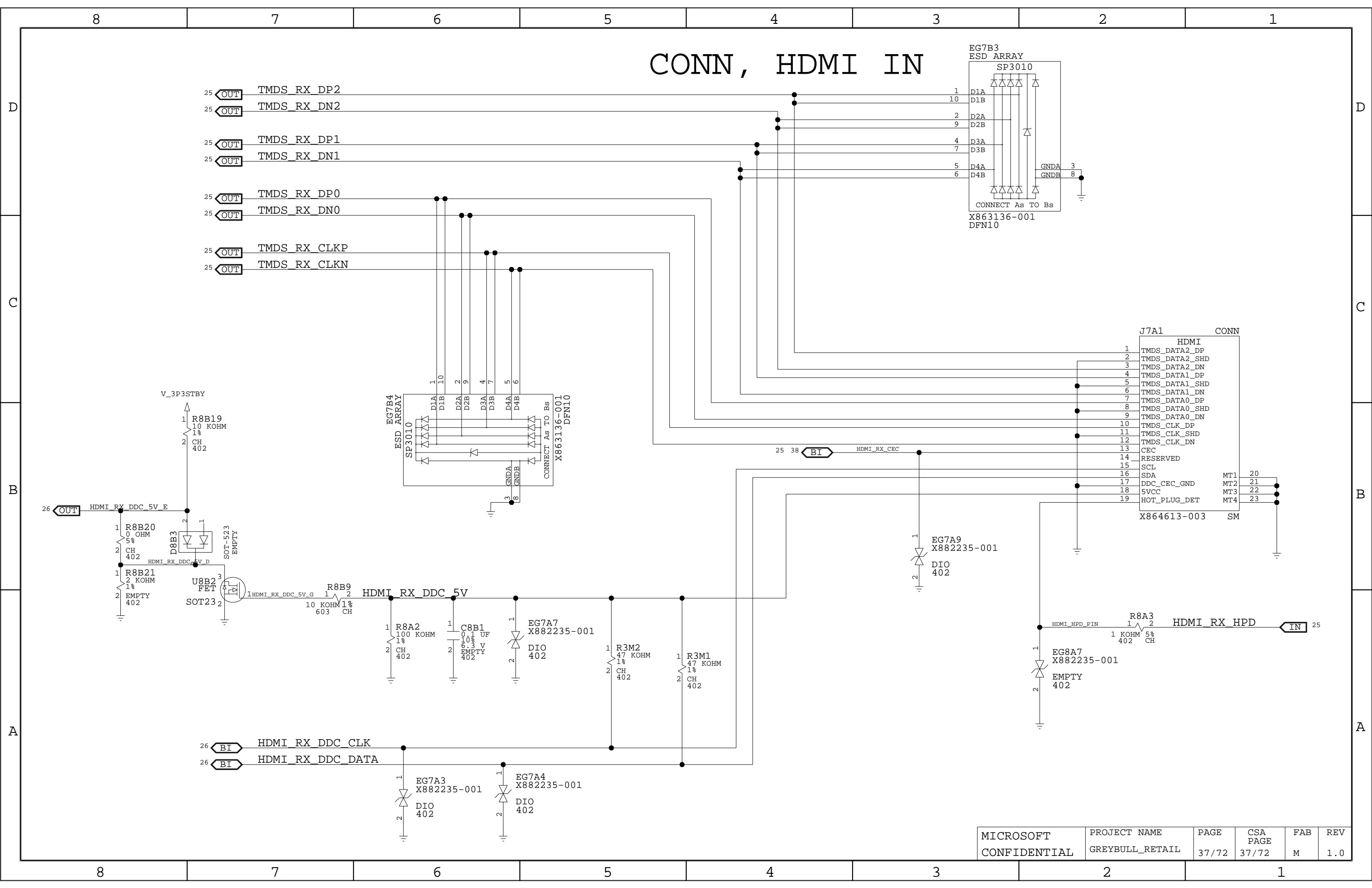
MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	REV
CONFIDENTIAL	GREYBULL_RETAIL	35/72	35/72	M	1.0

# CONN, USB

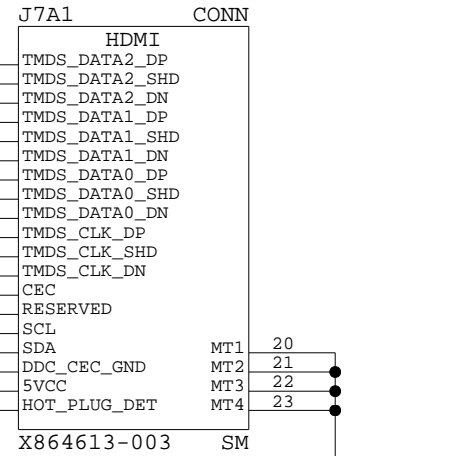
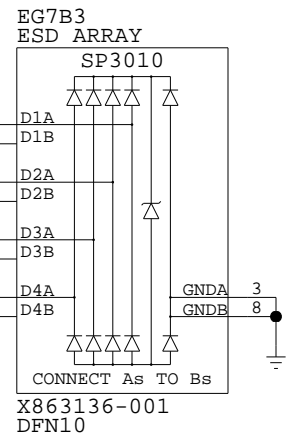


MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 36/72	CSA PAGE 36/72	FAB M	REV 1.0
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# CONN, HDMI IN

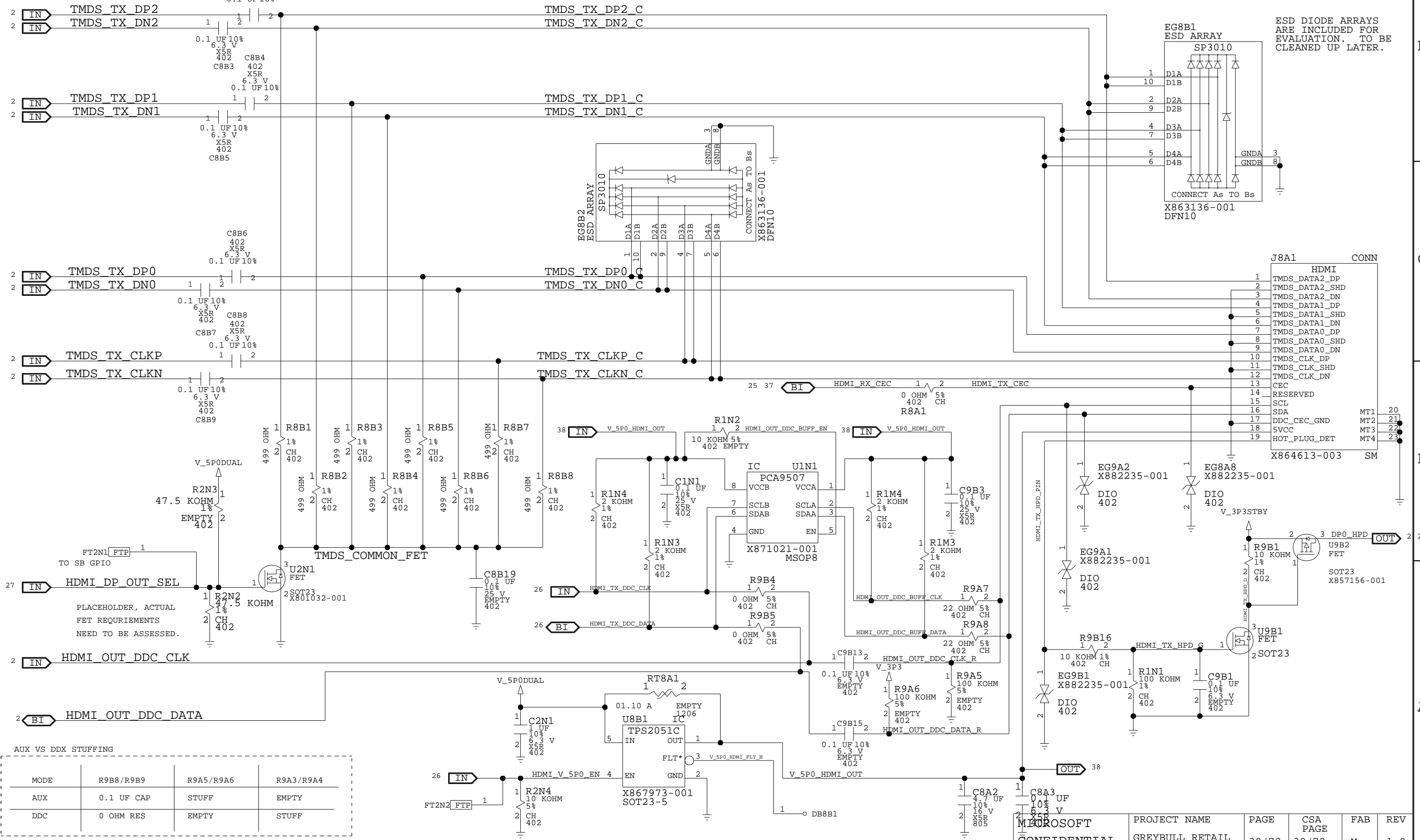


- 25 OUT TMDS RX DP2
- 25 OUT TMDS RX DN2
- 25 OUT TMDS RX DP1
- 25 OUT TMDS RX DN1
- 25 OUT TMDS RX DP0
- 25 OUT TMDS RX DN0
- 25 OUT TMDS RX CLKP
- 25 OUT TMDS RX CLKN



MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 37/72	CSA PAGE 37/72	FAB M	REV 1.0
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# CONN, HDMI OUT

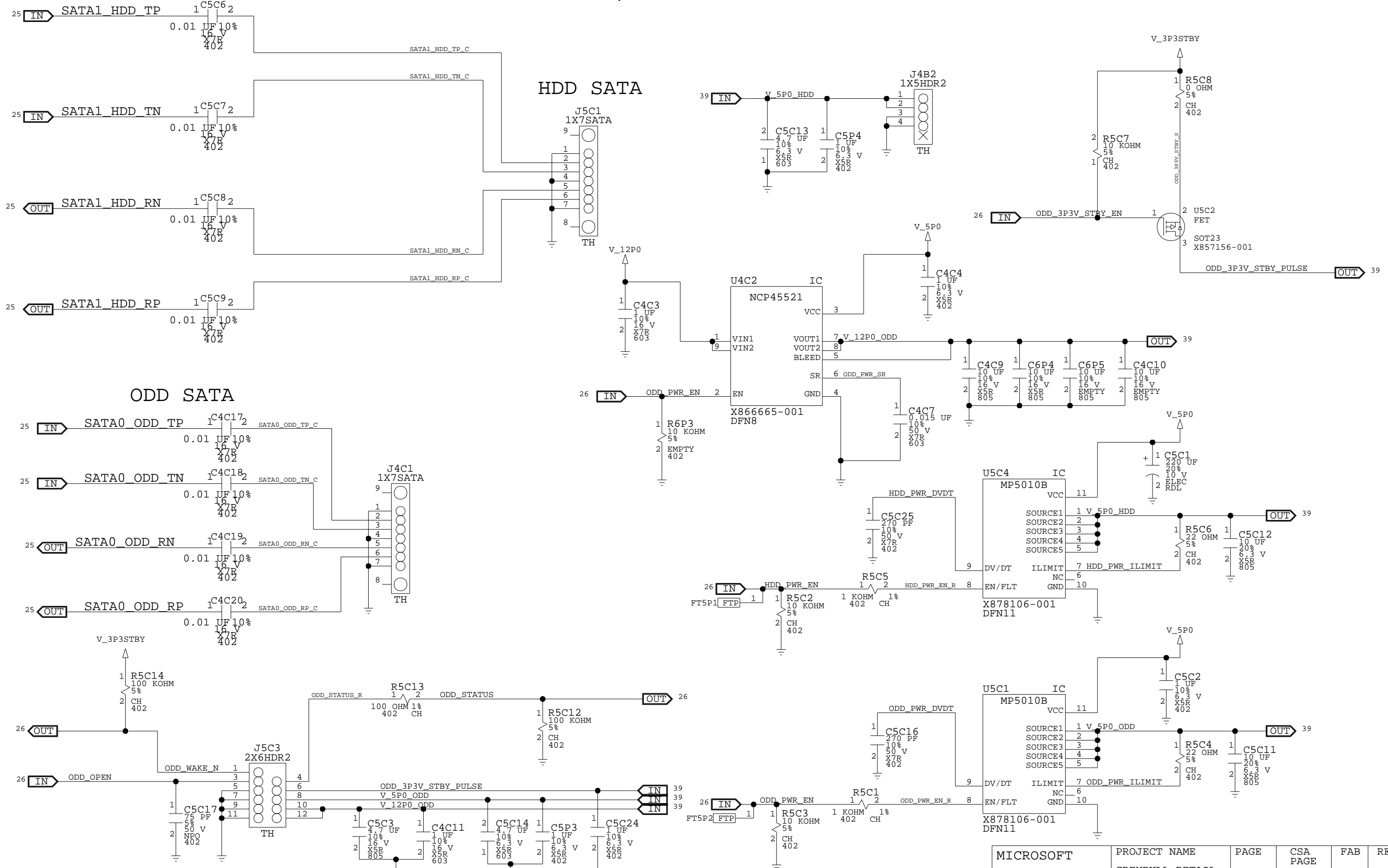


ESD DIODE ARRAYS ARE INCLUDED FOR EVALUATION. TO BE CLEANED UP LATER.

AUX VS DDX STUFFING

MODE	R9B8/R9B9	R9A5/R9A6	R9A3/R9A4
AUX	0.1 UF CAP	STUFF	EMPTY
DDC	0 OHM RES	EMPTY	STUFF

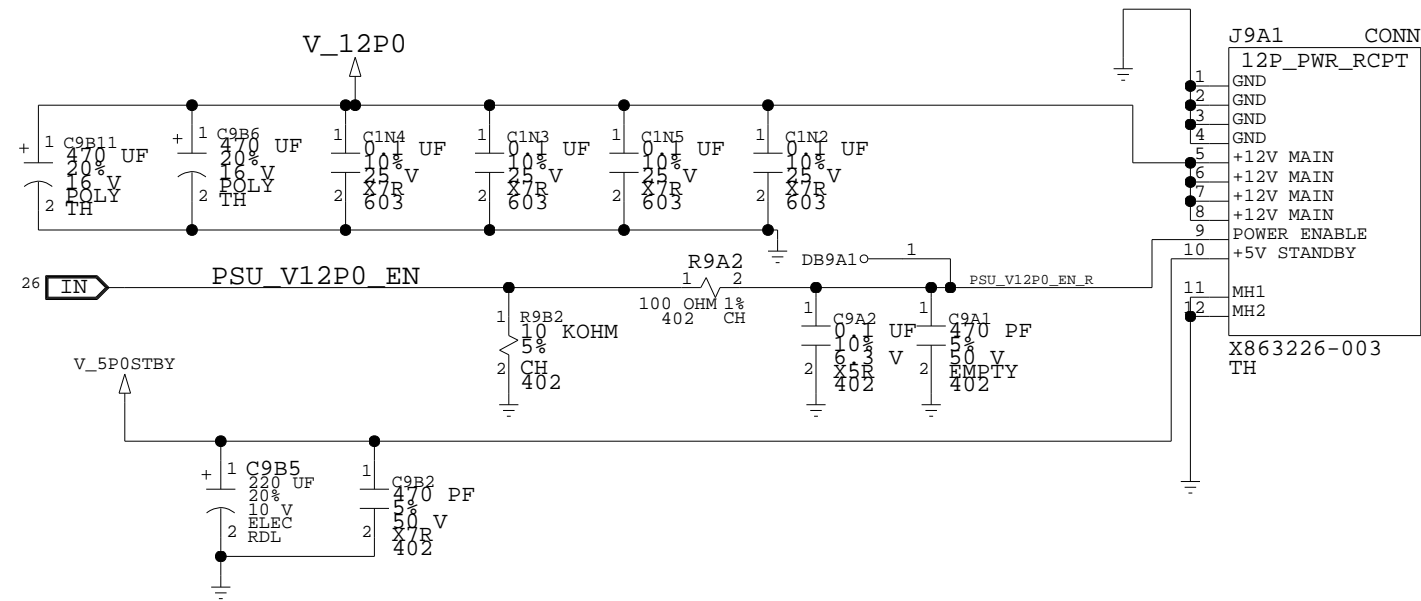
# CONN, ODD + HDD







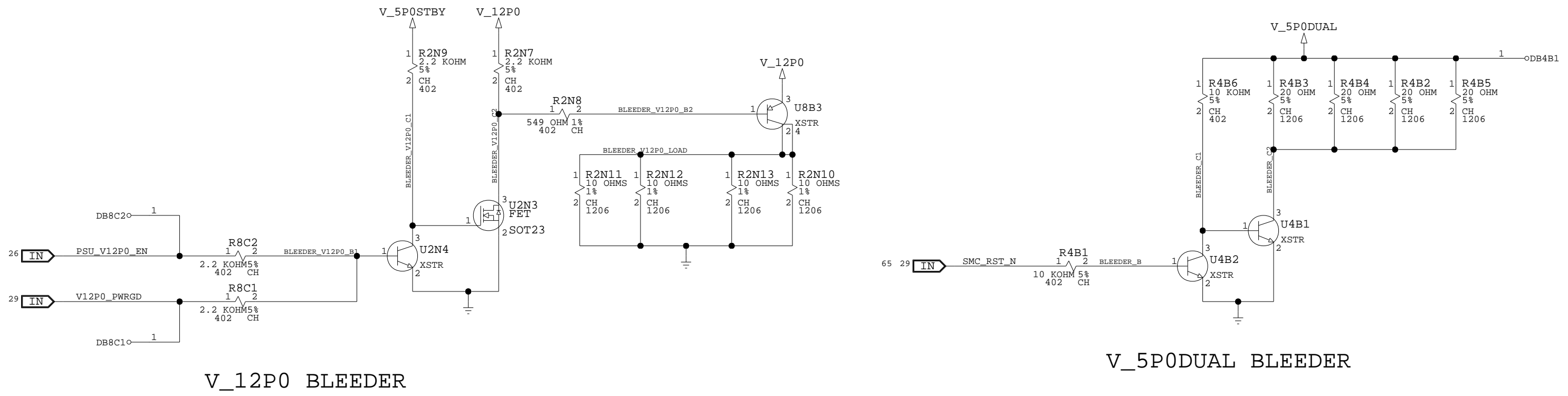
# CONN, PWR



DRAWING  
Tue Jun 18 16:42:28

MICROSOFT	PROJECT NAME	PAGE	CSA	FAB	REV
CONFIDENTIAL	GREYBULL_RETAIL	41/72	41/72	M	1.0

# VREGS, BLEEDERS

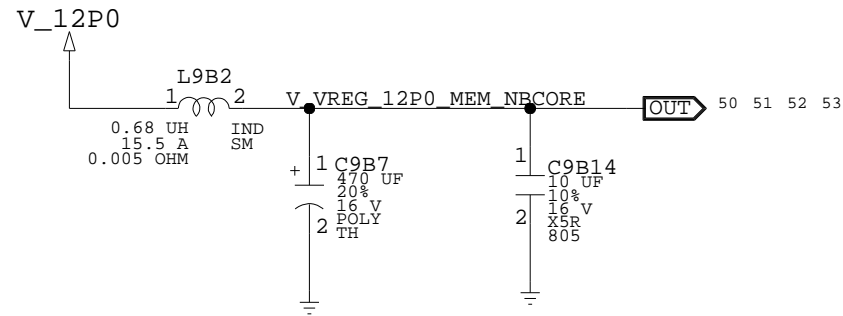


V\_12P0 BLEEDER

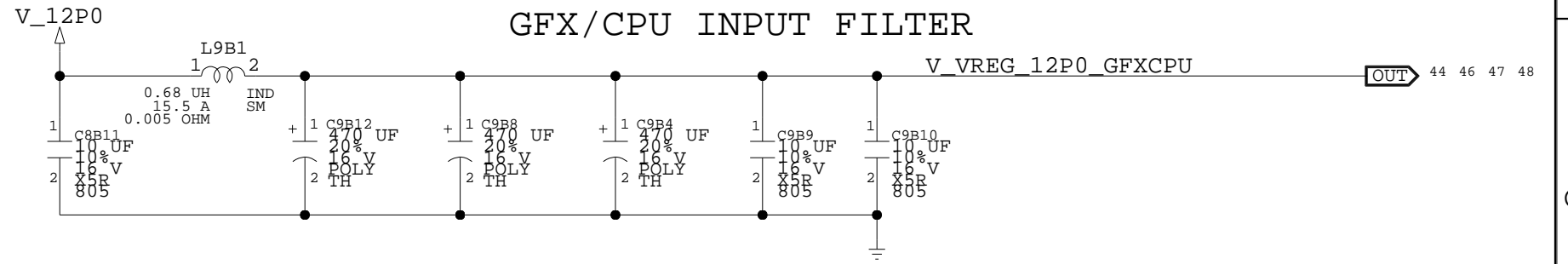
V\_5P0DUAL BLEEDER

# VREGS, INPUT + OUTPUT FILTERS

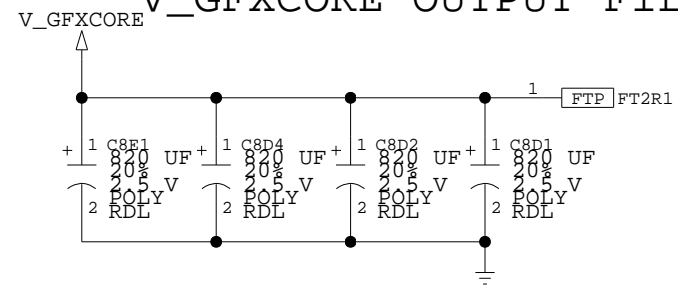
## IO/NBCORE/MEMCORE INPUT FILTER



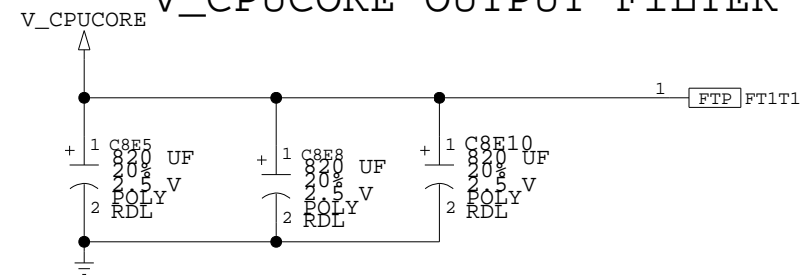
## GFX/CPU INPUT FILTER



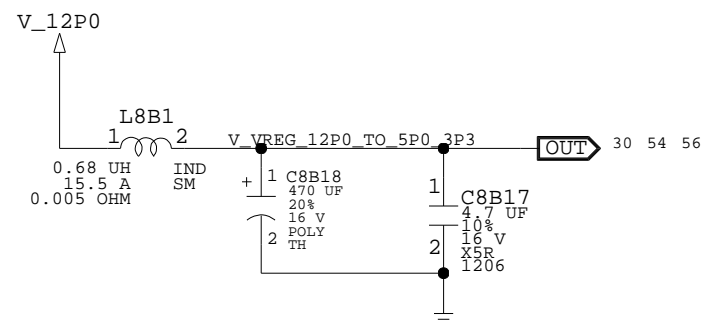
## V\_GFXCORE OUTPUT FILTER



## V\_CPUCORE OUTPUT FILTER

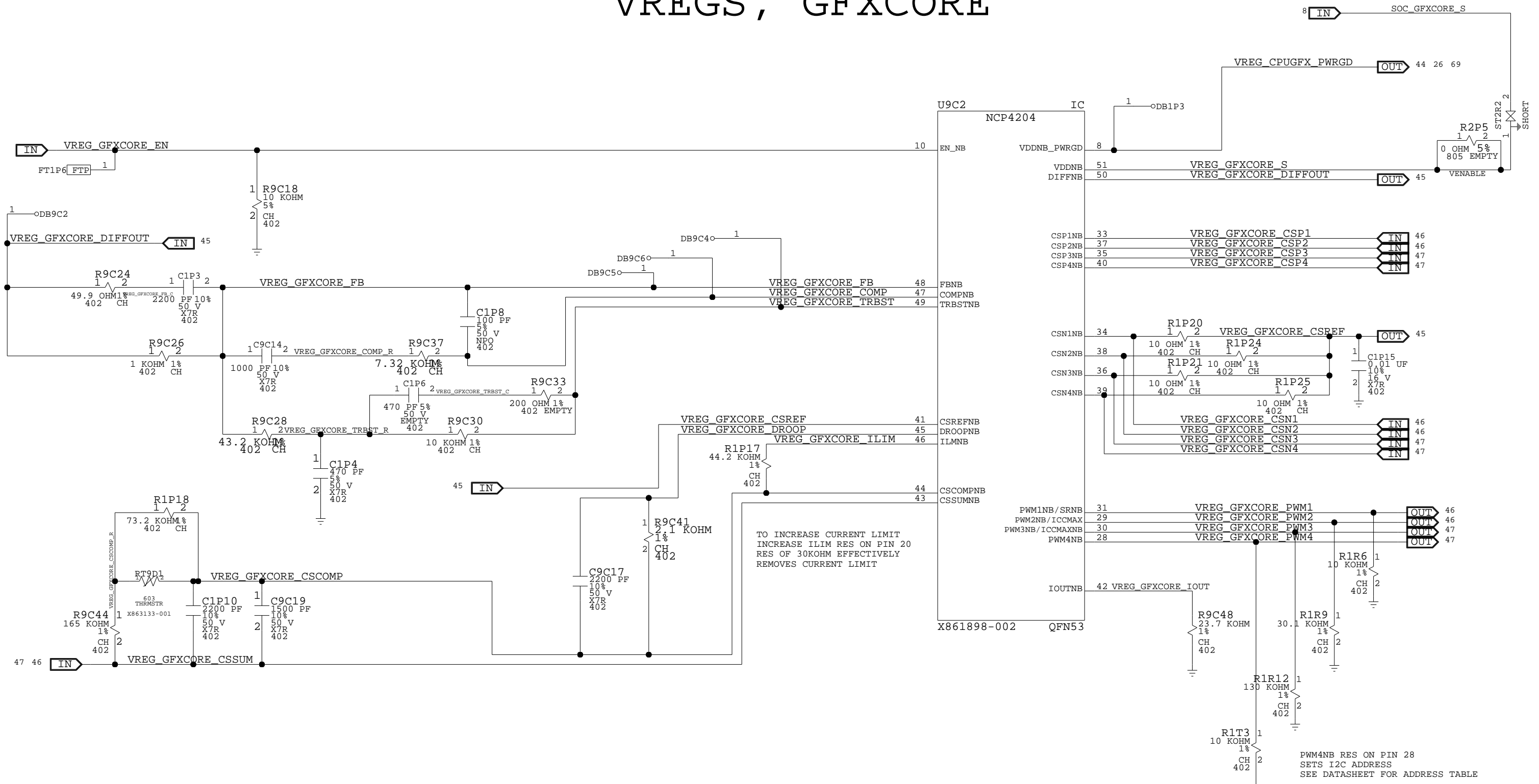


## 5P0/3P3 INPUT FILTER





# VREGS, GFXCORE



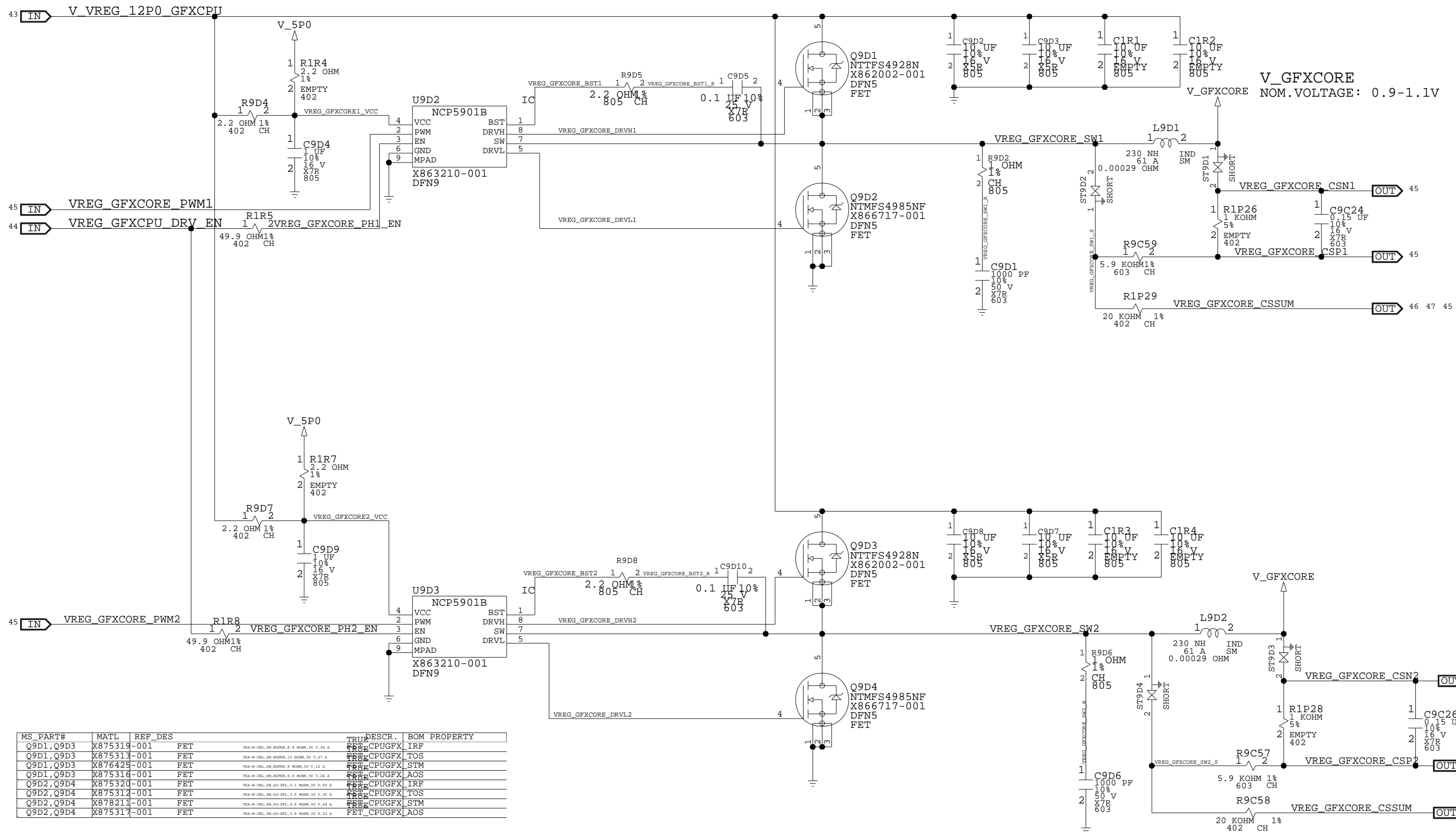
TO INCREASE CURRENT LIMIT  
INCREASE ILIM RES ON PIN 20  
RES OF 30KOHM EFFECTIVELY  
REMOVES CURRENT LIMIT

PWM4NB RES ON PIN 28  
SETS I2C ADDRESS  
SEE DATASHEET FOR ADDRESS TABLE

SLEW RATE SET BY SRNB RES ON PIN 31

SLEW RATE	RESISTANCE
10MV/US	10 KOHM
20MV/US	25 KOHM
30MV/US	45 KOHM

# VREGS , GFXCORE OUTPUT PHASE 1 & 2

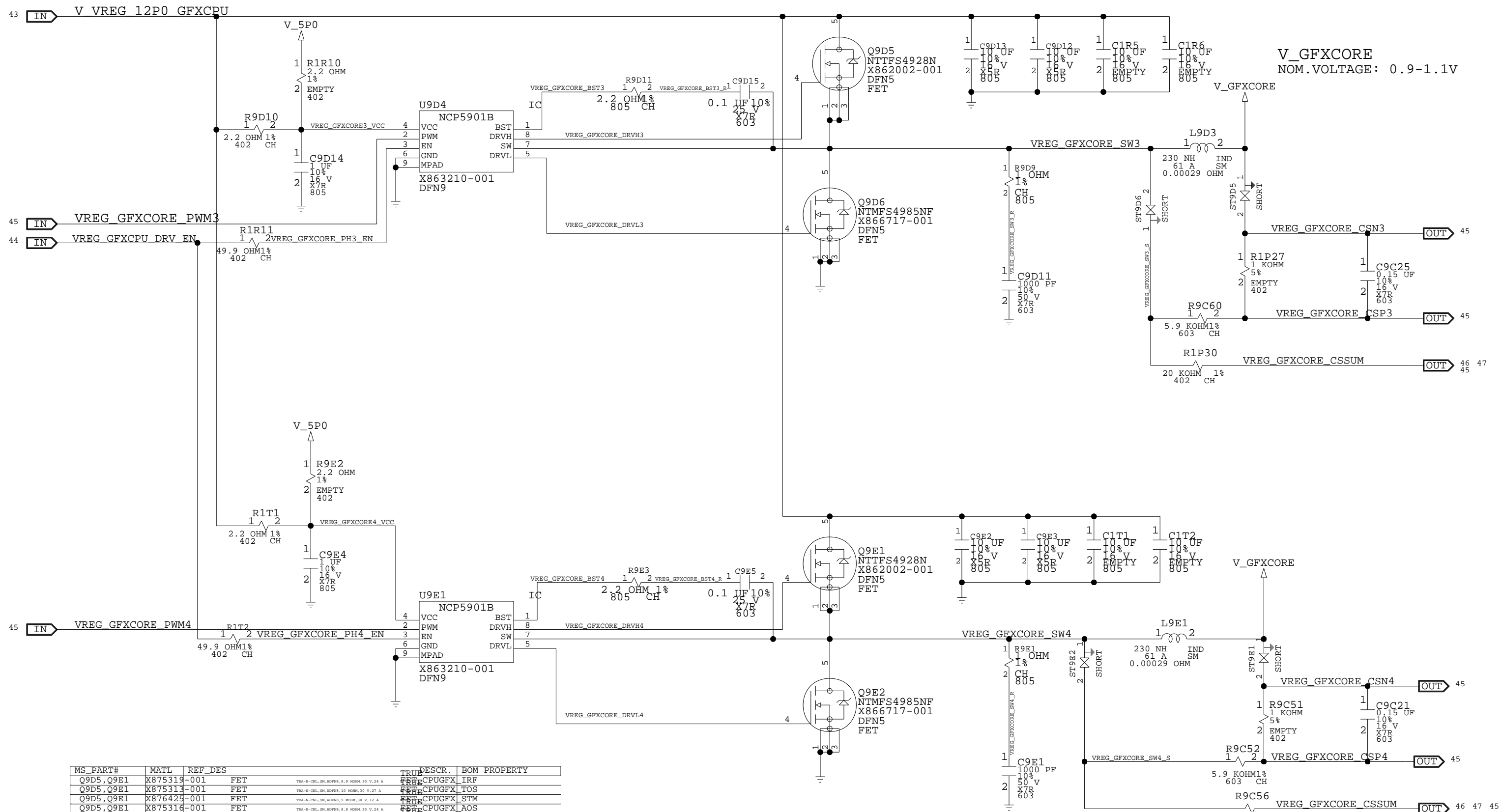


MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
Q9D1, Q9D3	X875319	-001	FET	TRA-N-CHL-SM, MOPNR, 8.9 MOHM, 30 V, 24 A
Q9D1, Q9D3	X875313	-001	FET	TRA-N-CHL-SM, MOPNR, 10 MOHM, 30 V, 27 A
Q9D1, Q9D3	X876425	-001	FET	TRA-N-CHL-SM, MOPNR, 9 MOHM, 30 V, 12 A
Q9D1, Q9D3	X875316	-001	FET	TRA-N-CHL-SM, MOPNR, 8.8 MOHM, 30 V, 24 A
Q9D2, Q9D4	X875320	-001	FET	TRA-N-CHL-SM, SO-EPL, 3.1 MOHM, 30 V, 50 A
Q9D2, Q9D4	X875312	-001	FET	TRA-N-CHL-SM, SO-EPL, 3.5 MOHM, 30 V, 35 A
Q9D2, Q9D4	X878211	-001	FET	TRA-N-CHL-SM, SO-EPL, 4.5 MOHM, 30 V, 24 A
Q9D2, Q9D4	X875317	-001	FET	TRA-N-CHL-SM, SO-EPL, 3.6 MOHM, 30 V, 32 A

DRAWING  
Tue Jun 18 16:42:25

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 46/72	CSA PAGE 46/72	FAB M	REV 1.0
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# VREGS, GFXCORE OUTPUT PHASE 3 & 4

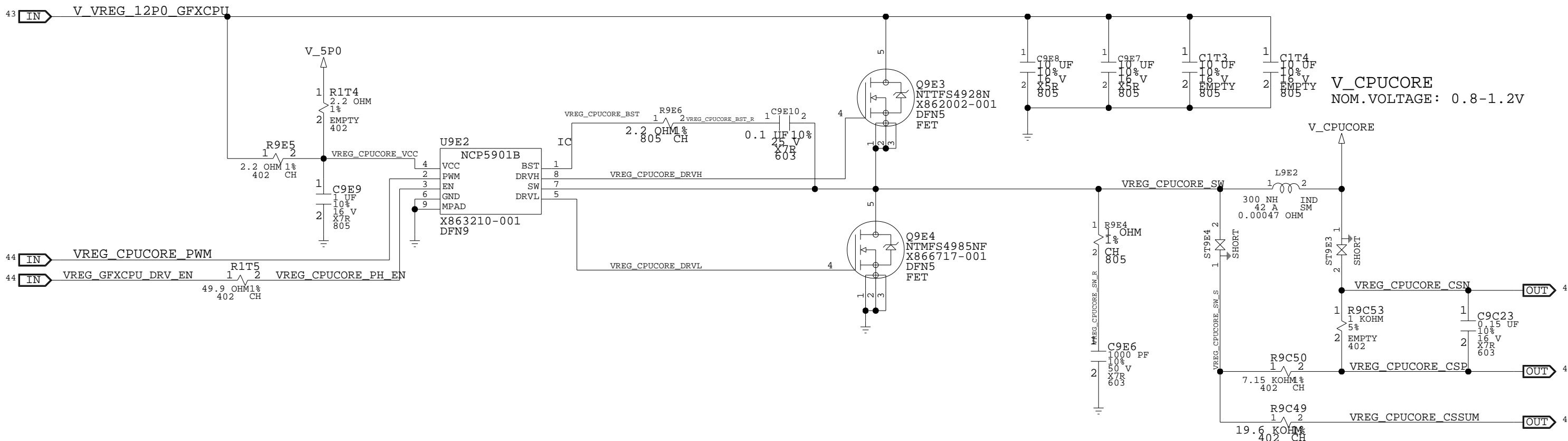


MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
Q9D5, Q9E1	X875319-001	FET	FET_CPUGFX_IRF	
Q9D5, Q9E1	X875313-001	FET	FET_CPUGFX_TOS	
Q9D5, Q9E1	X876425-001	FET	FET_CPUGFX_STM	
Q9D5, Q9E1	X875316-001	FET	FET_CPUGFX_AOS	
Q9D6, Q9E2	X875320-001	FET	FET_CPUGFX_IRF	
Q9D6, Q9E2	X875312-001	FET	FET_CPUGFX_TOS	
Q9D6, Q9E2	X878211-001	FET	FET_CPUGFX_STM	
Q9D6, Q9E2	X875317-001	FET	FET_CPUGFX_AOS	

DRAWING  
Tue Jun 18 16:42:25

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 47/72	CSA PAGE 47/72	FAB M	REV 1.0
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# VREGS, CPUCORE OUTPUT PHASE

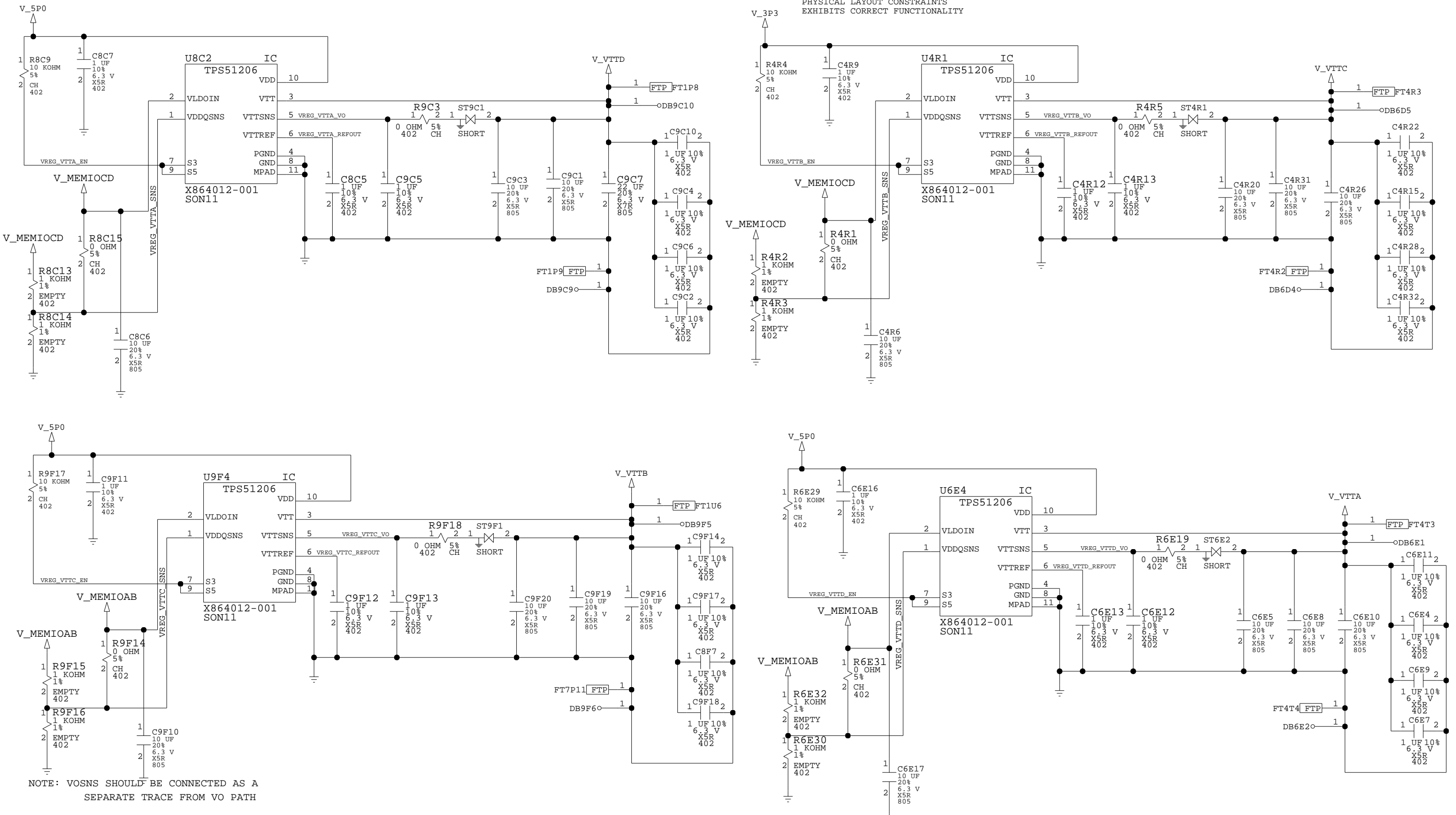


MS_PART#	MATL	REF_DES	TRU	DESCR.	BOM PROPERTY
Q9E3	X875319-001	FET	TRUE	FET_CPUGFX	IRF
Q9E3	X875313-001	FET	TRUE	FET_CPUGFX	TOS
Q9E3	X876425-001	FET	TRUE	FET_CPUGFX	STM
Q9E3	X875316-001	FET	TRUE	FET_CPUGFX	AOS
Q9E4	X875320-001	FET	TRUE	FET_CPUGFX	IRF
Q9E4	X875312-001	FET	TRUE	FET_CPUGFX	TOS
Q9E4	X878211-001	FET	TRUE	FET_CPUGFX	STM
Q9E4	X875317-001	FET	TRUE	FET_CPUGFX	AOS



# VREGS, VTT TERMINATION

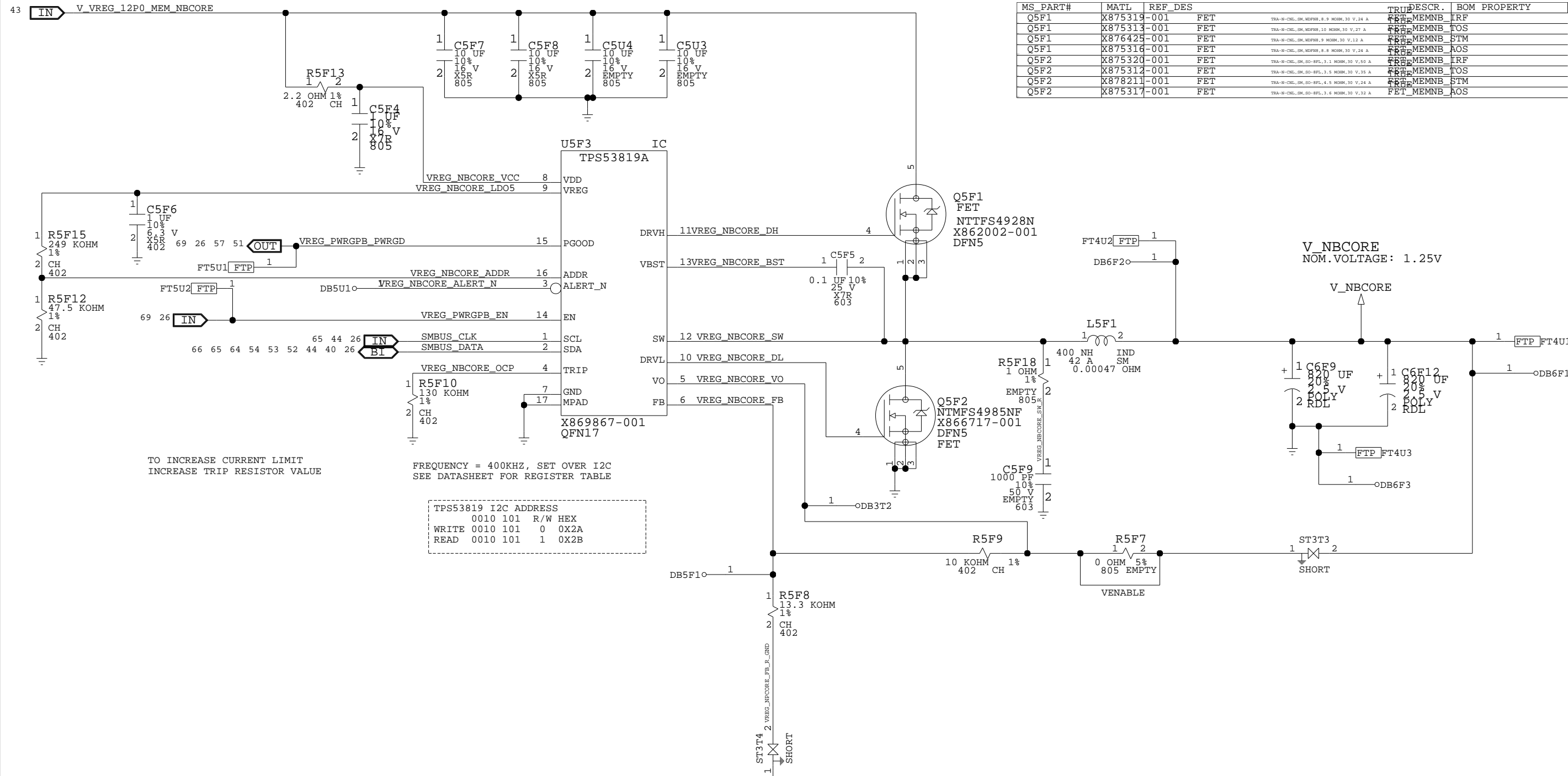
POWERED BY V3P3 DUE TO PHYSICAL LAYOUT CONSTRAINTS EXHIBITS CORRECT FUNCTIONALITY



NOTE: VOSNS SHOULD BE CONNECTED AS A SEPARATE TRACE FROM VO PATH

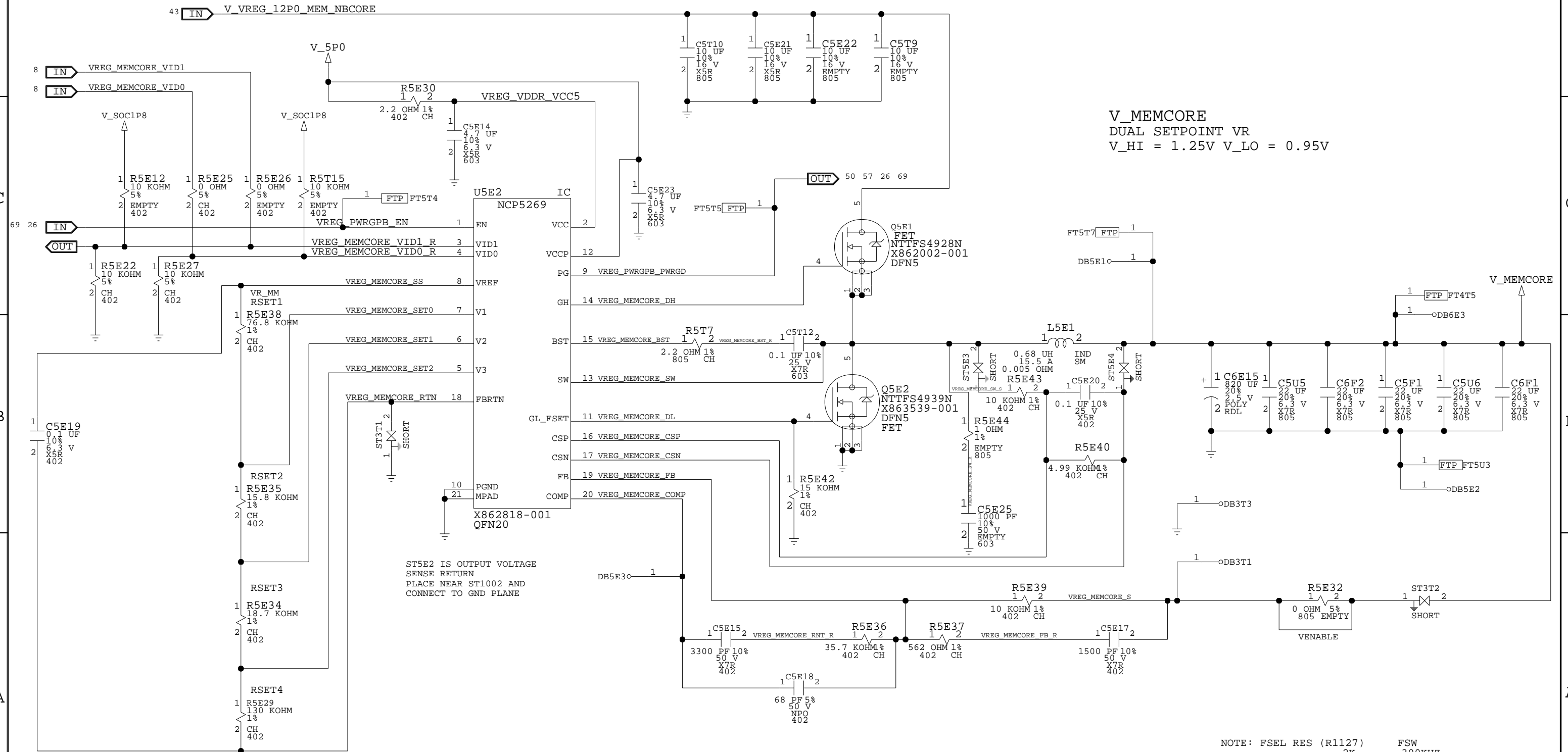
MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 49/72	CSA PAGE 49/72	FAB M	REV 1.0
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# VREGS, NBCORE



MS_PART#	MATL	REF_DES	TRUP	DESCR.	BOM PROPERTY
Q5F1	X875319-001	FET	TRA-8-CHE, SM, NDFPB, 8.9 MOHM, 30 V, 24 A	FET_MEMNB_IRF	
Q5F1	X875313-001	FET	TRA-8-CHE, SM, NDFPB, 10 MOHM, 30 V, 27 A	FET_MEMNB_TOS	
Q5F1	X876425-001	FET	TRA-8-CHE, SM, NDFPB, 9 MOHM, 30 V, 12 A	FET_MEMNB_STM	
Q5F1	X875316-001	FET	TRA-8-CHE, SM, NDFPB, 8.8 MOHM, 30 V, 24 A	FET_MEMNB_AOS	
Q5F2	X875320-001	FET	TRA-8-CHE, SM, SD-RFL, 3.1 MOHM, 30 V, 50 A	FET_MEMNB_IRF	
Q5F2	X875312-001	FET	TRA-8-CHE, SM, SD-RFL, 3.5 MOHM, 30 V, 35 A	FET_MEMNB_TOS	
Q5F2	X878211-001	FET	TRA-8-CHE, SM, SD-RFL, 4.5 MOHM, 30 V, 24 A	FET_MEMNB_STM	
Q5F2	X875317-001	FET	TRA-8-CHE, SM, SD-RFL, 3.6 MOHM, 30 V, 32 A	FET_MEMNB_AOS	

# VREGS , MEMCORE



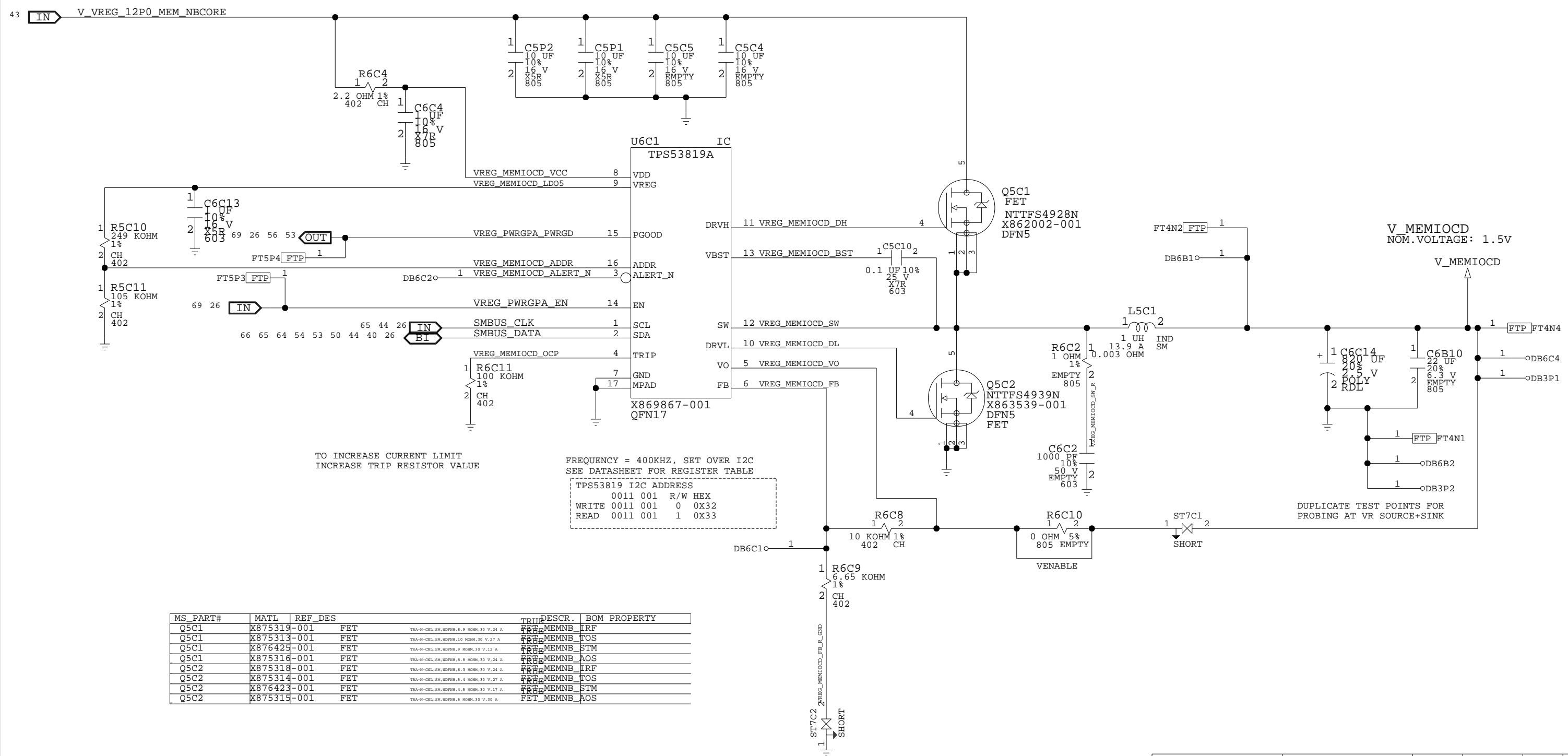
V\_MEMCORE  
 DUAL SETPOINT VR  
 V\_HI = 1.25V V\_LO = 0.95V

ST5E2 IS OUTPUT VOLTAGE  
 SENSE RETURN  
 PLACE NEAR ST1002 AND  
 CONNECT TO GND PLANE

NOTE: FSEL RES (R1127) 2K 300KHZ  
 6K 400KHZ  
 15K 600KHZ

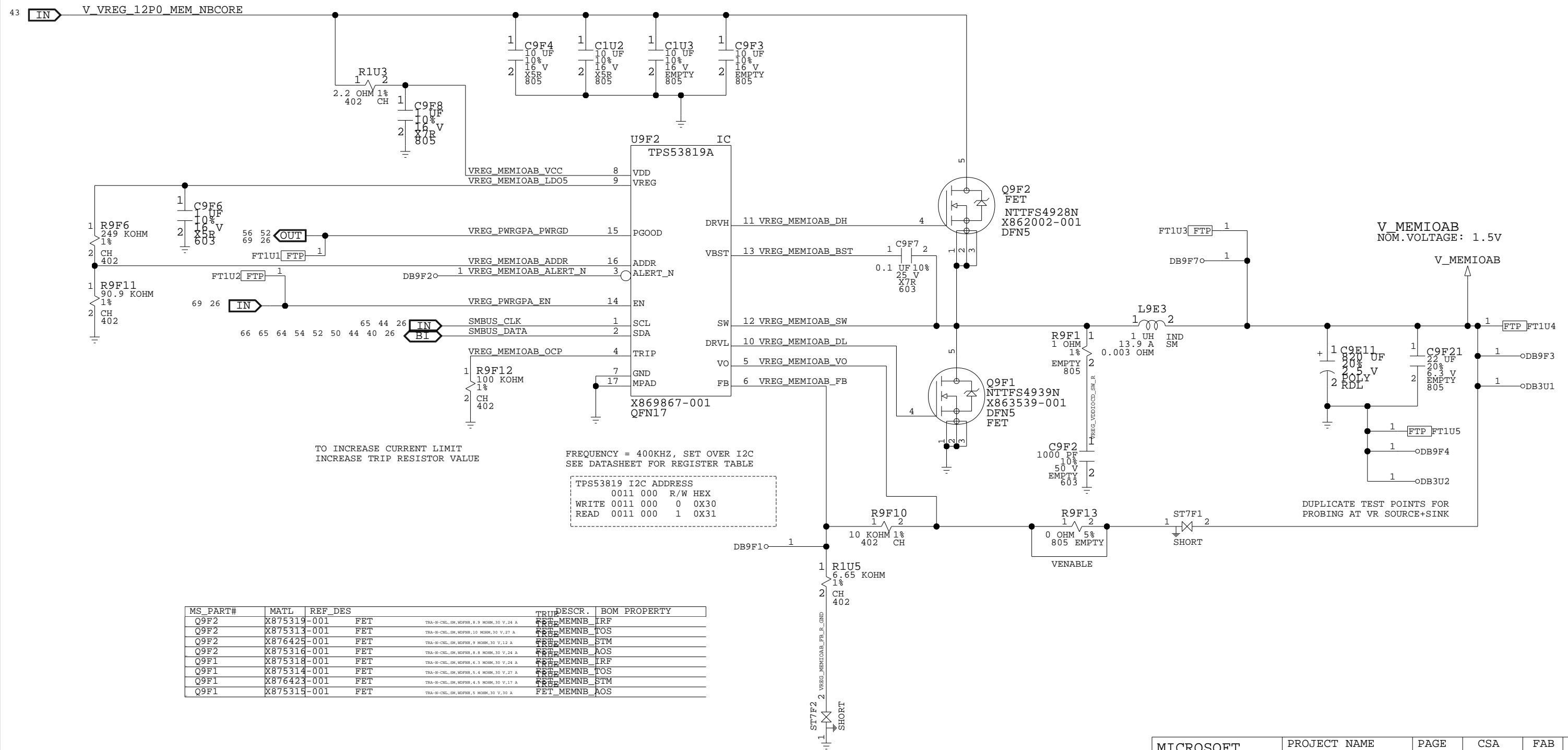
MS PART#	MATL	REF	DESC	TRIP	DESCR.	BOM PROPERTY
Q5E1	X875319	001	FET	TRIP	MEMNB	IRF
Q5E1	X875313	001	FET	TRIP	MEMNB	TOS
Q5E1	X876425	001	FET	TRIP	MEMNB	STM
Q5E1	X875316	001	FET	TRIP	MEMNB	AOS
Q5E2	X875318	001	FET	TRIP	MEMNB	IRF
Q5E2	X875314	001	FET	TRIP	MEMNB	TOS
Q5E2	X876423	001	FET	TRIP	MEMNB	STM
Q5E2	X875315	001	FET	TRIP	MEMNB	AOS

# VREG, MEMIOCD



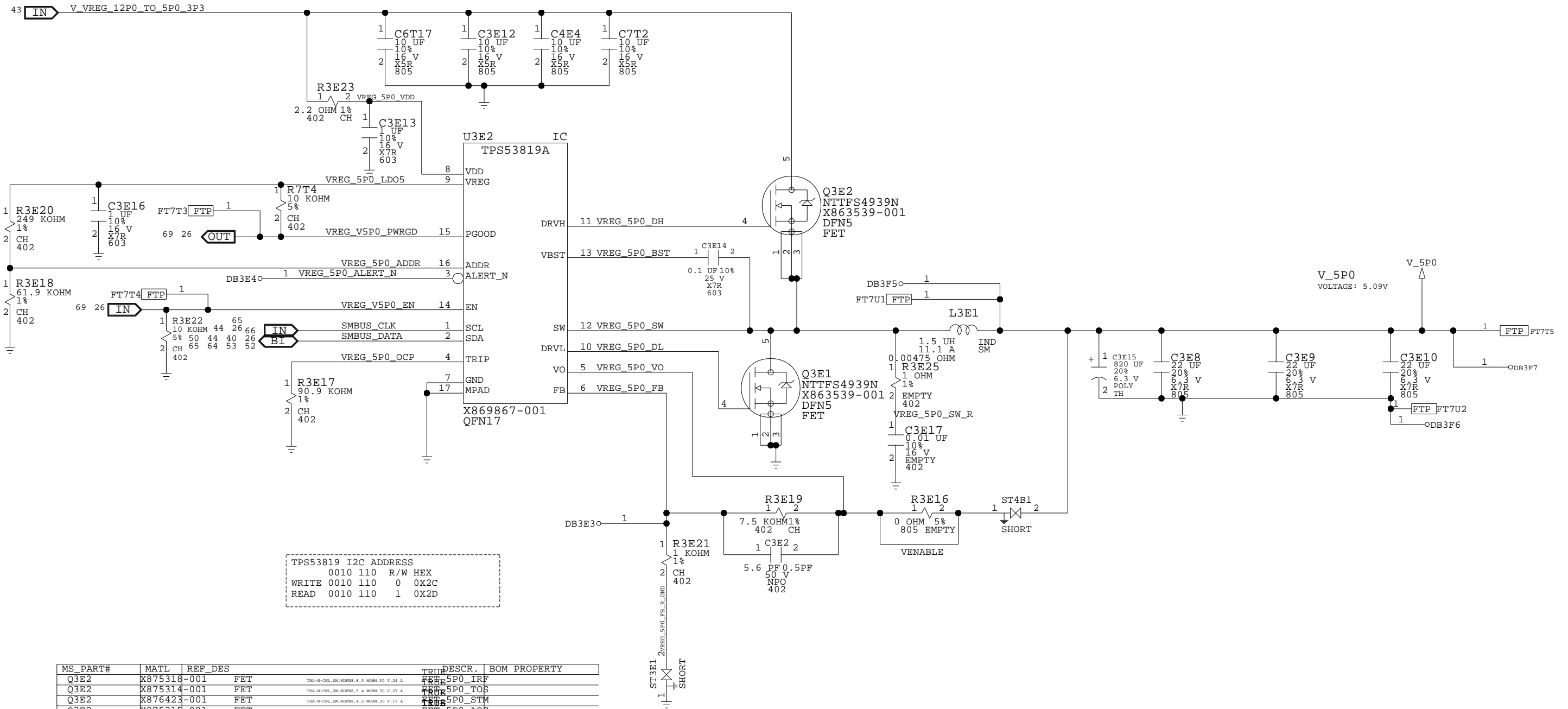
MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
Q5C1	X875319-001	FET	IRF	MEMNB	IRF
Q5C1	X875313-001	FET	FOS	MEMNB	FOS
Q5C1	X876425-001	FET	STM	MEMNB	STM
Q5C1	X875316-001	FET	AOS	MEMNB	AOS
Q5C2	X875318-001	FET	IRF	MEMNB	IRF
Q5C2	X875314-001	FET	FOS	MEMNB	FOS
Q5C2	X876423-001	FET	STM	MEMNB	STM
Q5C2	X875315-001	FET	AOS	MEMNB	AOS

# VREG, MEMIOAB



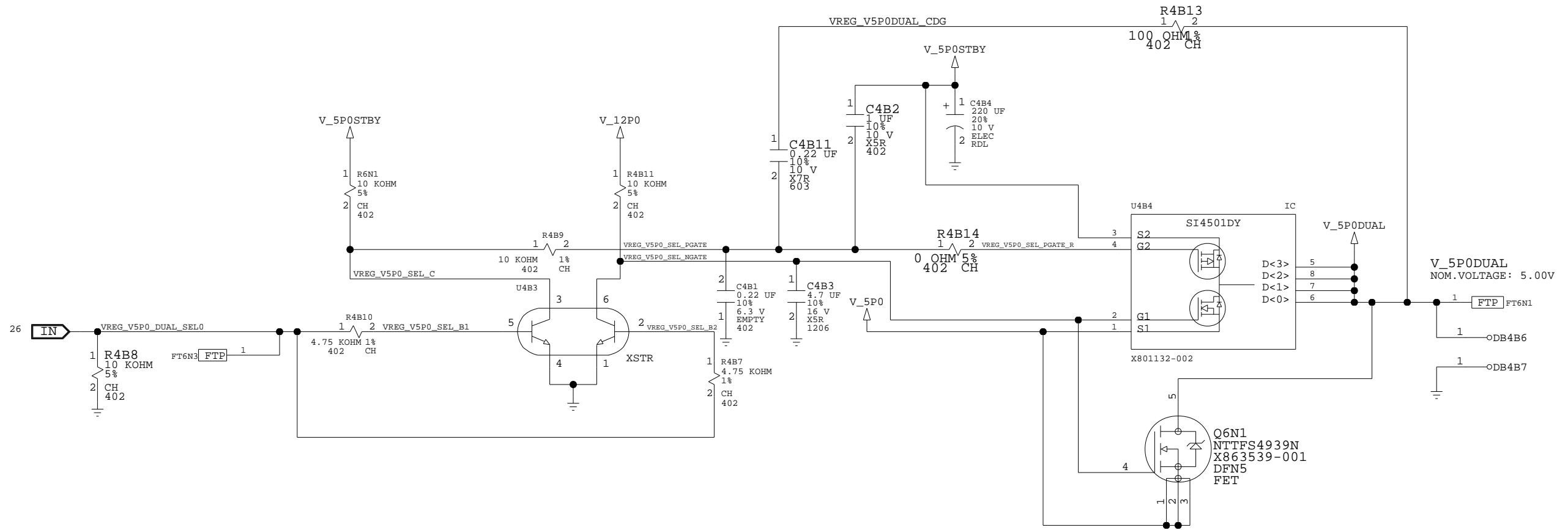
MS_PART#	MATL	REF_DES	TRU	DESCR.	BOM PROPERTY
Q9F2	X875319-001	FET	TRA-N-CNL, SM, NDFPS, 8.9	MEMNB, 30 V, 24 A	IRF
Q9F2	X875313-001	FET	TRA-N-CNL, SM, NDFPS, 10	MEMNB, 30 V, 27 A	TOS
Q9F2	X876425-001	FET	TRA-N-CNL, SM, NDFPS, 9	MEMNB, 30 V, 12 A	STM
Q9F2	X875316-001	FET	TRA-N-CNL, SM, NDFPS, 8.8	MEMNB, 30 V, 24 A	AOS
Q9F1	X875318-001	FET	TRA-N-CNL, SM, NDFPS, 6.3	MEMNB, 30 V, 24 A	IRF
Q9F1	X875314-001	FET	TRA-N-CNL, SM, NDFPS, 5.4	MEMNB, 30 V, 27 A	TOS
Q9F1	X876423-001	FET	TRA-N-CNL, SM, NDFPS, 4.5	MEMNB, 30 V, 17 A	STM
Q9F1	X875315-001	FET	TRA-N-CNL, SM, NDFPS, 5	MEMNB, 30 V, 30 A	AOS

# VREGS, V5P0



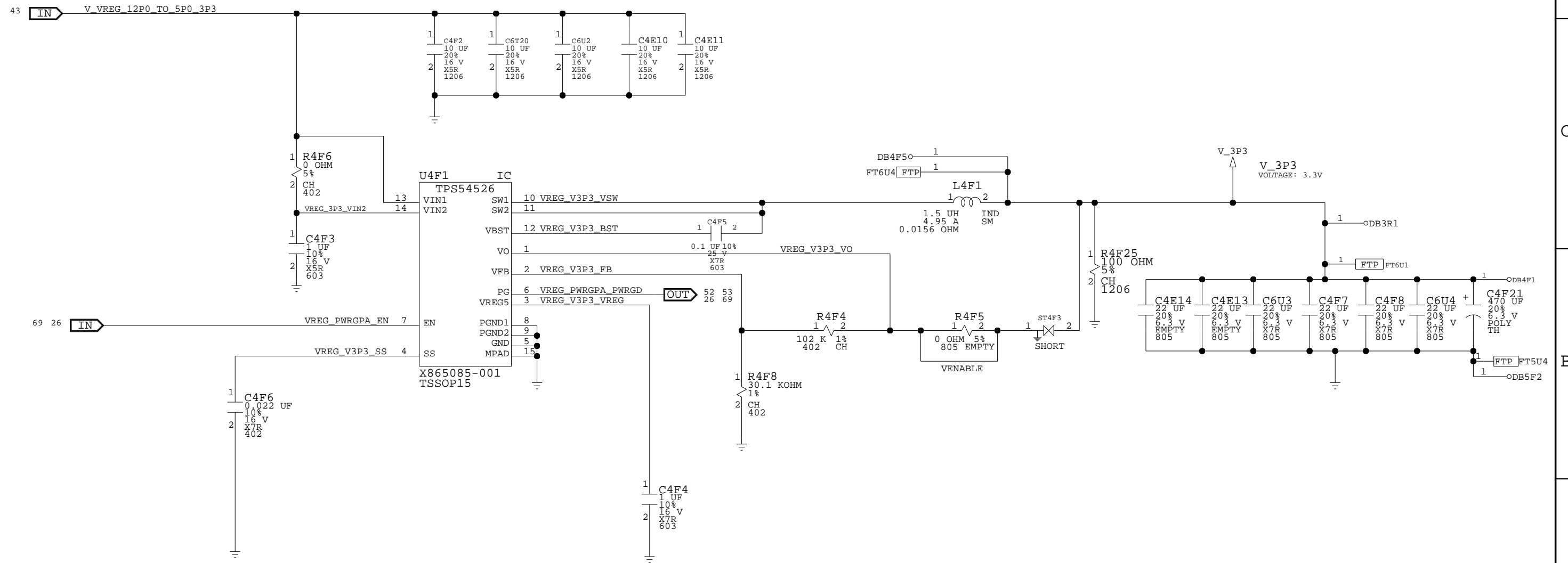
MS_PART#	MATL	REF_DES	TRIP	DESCR.	BOM PROPERTY
Q3E2	X875318-001	FET	TRIP	FET_5P0_IRF	
Q3E2	X875314-001	FET	TRIP	FET_5P0_TOS	
Q3E2	X876423-001	FET	TRIP	FET_5P0_STM	
Q3E2	X875315-001	FET	TRIP	FET_5P0_AOS	
Q3E1	X875318-001	FET	TRIP	FET_5P0_IRF	
Q3E1	X875314-001	FET	TRIP	FET_5P0_TOS	
Q3E1	X876423-001	FET	TRIP	FET_5P0_STM	
Q3E1	X875315-001	FET	TRIP	FET_5P0_AOS	

# VREGS, V5P0 DUAL



VREG_V5P0_DUAL_SEL0	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5POSTBY
LOW	HIGH	V_5P0

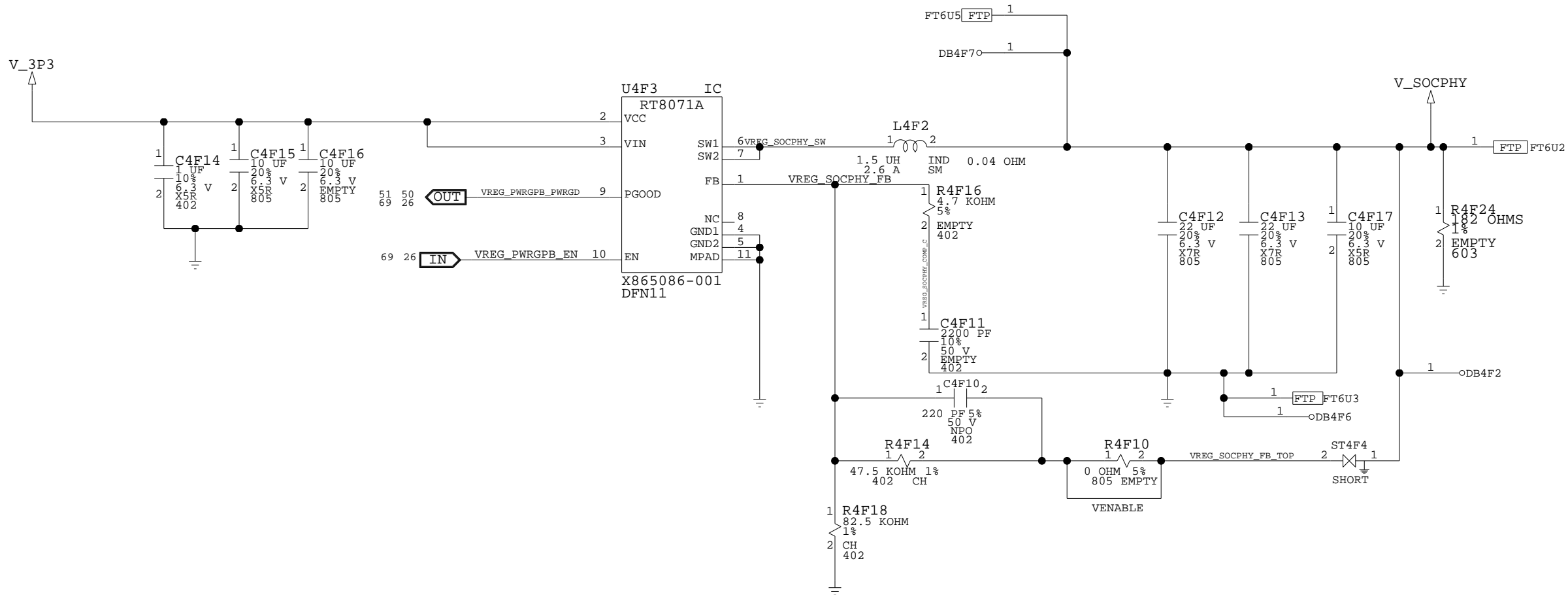
# VREGS, V3P3



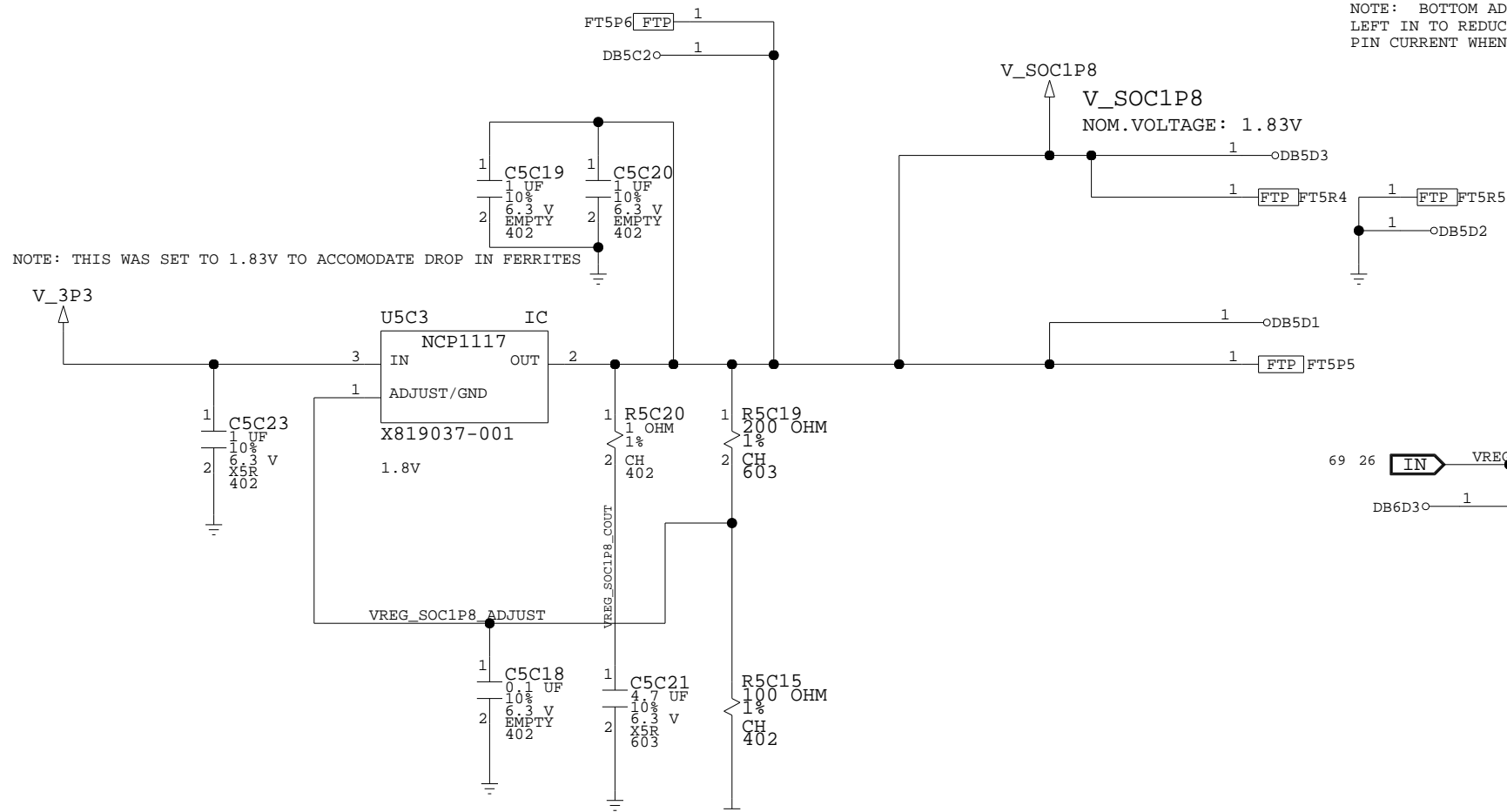
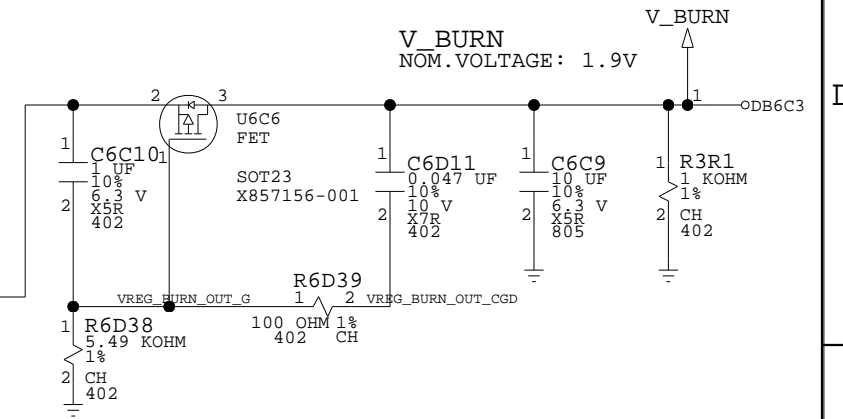
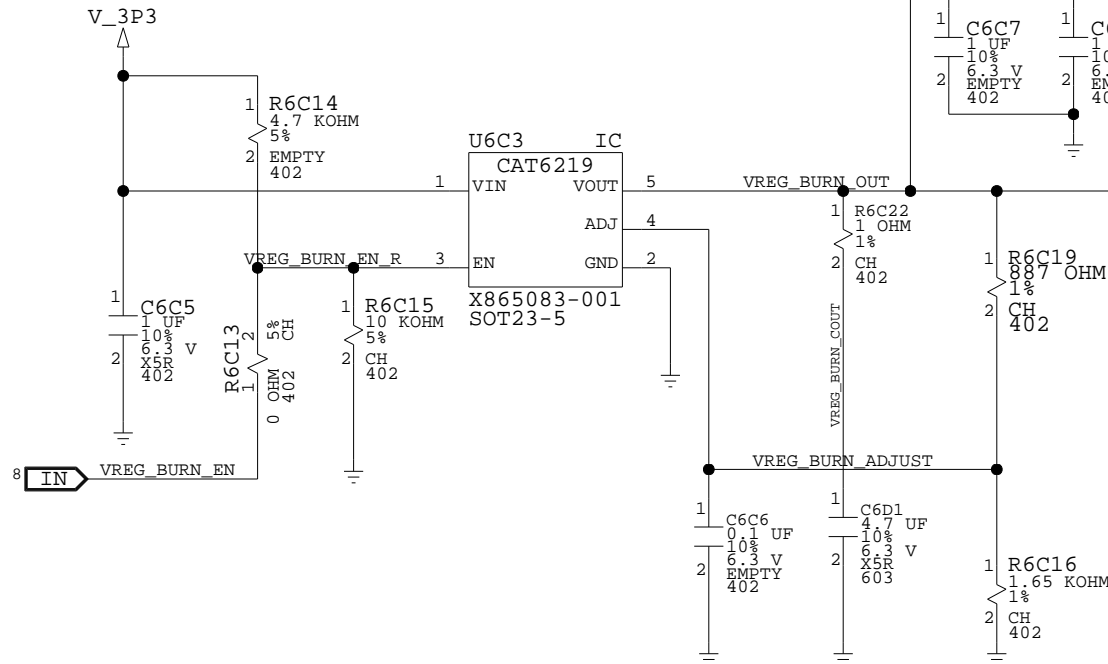
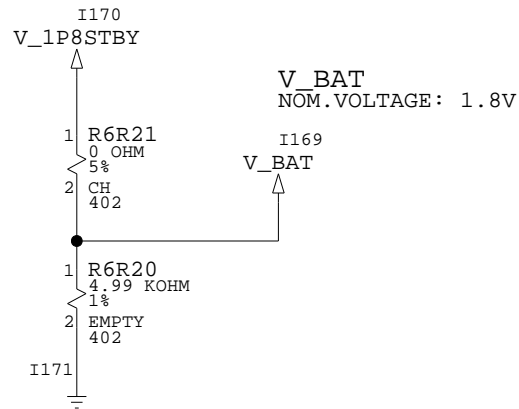


# VREGS, VSOCPHY

V\_SOCPHY  
NOM.VOLTAGE: 0.95V



# VREGS, VSOCPLL + VBURN + VFUSE + VBAT

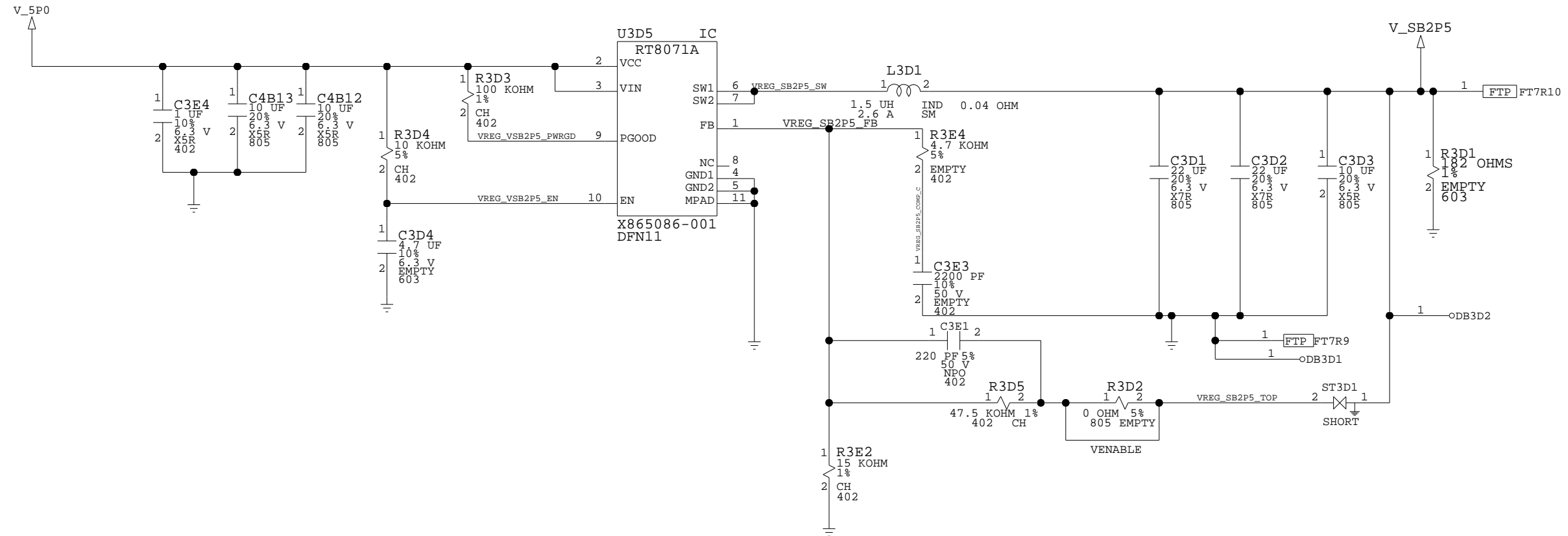


NOTE: BOTTOM ADJUST RESISTOR LEFT IN TO REDUCE EFFECT OF ADJUST PIN CURRENT WHEN USED WITH 1K DIGIPOT

NOTE: BOTTOM ADJUST RESISTOR LEFT IN TO REDUCE EFFECT OF ADJUST PIN CURRENT WHEN USED WITH 1K DIGIPOT

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 58/72	CSA PAGE 58/72	FAB M	REV 1.0
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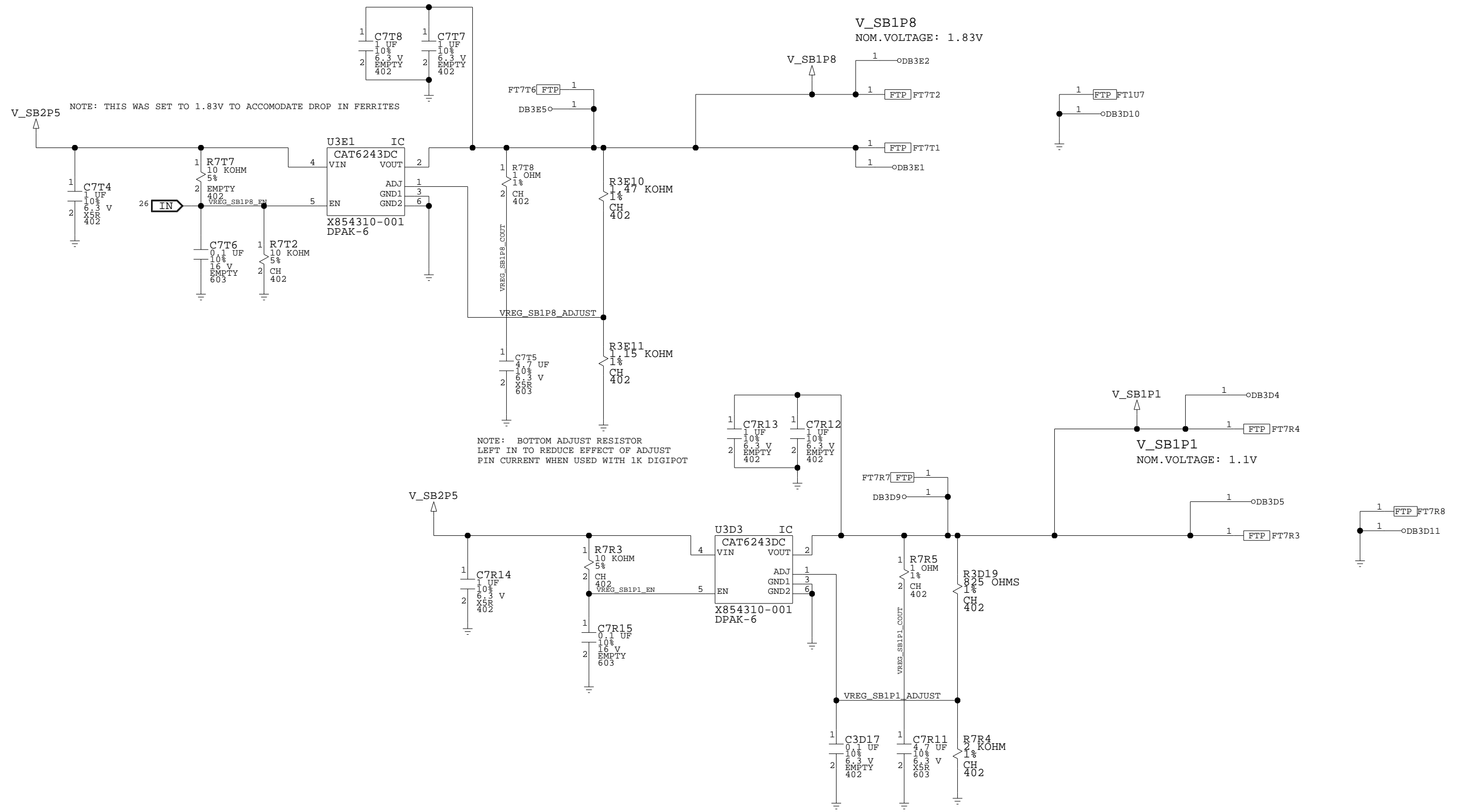
# VREGS, VSB2P5



V\_SB2P5  
NOM.VOLTAGE: 2.5V

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 59/72	CSA PAGE 59/72	FAB M	REV 1.0
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# VREGS, VSB1P8PLL + VSB1P8IO + VSBCORE + VSB1P1PLL

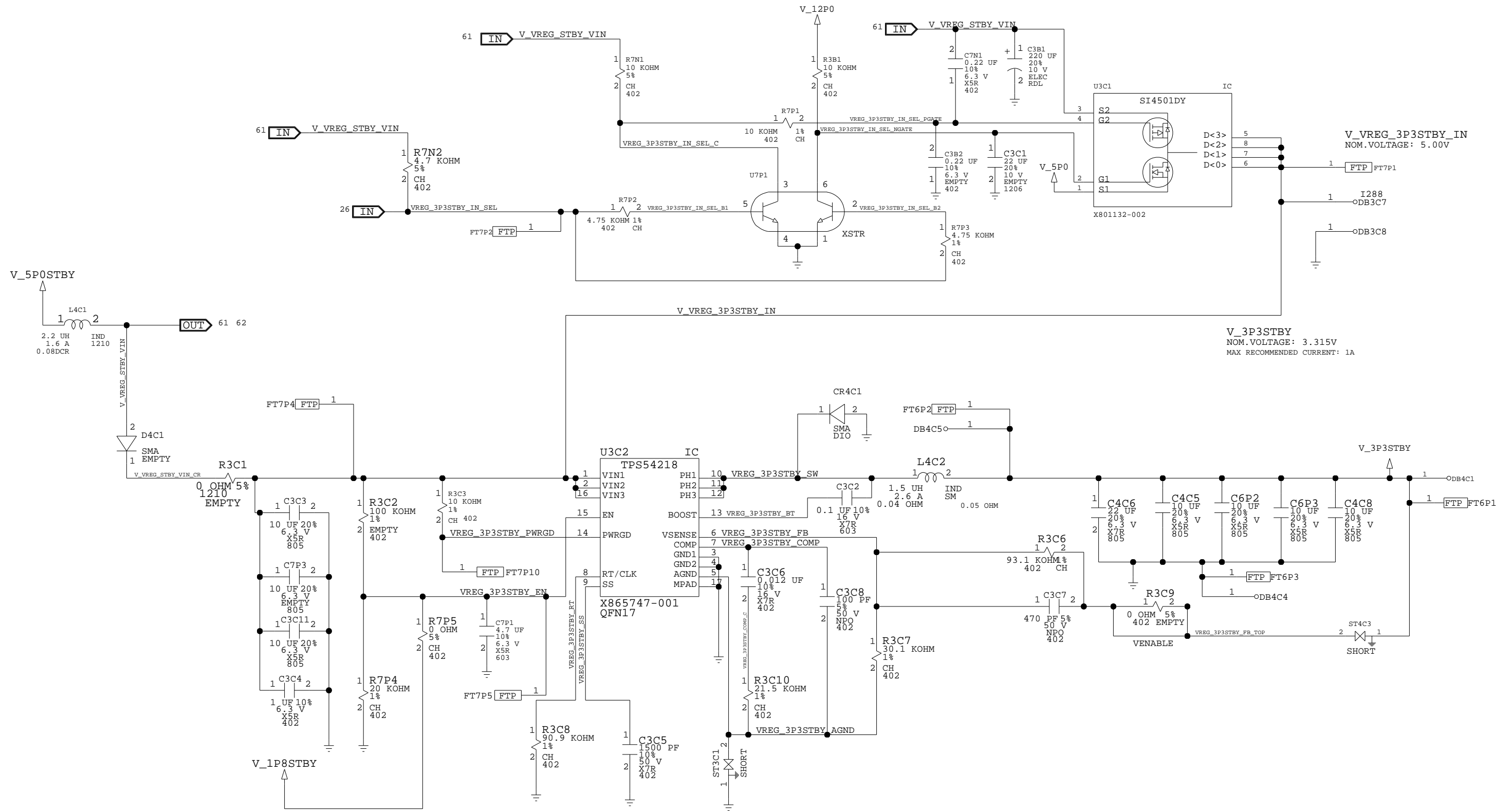


NOTE: BOTTOM ADJUST RESISTOR LEFT IN TO REDUCE EFFECT OF ADJUST PIN CURRENT WHEN USED WITH 1K DIGIPOT

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 60/72	CSA PAGE 60/72	FAB M	REV 1.0
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# VREGS, STANDBY SWITCHERS 3P3

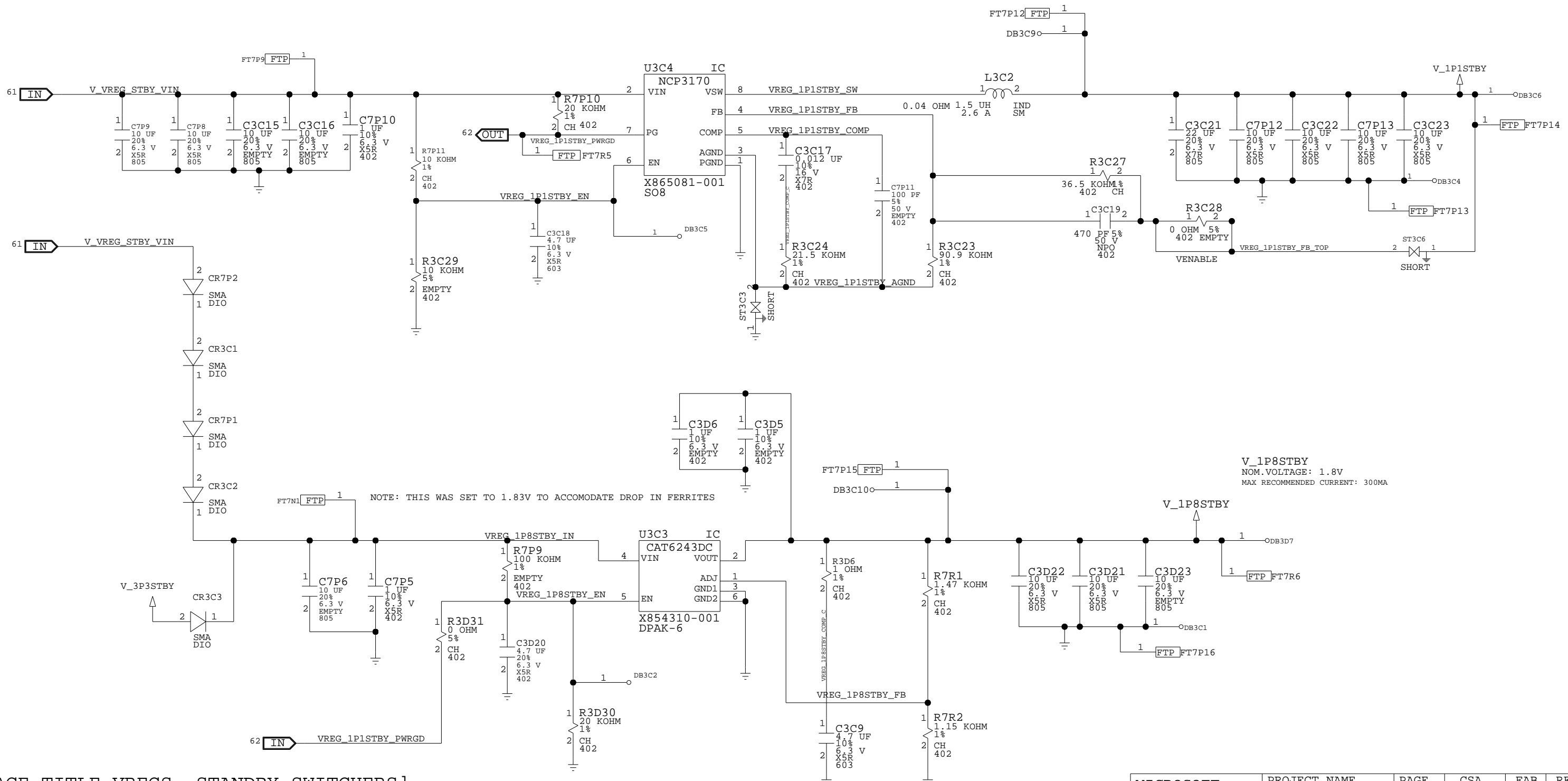
VREG_3P3STBY_IN_SEL	VREG_3P3STBY_IN_SEL NGATE/PGATE	VREG_3P3STBY_VCC
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0



# VREGS, STANDBY SWITCHERS 1P1 + 1P8

V\_1P1STBY  
 NOM.VOLTAGE: 1.13V  
 MAX RECOMMENDED CURRENT: 1.25A

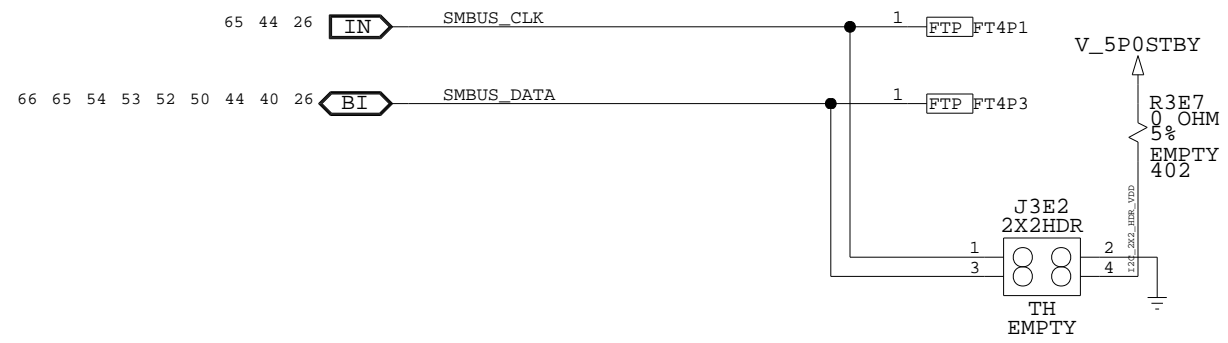
V\_1P8STBY  
 NOM.VOLTAGE: 1.8V  
 MAX RECOMMENDED CURRENT: 300MA



NOTE: THIS WAS SET TO 1.83V TO ACCOMMODATE DROP IN FERRITES

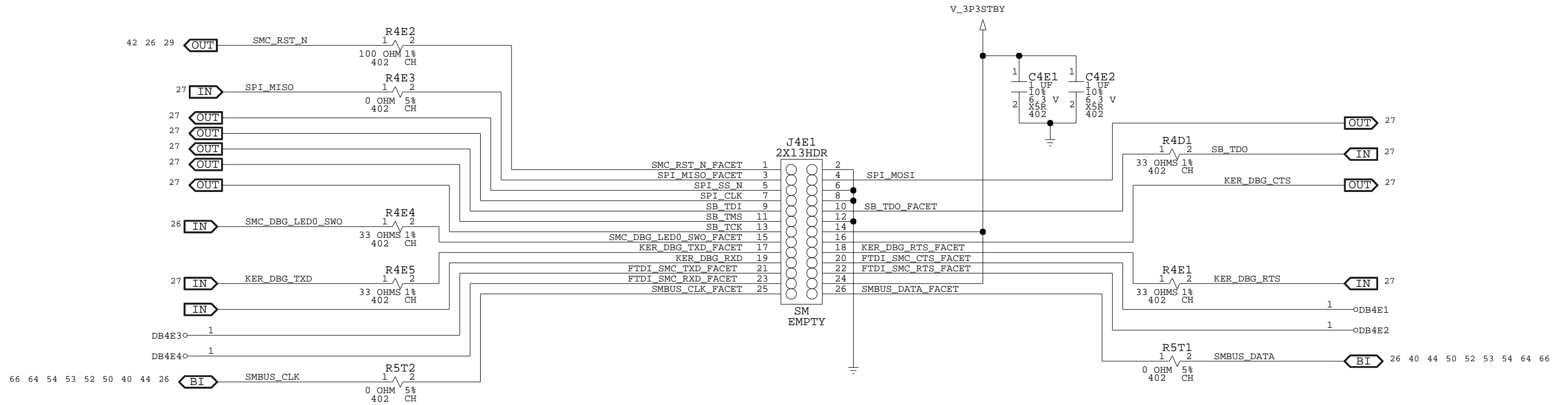


# I2C

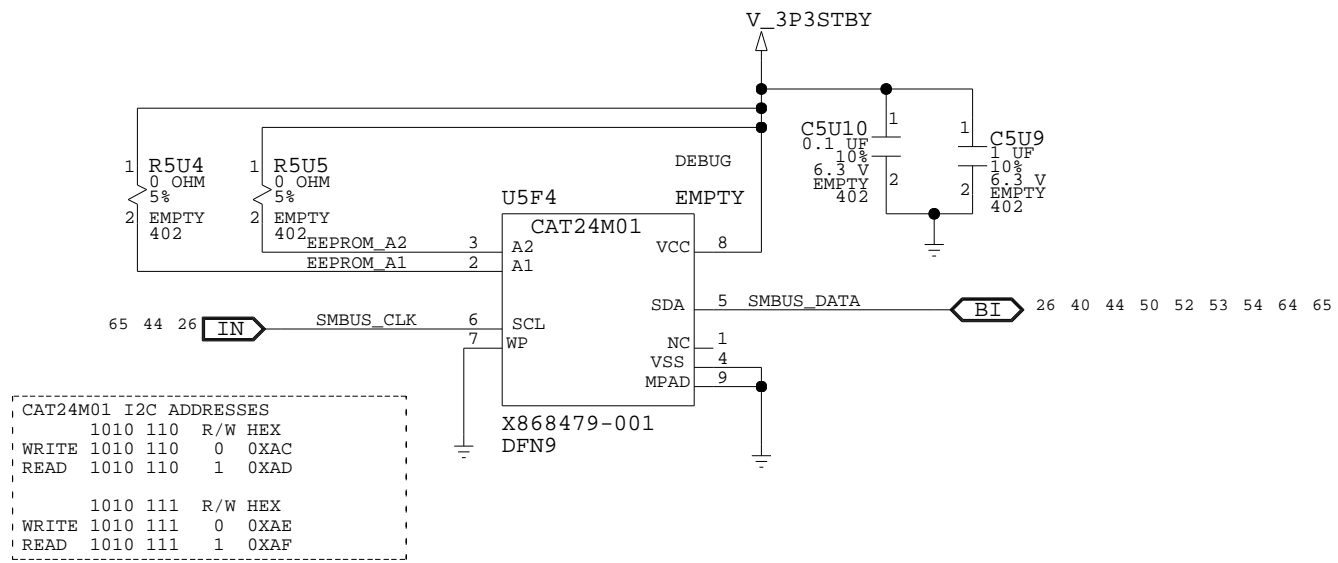




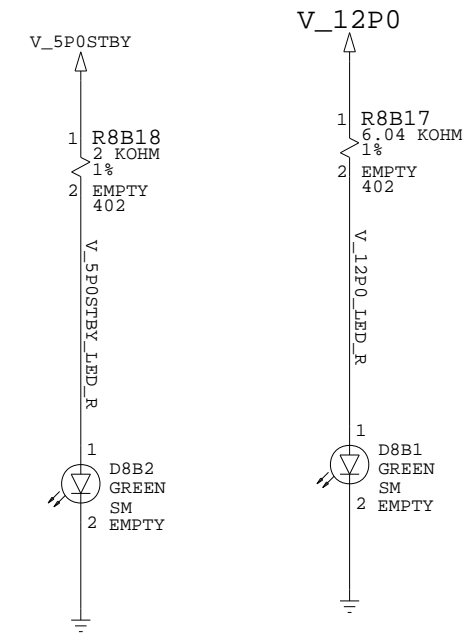
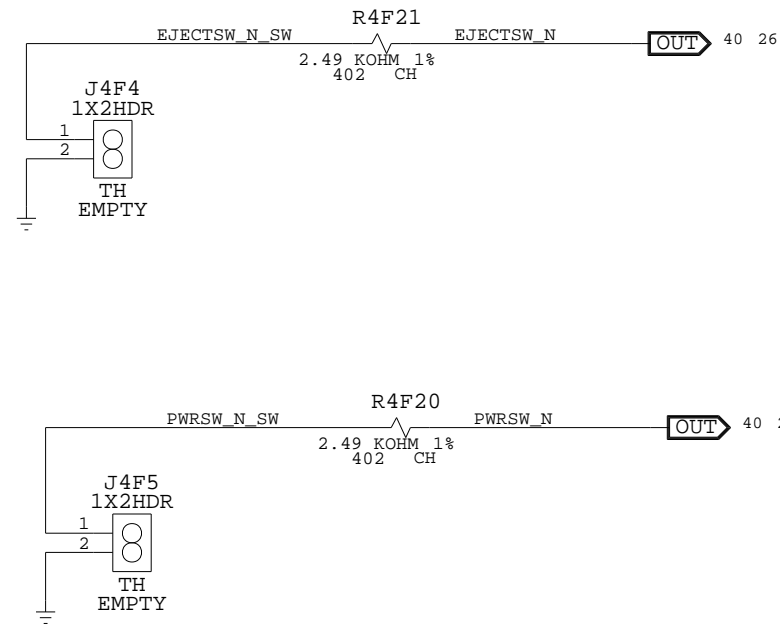
# FACET, FTDI



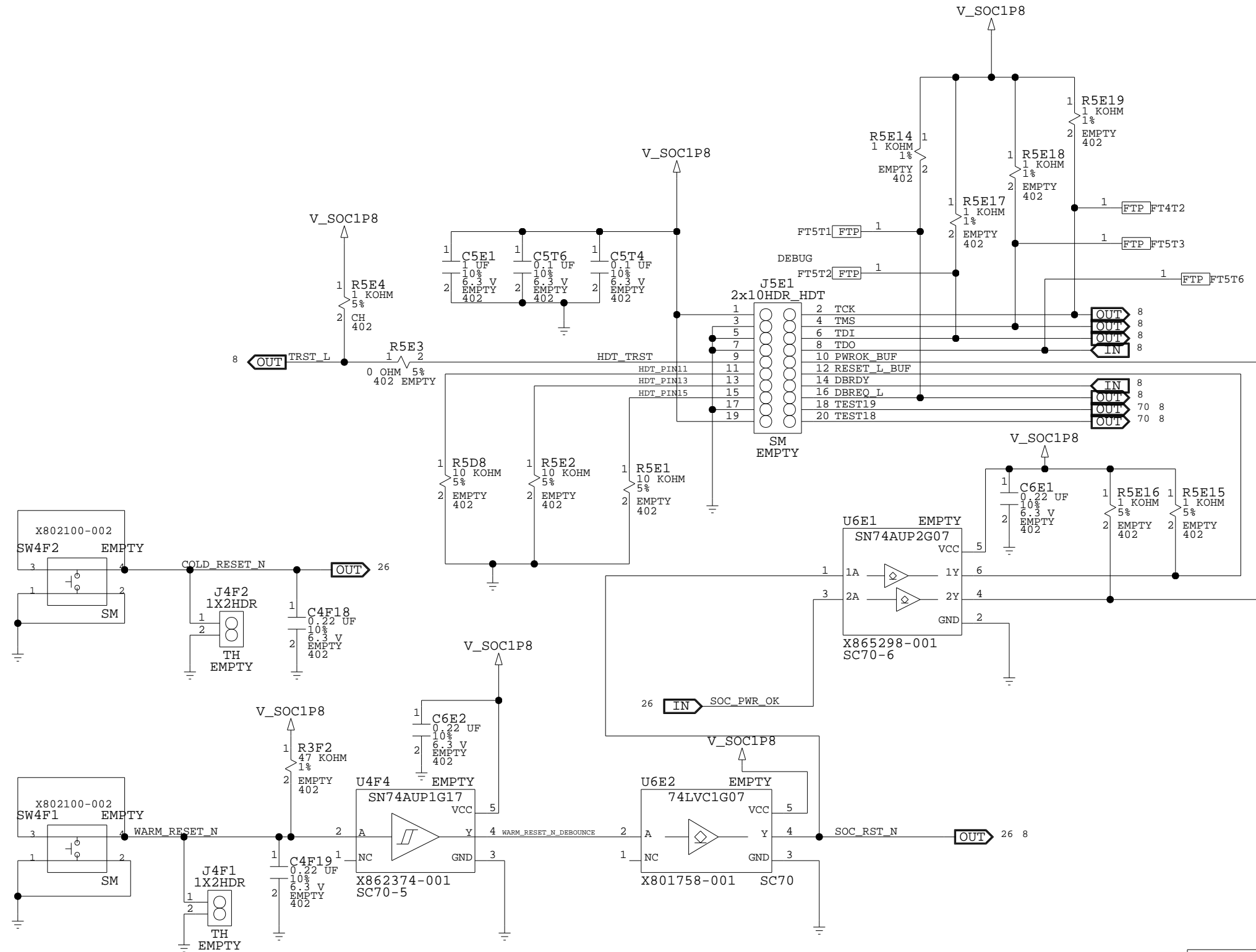
# FACET, FTDI+MISC



# CONN, SWITCHES

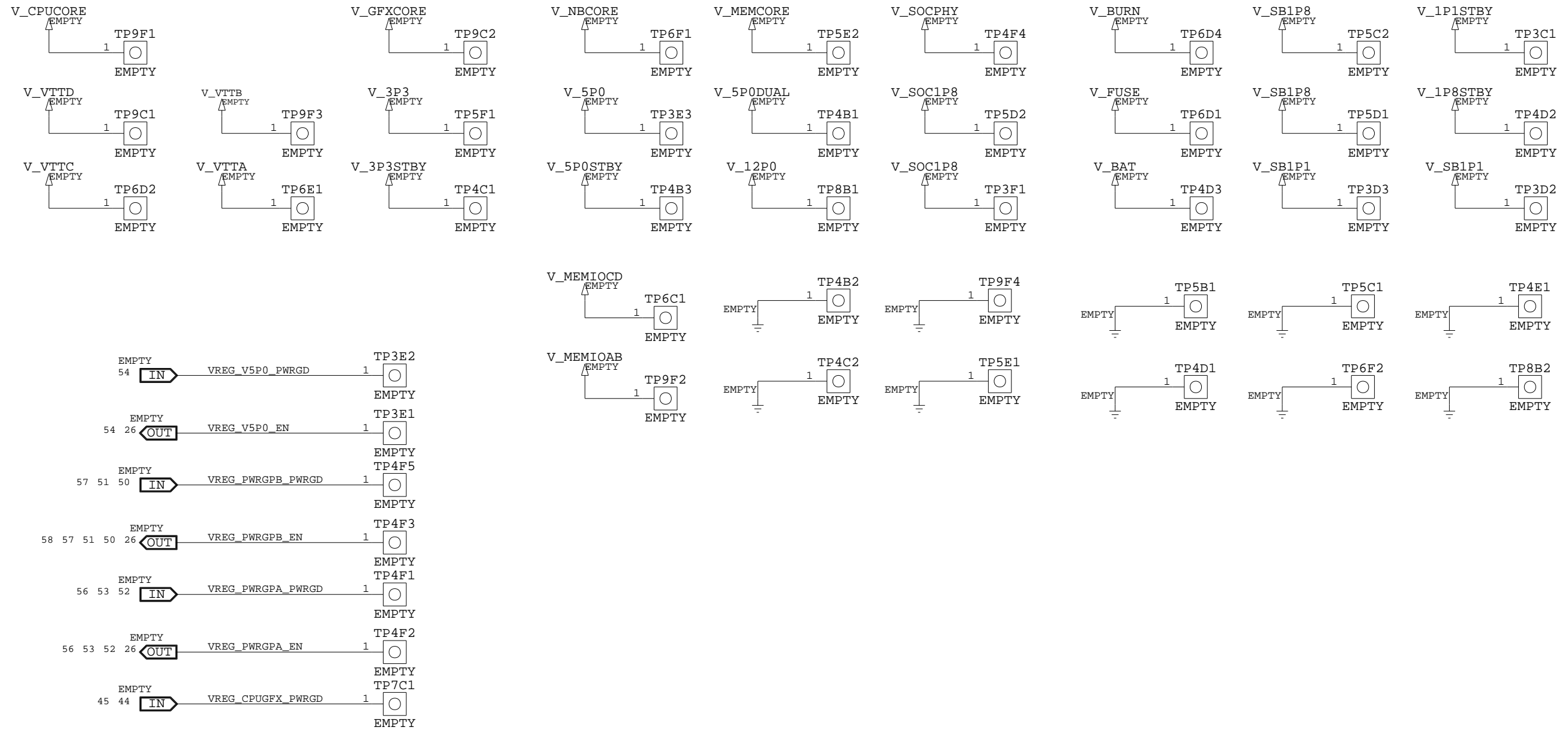


# CONN, HDT

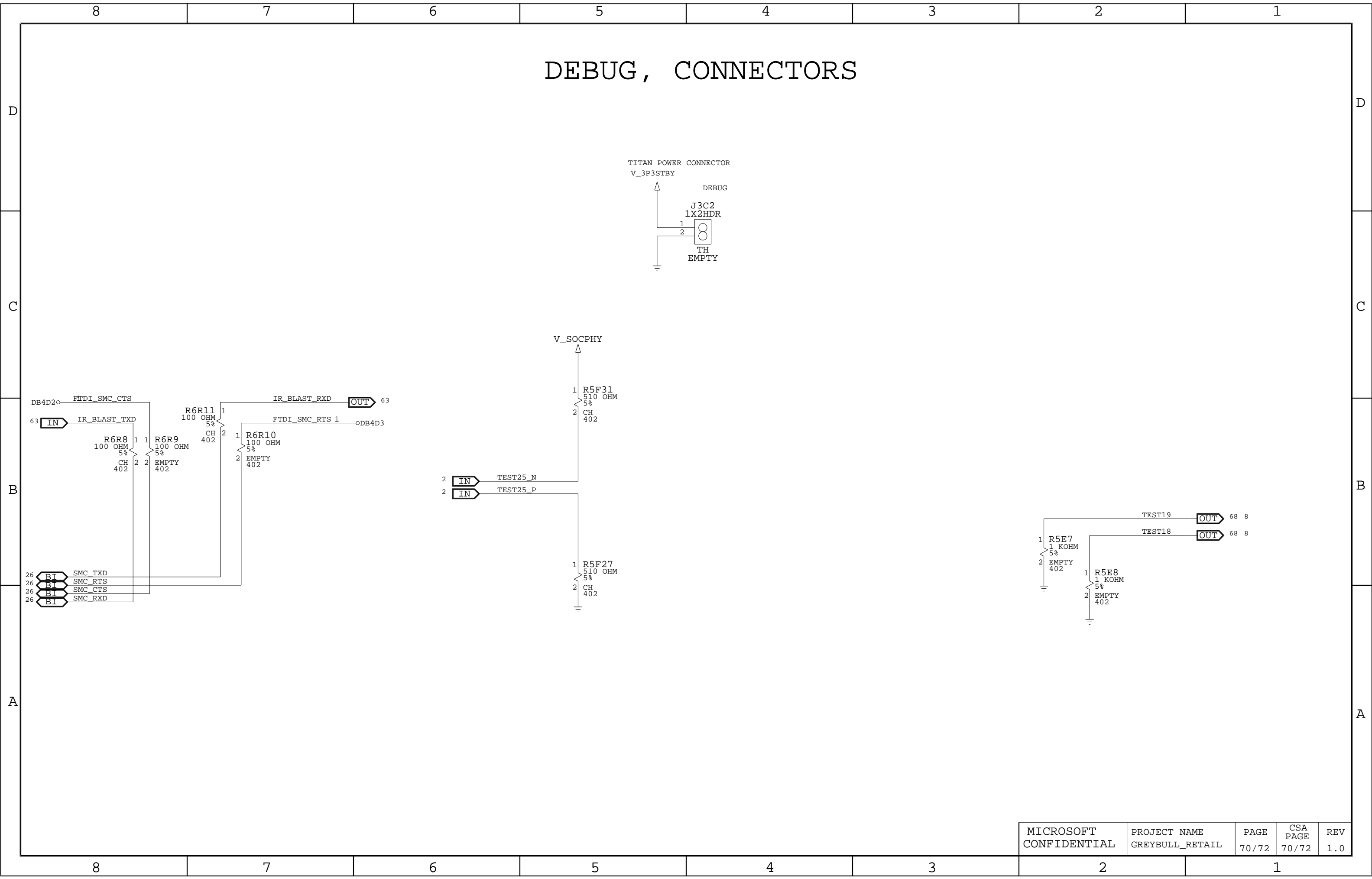


MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 68/72	CSA PAGE 68/72	FAB M	REV 1.0
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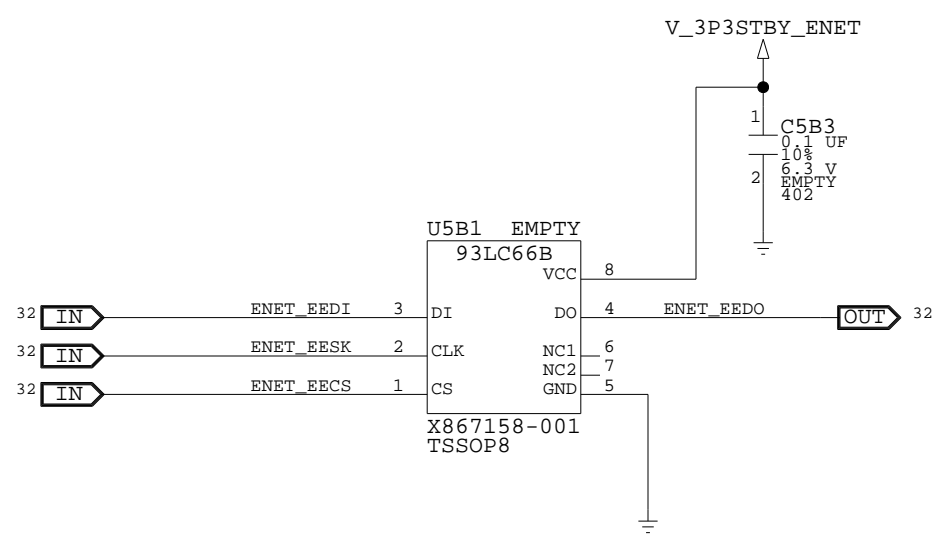
# DEBUG, VR HEADERS AND TEST POINTS



# DEBUG, CONNECTORS



# DEBUG, ENET EEPROM + MISC

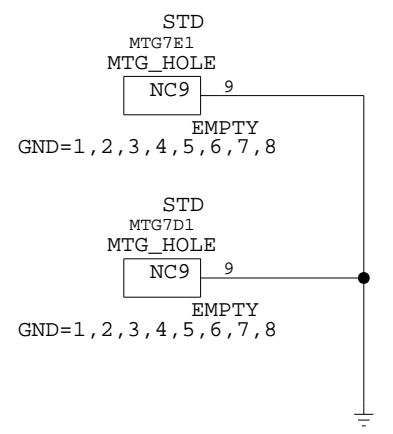
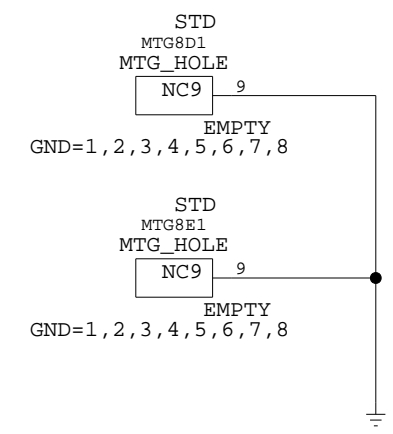


D

D

# LABELS AND MOUNTING

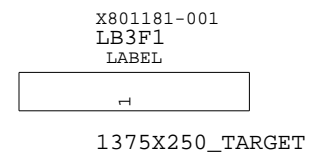
## HEAT SINK MOUNTING HOLES



C

C

## INTELLIGENT SERIAL NUMBER TARGET



B

B

A

A

MICROSOFT CONFIDENTIAL	PROJECT NAME GREYBULL_RETAIL	PAGE 72/72	CSA PAGE 72/72	FAB M	REV 1.0
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