CR-1 : @TUSCANY_LIB.TUSCANY(SCH_1):PAGE1

SCHEMATIC REV	PBA NUMBER	REV	BOM RELEASE DATE
5.1	X800101-100	F	04/13/04

********** IMPORTANT **********
SCHEMATIC CORRESPONDS TO BOM REVISION INDICATED.
PLEASE REFER TO AGILE FOR LATEST BOM AND ECOS FOR UPDATES

DVT
REV 5.1

FAB J/K
XM3

TUSCANY

PLEASE REFER TO THE TUSCANY DESIGN SPEC

NOTE: THIS SCHEMATIC REPRESENTS 4 DIFFERENT BOARD VERSIONS LISTED BELOW.

XM2 VERSIONS (-1X0) HAVE NOTES BESIDE COMPONENTS THAT CHANGE BETWEEN VERSIONS. XM3 VERSIONS (-1X1) SHOW PRODUCTION STUFFING.

FAB J BOARDS ARE THE -12X BOARDS (DVT1)
THESE HAVE 2 FOOTPRINTS FOR THE SUPERCAP

FAB K BOARDS ARE THE -13X BOARDS (DVT3)
THESE HAVE 1 FOOTPRINT FOR THE SUPERCAP

PAGES WITH DIFFERENCES ARE: 19, 35, 40

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

[PAGE_TITLE=COVER PAGE]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:55:10 2004

X01063-120(XM2)/X01063-121(XM3)

BOM RELEASE DATE	04/13/04	PB NUMBER X01063-130(XM2)/X01063-131(XM3)			
SIGNATURE	DATE	MICROSOFT XBOX			
DRN BY					
CHK BY		TITLE			
ENGR APVD		SCH, PBA, TUSCANY			
APVD		MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
APVD			TUSCANY	1/48	5.1

GPIO USAGE TABLE

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
MCPX	GPIO0	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO1	OUT	VCC3	H	H	CNFG_SEL1
MCPX	GPIO14	IN	VCC3	Z	Z	CNFG_SEL0
MCPX	GPIO15	OUT	VCC3	Z	Z	TP_DEBUG_GPIO15
MCPX	GPIO16	IN	VCC3	Z	Z	CNFG_SEL2
MCPX	GPIO19	OUT	VCC3	Z	Z	LVLCNT1
MCPX	GPIO20	OUT	VCC3	Z	Z	TESTPOINT (NOT USED)
MCPX	GPIO21	IN	VCC3	H	H	SMI* INPUT FROM SMC
MCPX	GPIO22	OUT	VCC3	Z	Z	LVLCNT0
MCPX	GPIO24		VCC3	Z	Z	TESTPOINT (NOT USED)

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
XCAL	GPIO0	I/O	?	?	?	UNUSED
XCAL	GPIO1	I/O	?	?	?	UNUSED
XCAL	GPIO2	I/O	?	?	?	UNUSED
XCAL	GPIO3	I/O	?	?	?	UNUSED

DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
XYCL	GPIO	I/O	?	?	?	UNUSED
XYCL	RTCACTIVE	IN	?	?	?	UNUSED

VOLTAGE RAILS

RAIL	TYPICAL(V)
V_CPUCORE	1.68V
VCC	5V
VCC3	3.3V
V_3P3_STBY	3.3V STANDBY
V_2P5	2.65V
V_1P3	1.33V
V_1P5_VTT	1.5V
V_1P25_MEMVTT	1.325V
AUD_5V_ANALOG'	5V
VCC_SW	5V (SWITCHED)
+12V	12V (SWITCHED)
V_LDO_2P5	2.5V
V_1P8	1.857V

BOM CONSOLIDATIONS

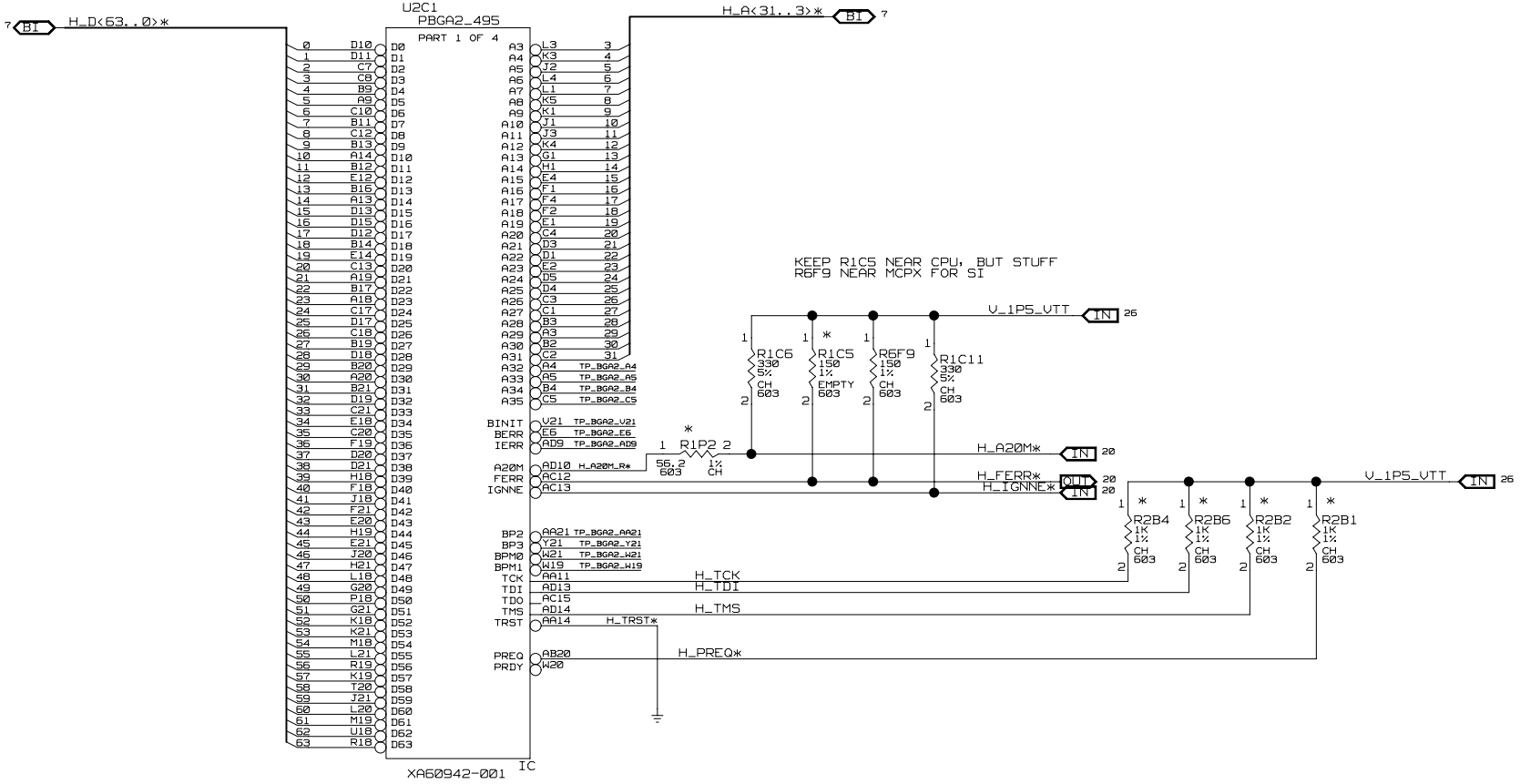
NOTE: COMPONENTS WITH A * HAVE BEEN CONSOLIDATED WITH SIMILAR PARTS.
TABLE BELOW SHOWS THE PARTS WHICH CHANGED. SEE CHANGELIST ON SHARE
(TUSCANY/EVT4/SCHEMATIC REVIEW MATERIAL) FOR MORE INFORMATION.

REF DES	OLD PART		NEW PART	
C4M5, C4N1, C4N4, C4N8, C4N11, C4N13, C4N14, C4N17, C4P4, C5N2	X602431-025	CAP,S/M,X7R,0.01 UF,50V,20%,0603	X603269-020	CAP,S/M,X7R,0.01 UF,50V,10%,0603
C4N19, C5N4	X626747-046	CAP,S/M,X7R,0.01 UF,50V,5%,0603	X603269-020	CAP,S/M,X7R,0.01 UF,50V,10%,0603
R6F3, R6F4, R8B4, R8G3	X202285-053	RES,S/M,1.5K,5%,1/16W,0603	X202286-211	RES,S/M,1.54K OHM,1%,1/16W,0603
R3G2, R3V2, R6A9, R7B2	X202285-025	RES,S/M,100 OHM,5%,1/16W,0603	X202286-097	RES,S/M,100.0 OHM,1%,1/16W,0603
R1C5, R1C7, R1C8, R1C14, R1C15	X202285-029	RES,S/M,150 OHM,5%,1/16W,0603	X202286-114	RES,S/M,150.0 OHM,1%,1/16W,0603
R4R3, R6E1	X202286-068	RES,S/M,49.90 OHM,1%,1/16W,0603	XA36092-045	RES,S/M,49.90 OHM,1%,1/16W,0402
R1D1, R1D5, R1P2, R7C1	X202285-019	RES,S/M,56 OHM,5%,1/16W,0603	X202286-073	RES,S/M,56.20 OHM,1%,1/16W,0603
R6D1, R7C1	XA36093-016	RES,S/M,1K OHM,5%,1/16W,0402	X202286-193	RES,S/M,1.0K OHM,1%,1/16W,0603
R1C3, R1C4, R1C10, R1D2, R1D10, R1P3, R2B1, R2B2, R2B4, R2B6, R4M7, R4M10, R4P1, R5A1, R5G1, R5M3, R6A1, R6A2, R6A4, R6U1, R7C4, R7D3, R7E12, R7M4, R7M5, R8B5	X202285-049	RES,S/M,1K OHM,5%,1/16W,0603	X202286-193	RES,S/M,1.0K OHM,1%,1/16W,0603
R1D6, R6B3, R7E8, R7R2	X202285-065	RES,S/M,4.7K OHM,5%,1/16W,0603	X202286-258	RES,S/M,4.75K OHM,1%,1/16W,0603

[PAGE_TITLE=GPIO TABLE/VOLTAGE RAILS]

DRAWING
TUSCANY_FABK
Wed Jan 14 13:41:55 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	2	5.1



NC: A15, A16, A17, C14, D8, D14, D16, E15, G2, G5, G18, H3, H5, J5, M4, M5, P3, P4, AA5, AA19, AC3, AC20, AD15

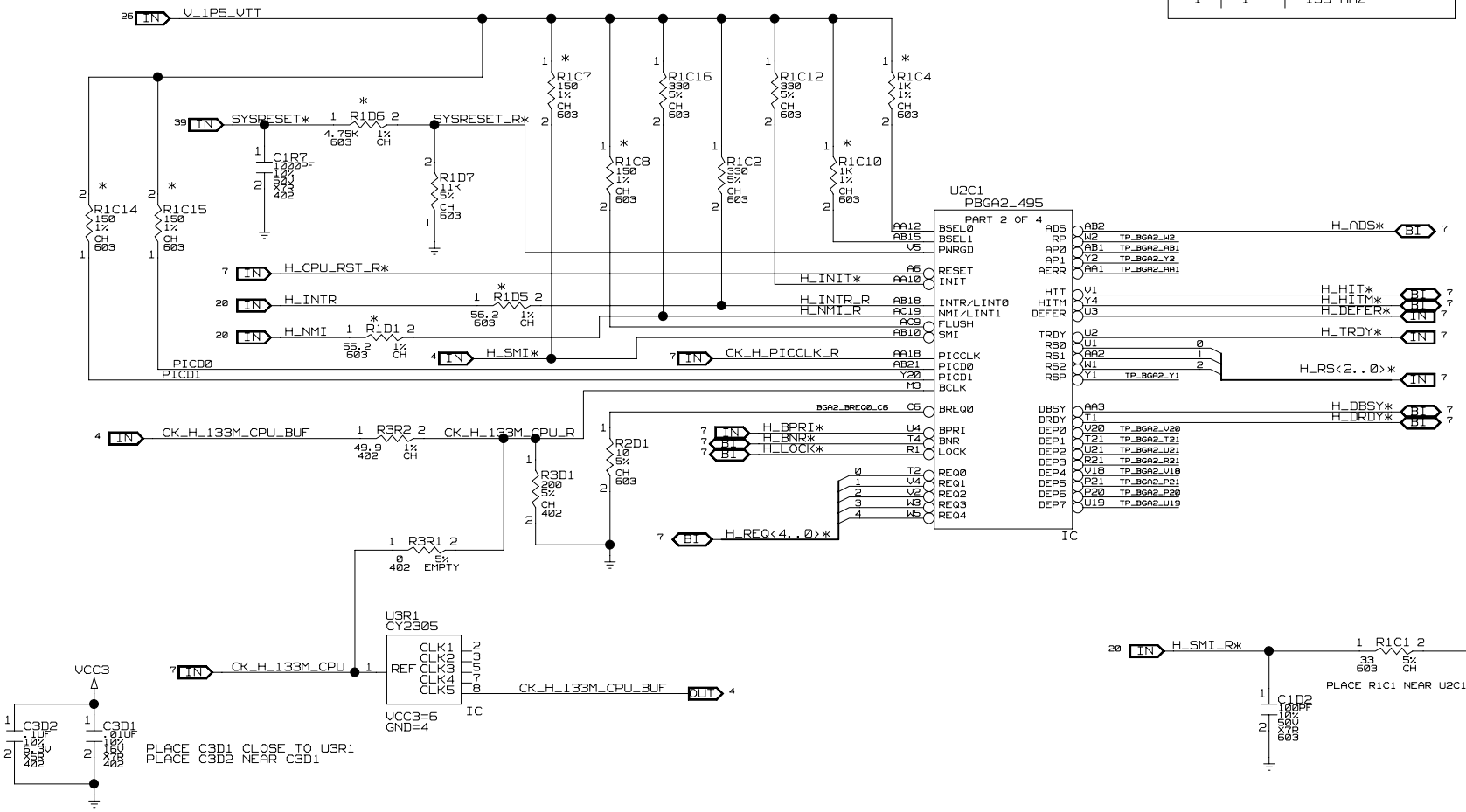
GND: A2, A7, A8, A12, A21, B1, B5, B6, B7, B8, B10, B15, B18, C9, C11, C15, C16, C19, D2, D6, D7, D9, E3, E7, E8, E9
GND: E10, E11, E13, E19, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F20, G3, G19, H2, H7, H9, H11, H13, H15
GND: H20, J4, J8, J10, J12, J14, J16, J19, K2, K7, K9, K11, K13, K15, K20, L5, L8, L10, L12, L14, L16, L19, M7, M9, M11
GND: M13, M15, M20, N2, N3, N4, N8, N10, N12, N14, N16, N18, N19, N20, P5, P7, P9, P11, P13, P15, P19, R3, R4, R5, R8, R10, R12, R14, R16, R20
GND: T3, T5, T7, T9, T11, T13, T15, T18, T19, U8, U10, U12, U14, U16, U20, V3, V19, W4, W18, Y3, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y19
GND: AA4, AA13, AA20, AB3, AB5, AB9, AB11, AB13, AB14, AB17, AC1, AC2, AC5, AC10, AC14, AC16, AC21, AD1, AD5, AD16, AD21, AC18

[PAGE_TITLE=PENTIUM III BGA2 PART 1 OF 4]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:26:47 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	3	5.1

BSEL1	BSEL0	SYSTEM BUS FREQUENCY
0	0	RESERVED
0	1	100 MHZ
1	0	RESERVED
1	1	133 MHZ



[PAGE_TITLE=PENTIUM III BGA2 PART 2 OF 4]

DRAWING
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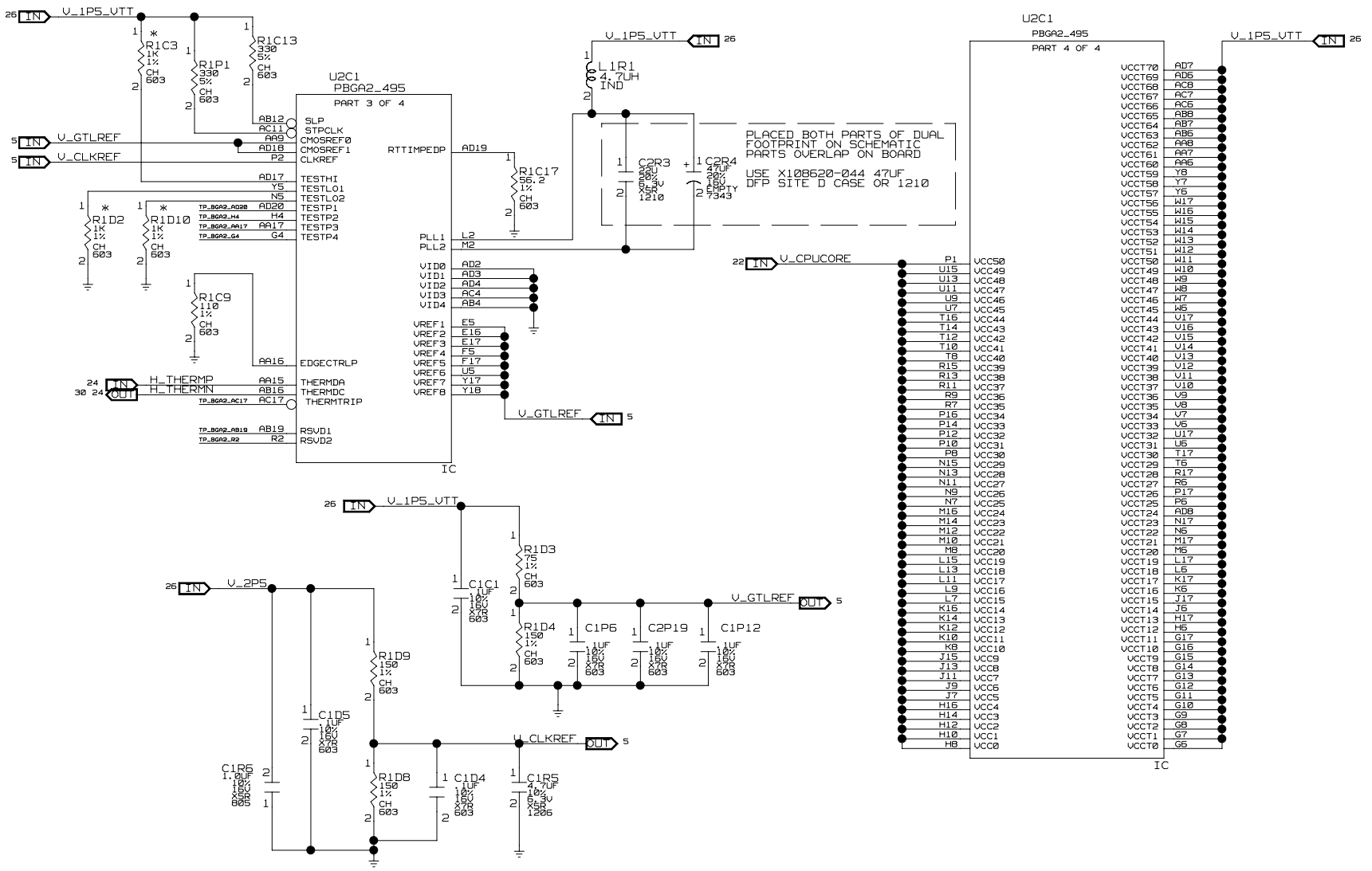
Mon Mar 15 14:26:56 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	4	5.1

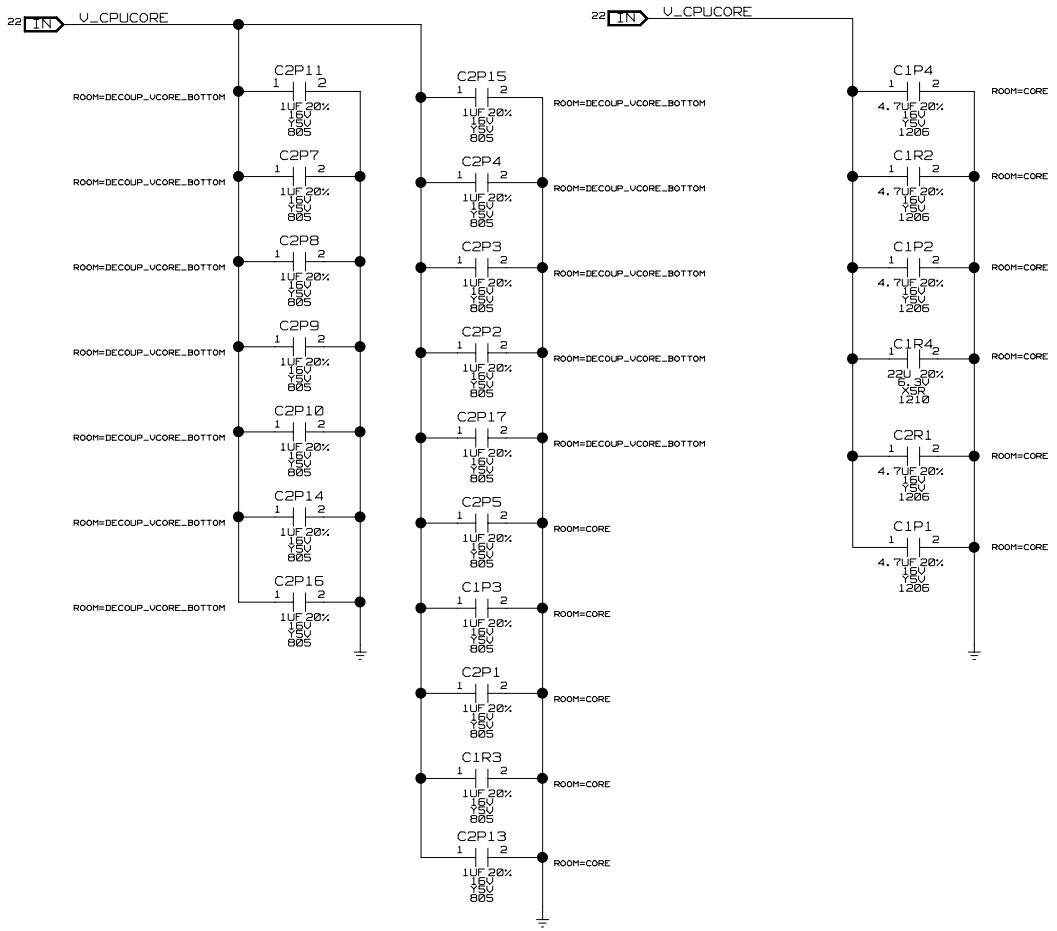


[PAGE_TITLE=PENTIUM III BGA2 PARTS 3 & 4]

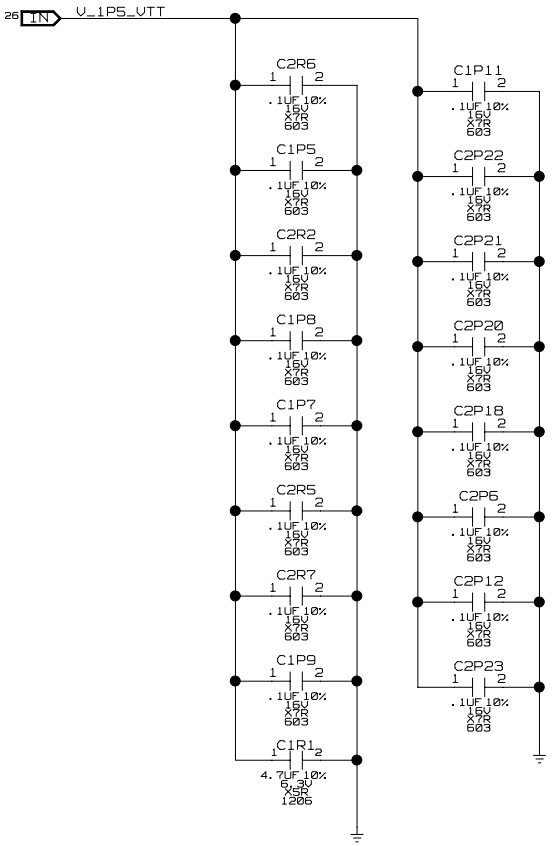
DRAWING
TUSCANY_FABK
Mon Mar 15 14:27:04 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	5	5.1

CPU VCORE DECOUPLING



CPU VTT DECOUPLING



[PAGE_TITLE=CPU VCORE/VTT DECOUPLING]

DRAWING
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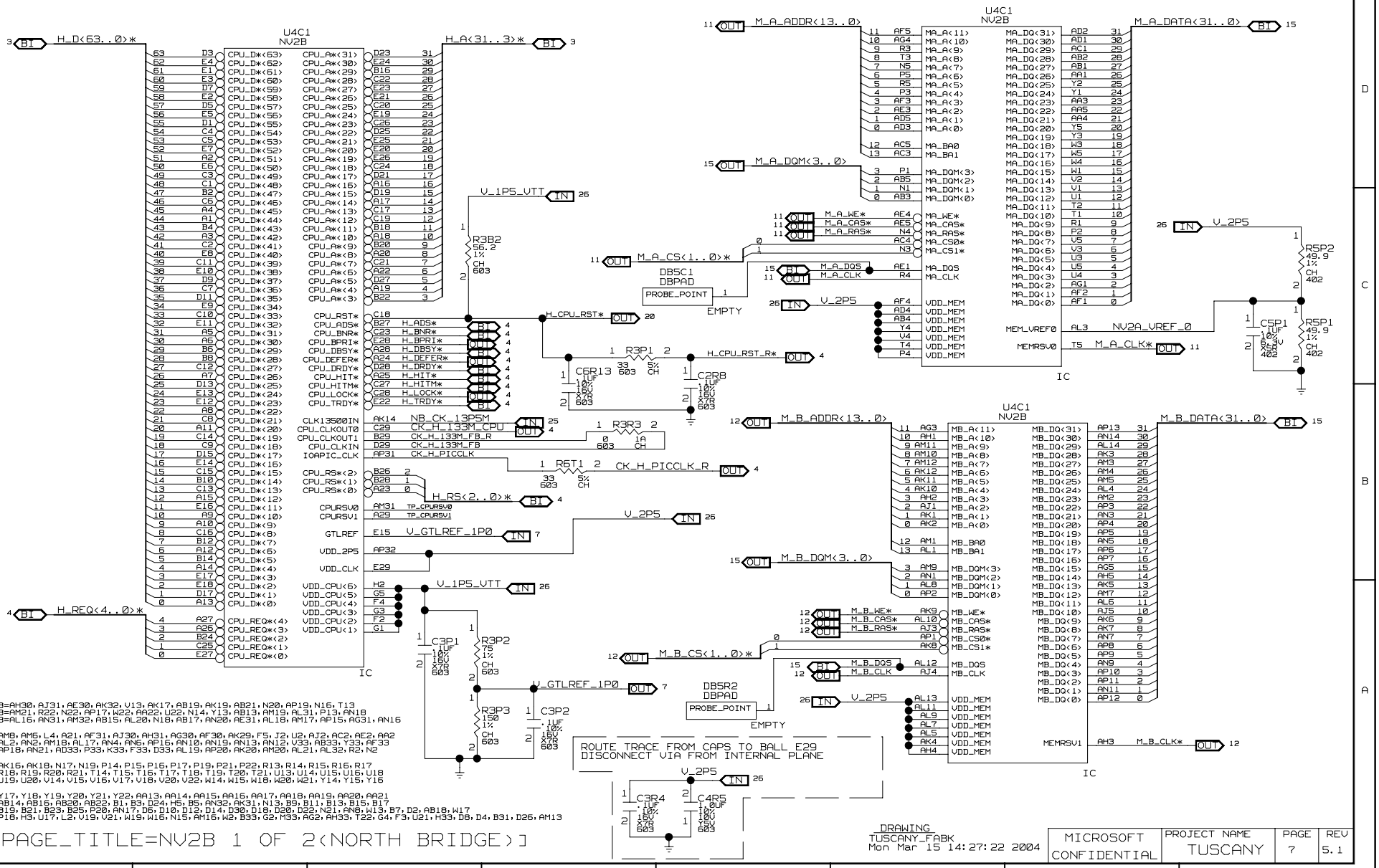
Mon Mar 15 14:27:12 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	6	5.1



V_1P3=AH30,AJ31,AE30,AK32,V13,AK17,AB19,AK19,AB21,N20,AP19,N16,T13
V_1P3=AM21,R22,N22,AP17,W22,AA22,U22,N14,Y13,AB13,AM19,AL31,P13,AN18
V_1P3=AL16,AN31,AM32,AB15,AL20,N18,AB17,AN20,AE31,AL18,AM17,AP15,AG31,AN16

GND=AM8,AM6,L4,A21,AF31,AJ30,AH31,AG30,AF30,AK29,F5,J2,U2,AJ2,AC2,AE2,AA2
GND=AL2,AN2,AM18,AL17,AN4,AN6,AP16,AN10,AN19,AN13,AN12,V33,AB33,Y33,AF33
GND=AP18,AN21,AD33,P33,K33,F33,D33,AL19,AP20,AK20,AM20,AL21,AL32,R2,N2

GND=AK16,AK18,N17,N19,P14,P15,P16,P17,P19,P21,P22,R13,R14,R15,R16,R17
GND=R18,R19,R20,R21,T14,T15,T16,T17,T18,T19,T20,T21,U13,U14,U15,U16,U18
GND=U19,U20,V14,V15,V16,V17,V18,V20,V22,W14,W15,W18,W20,W21,Y14,Y15,Y16

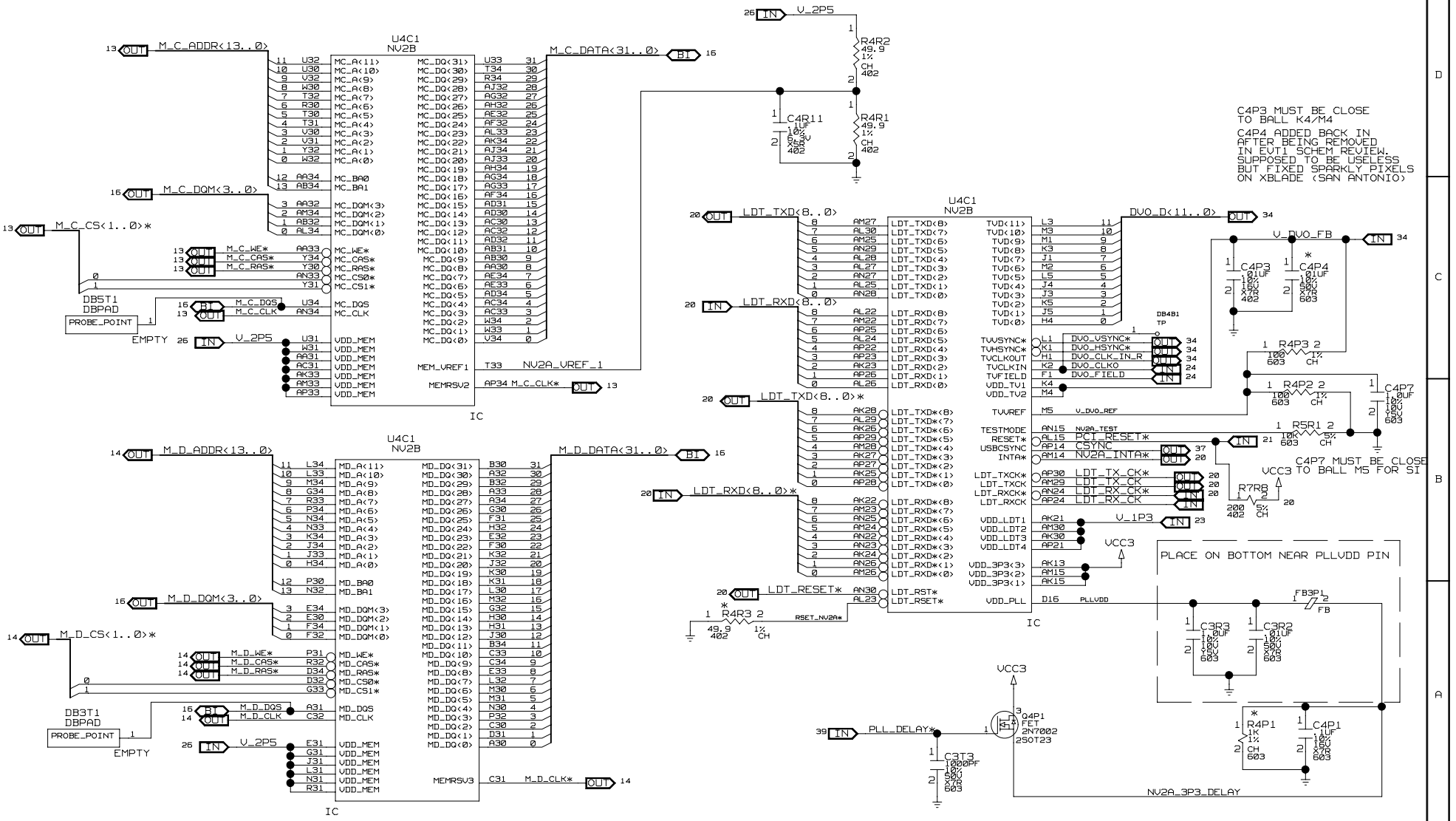
GND=Y17,Y18,Y19,Y20,Y21,Y22,AA13,AA14,AA15,AA16,AA17,AA18,AA19,AA20,AA21
GND=AB14,AB16,AB20,AB22,B1,B3,D24,H5,B5,AN32,AK31,N13,B9,B11,B13,B15,B17
GND=B19,B21,B23,B25,P20,AN17,D6,D10,D12,D14,D30,D18,D20,D22,N21,AN8,W13,B7,D2,AB18,W17
GND=P18,H3,U17,L2,V19,V21,W19,W16,N15,AM16,W2,B33,G2,M33,AG2,AH33,T22,G4,F3,U21,H33,D8,D4,B31,D26,AM13

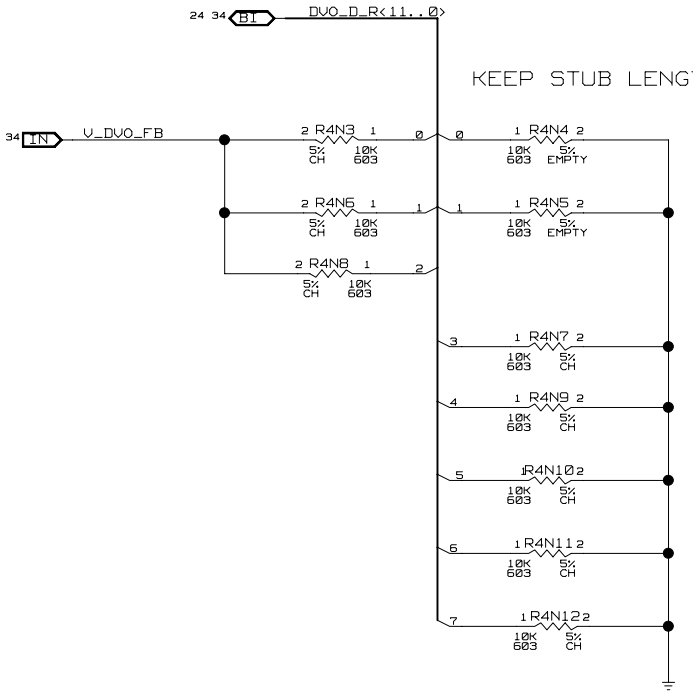
[PAGE_TITLE=NV2B 1 OF 2(NORTH BRIDGE)]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:27:22 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	7	5.1

CR-8 : @TUSCANY_LIB.TUSCANY(SCH_1):PAGE8





TVD		DEFINITION
[7]	0*	ENABLE INTERNAL LDT TERMINATION
	1	DISABLE INTERNAL LDT TERMINATION
[6]	0*	13.5MHZ OR 16.6MHZ
	1	14.31818MHZ
[5:4]	00*	USE FSB FREQUENCY BASED ON TVD[3:2]
	01	USE INTERNAL PROGRAMMED VALUE A
	10	USE INTERNAL PROGRAMMED VALUE B
	11	FORCE 66MHZ
[3:2]	00	NA
	01*	FSB FREQ=133MHZ FOR 16.6MHZ INPUT CLK
	10	NA
	11	NA
[1:0]	00*	BITS [1:0] ARE UNUSED ON TUSCANY
	01	USED TO BE MEMORY DRIVE STRENGTH SETTINGS
	10	NOW ALL SETTINGS READ FROM THE EEPROM
	11	

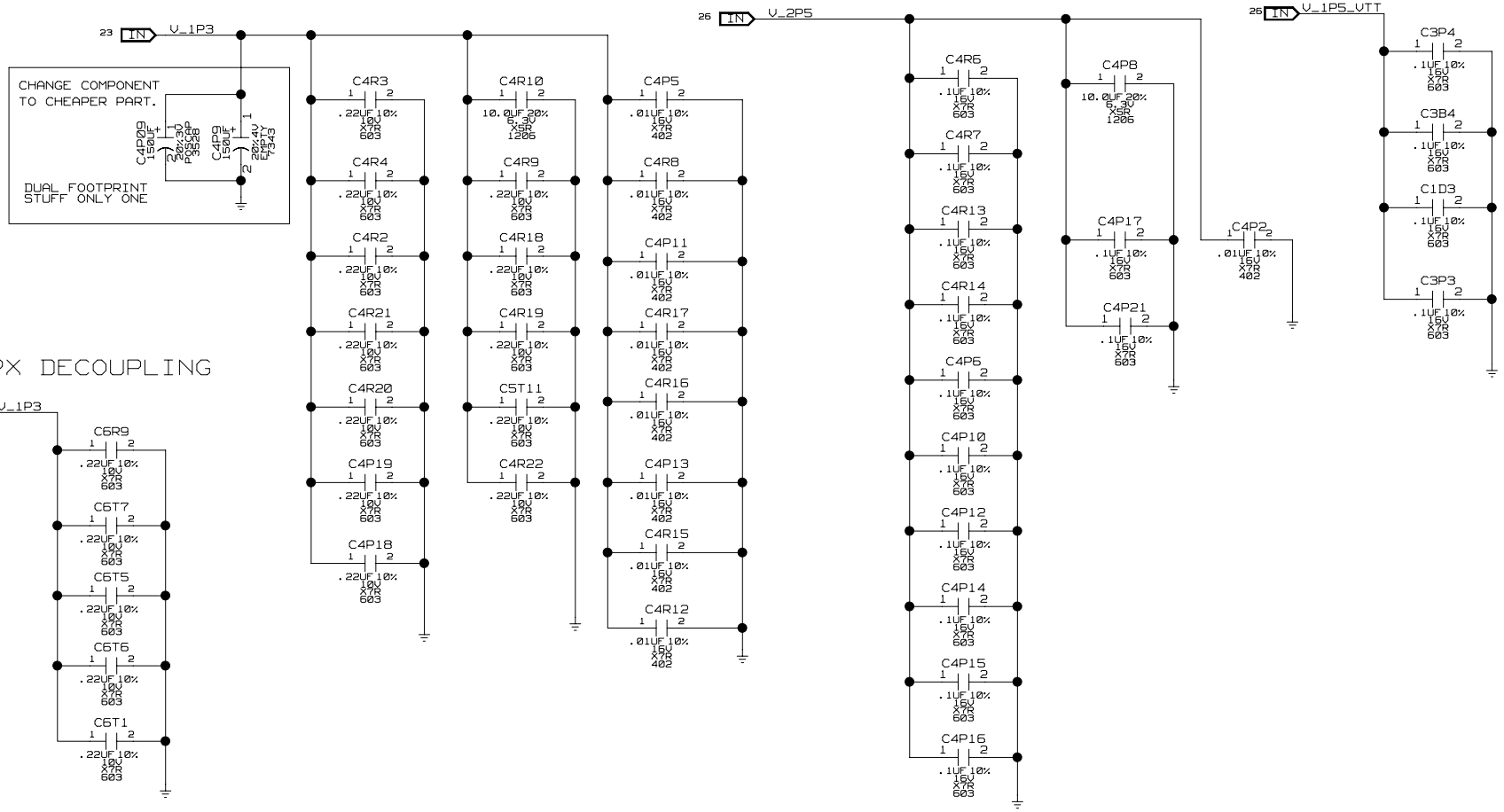
* = CURRENT SETTING

[PAGE_TITLE=NV2B STRAPPING]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:27:53 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	9	5.1

NV2B DECOUPLING



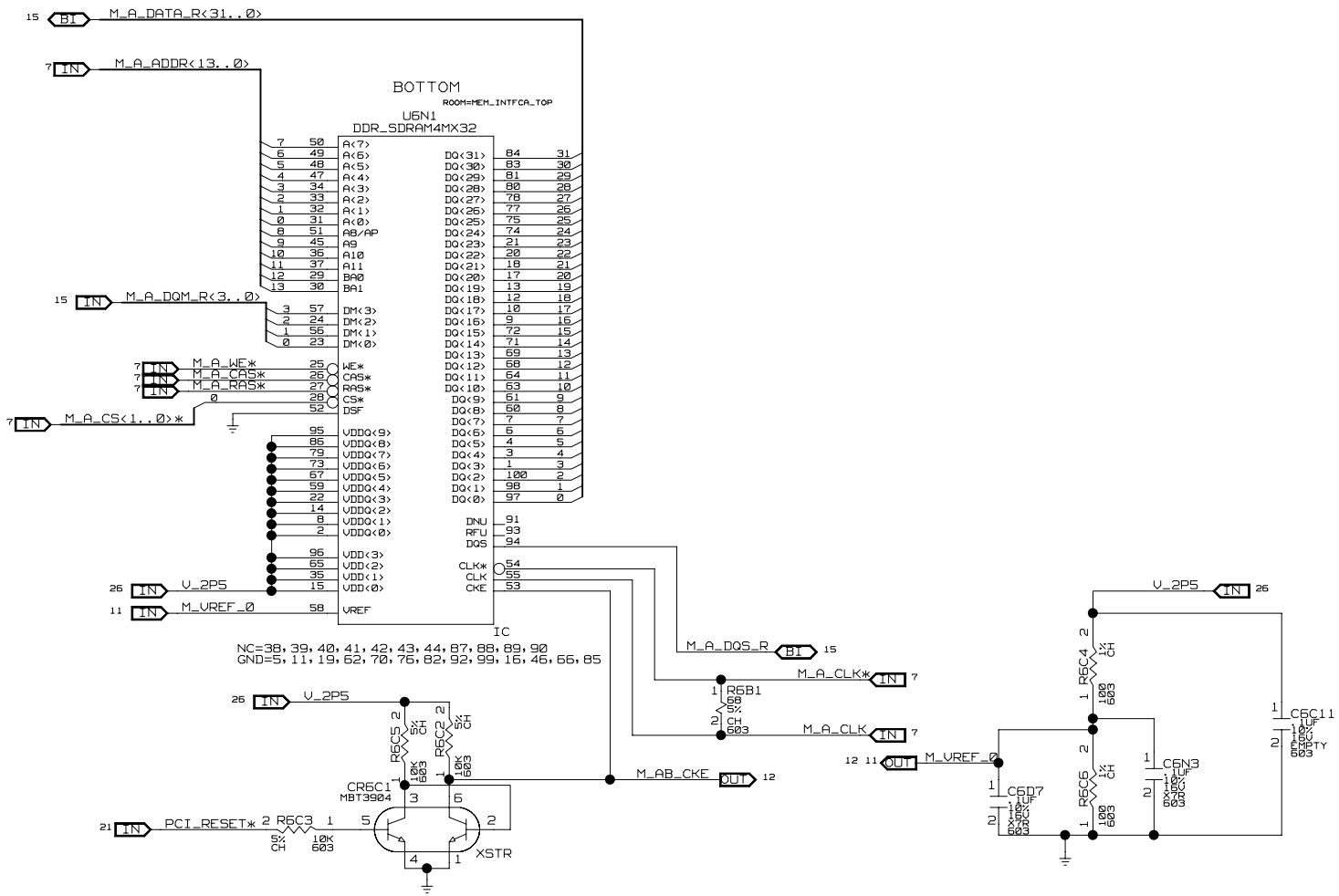
MCPX DECOUPLING

[PAGE_TITLE=NV2B/MCPX DECOUPLING]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:28:05 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	10	5.1

MEMORY INTERFACE PARTITION A

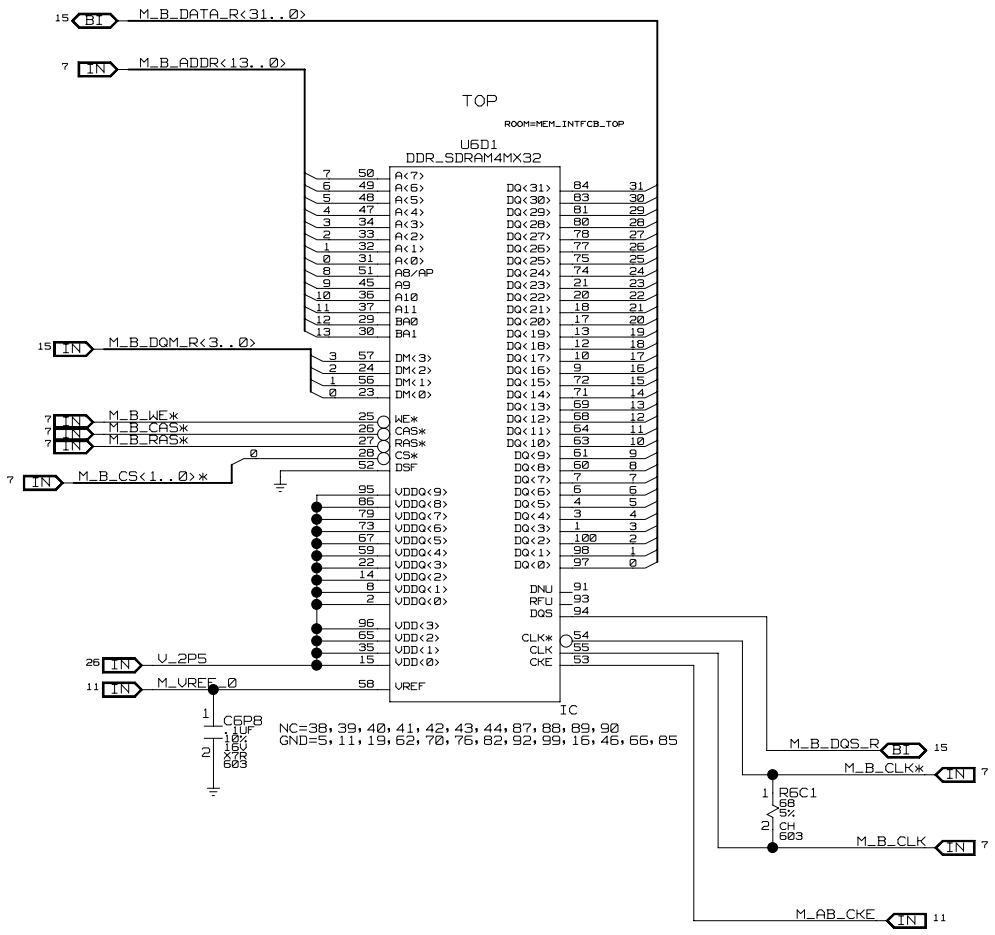


[PAGE_TITLE=DDR SDRAM (PARTITION A)]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:28:17 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	11	5.1

MEMORY INTERFACE PARTITION B

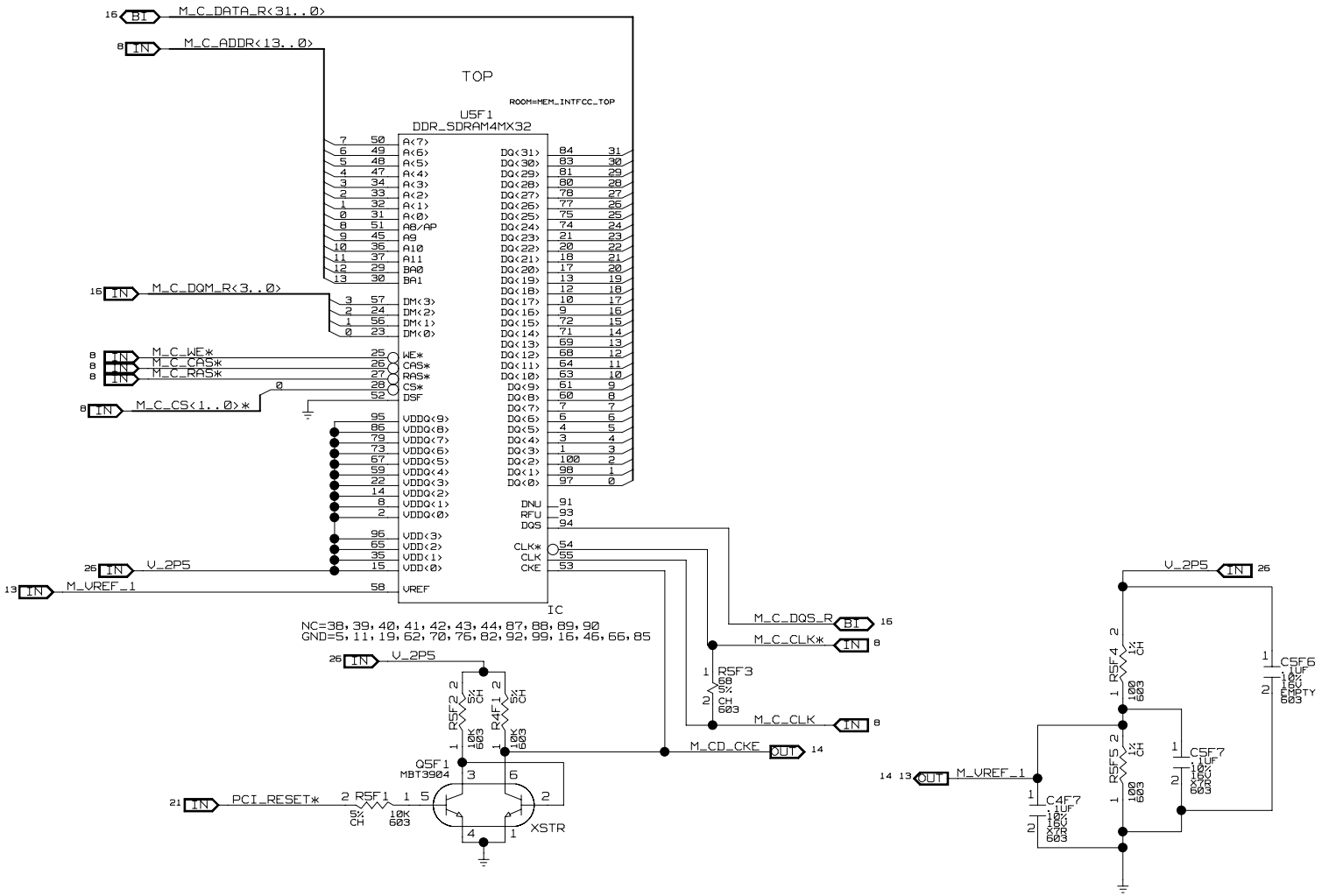


[PAGE_TITLE=DDR SDRAM (PARTITION B)]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:28:30 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	12	5.1

MEMORY INTERFACE PARTITION C

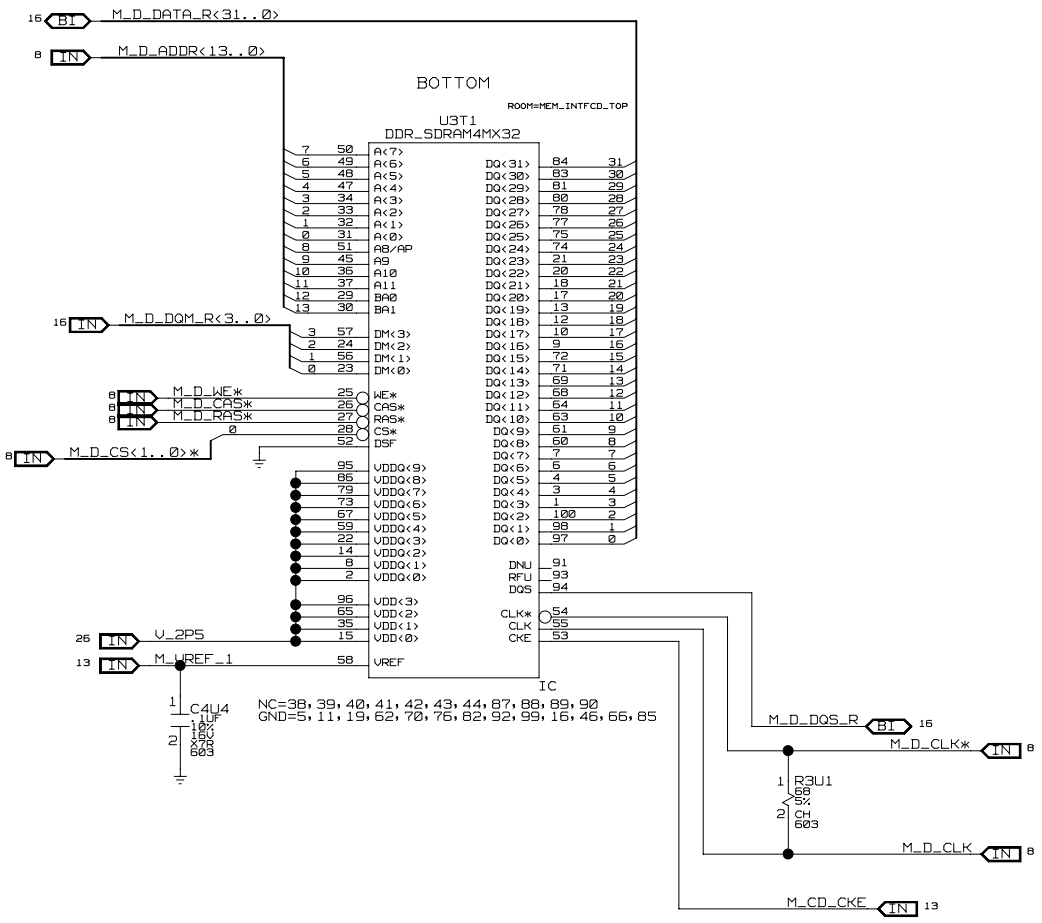


[PAGE_TITLE=DDR SDRAM (PARTITION C)]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:28:47 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	13	5.1

MEMORY INTERFACE PARTITION D



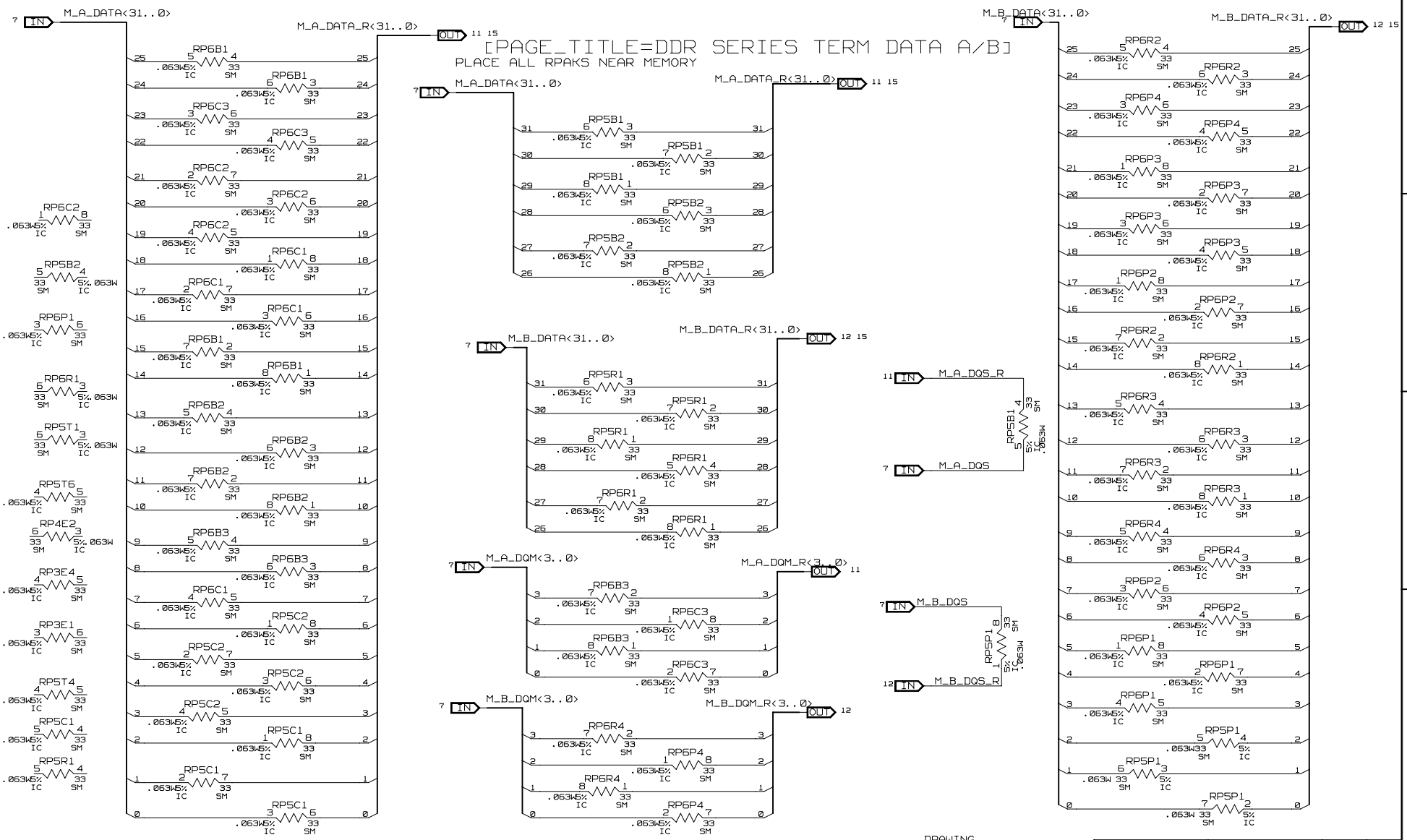
[PAGE_TITLE=DDR SDRAM (PARTITION D)]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:29:34 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	14	5.1

[PAGE_TITLE=DDR SERIES TERM DATA A/B]

PLACE ALL RPAKS NEAR MEMORY



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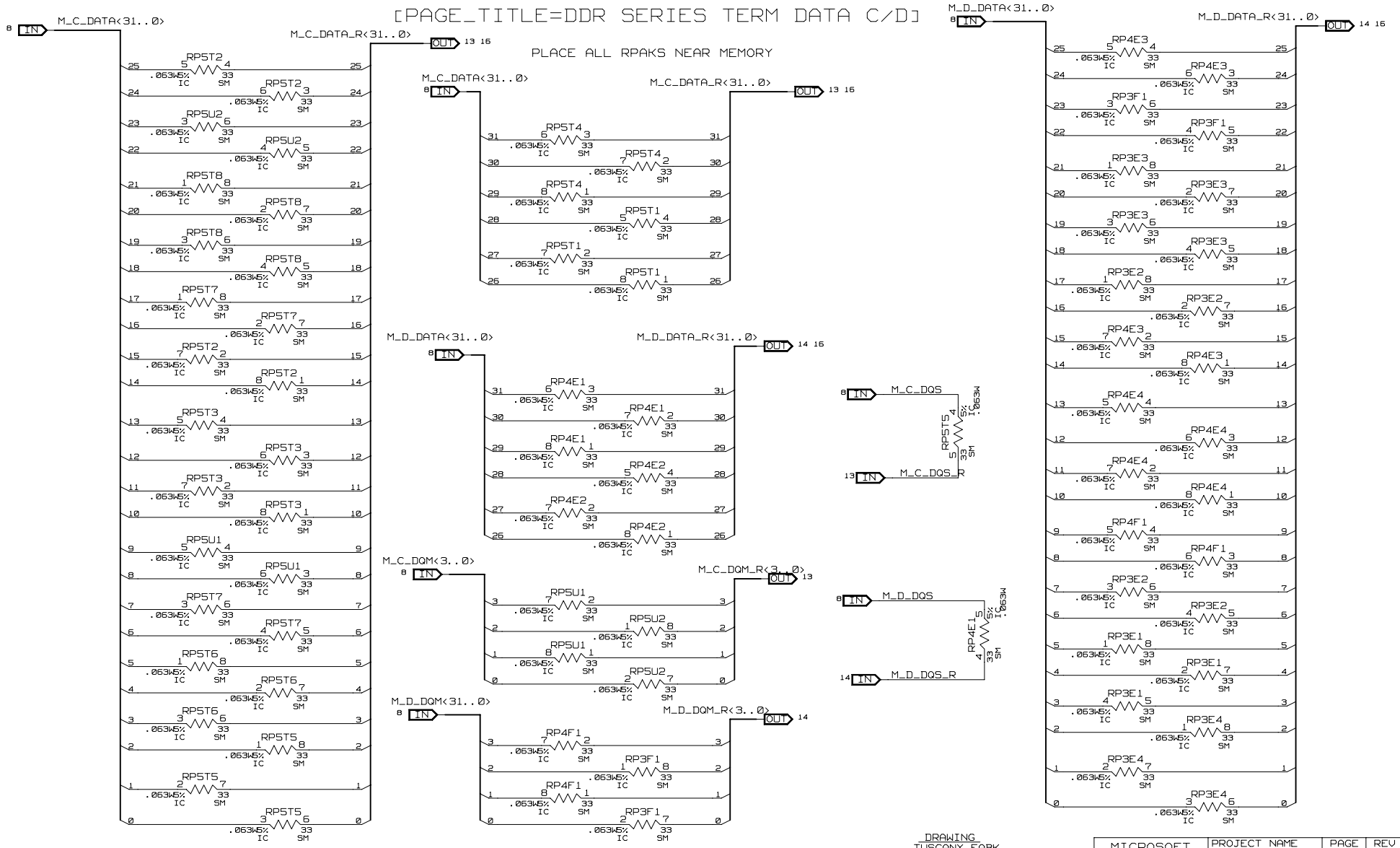
TUSCANY_FABK
Mon Mar 15 14:29:52 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	15	5.1

[PAGE_TITLE=DDR SERIES TERM DATA C/D]

PLACE ALL RPAKS NEAR MEMORY



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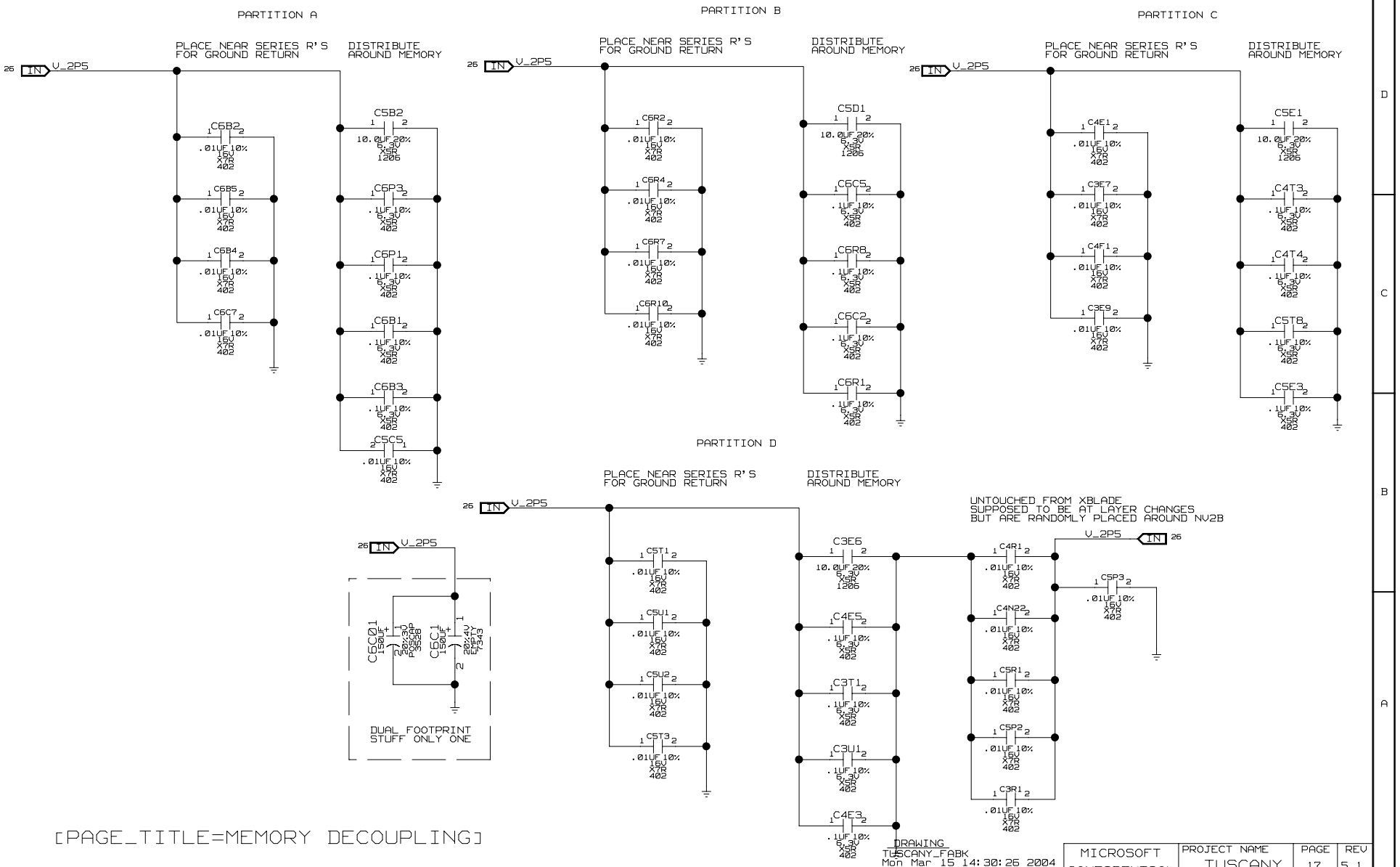
Mon Mar 15 14:30:09 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	16	5.1


PARTITION A
PLACE NEAR SERIES R'S FOR GROUND RETURN
DISTRIBUTE AROUND MEMORY
26 IN V_2P5
C6B2 .01UF 10% 16V X7R 402
C6B5 .01UF 10% 16V X7R 402
C6B4 .01UF 10% 16V X7R 402
C6C7 .01UF 10% 16V X7R 402
C5B2 10.0UF 20% 6.3V X5R 1206
C6P3 .1UF 10% 6.3V X5R 402
C6P1 .1UF 10% 6.3V X5R 402
C6B1 .1UF 10% 6.3V X5R 402
C6B3 .1UF 10% 6.3V X5R 402
C5C5 .01UF 10% 16V X7R 402
PARTITION B
PLACE NEAR SERIES R'S FOR GROUND RETURN
DISTRIBUTE AROUND MEMORY
26 IN V_2P5
C6R2 .01UF 10% 16V X7R 402
C6R4 .01UF 10% 16V X7R 402
C6R7 .01UF 10% 16V X7R 402
C6R10 .01UF 10% 16V X7R 402
C5D1 10.0UF 20% 6.3V X5R 1206
C6C5 .1UF 10% 6.3V X5R 402
C6R8 .1UF 10% 6.3V X5R 402
C6C2 .1UF 10% 6.3V X5R 402
C6R1 .1UF 10% 6.3V X5R 402
PARTITION C
PLACE NEAR SERIES R'S FOR GROUND RETURN
DISTRIBUTE AROUND MEMORY
26 IN V_2P5
C4E1 .01UF 10% 16V X7R 402
C3E7 .01UF 10% 16V X7R 402
C4F1 .01UF 10% 16V X7R 402
C3E9 .01UF 10% 16V X7R 402
C5E1 10.0UF 20% 6.3V X5R 1206
C4T3 .1UF 10% 6.3V X5R 402
C4T4 .1UF 10% 6.3V X5R 402
C5T8 .1UF 10% 6.3V X5R 402
C5E3 .1UF 10% 6.3V X5R 402
PARTITION D
PLACE NEAR SERIES R'S FOR GROUND RETURN
DISTRIBUTE AROUND MEMORY
26 IN V_2P5
C5T1 .01UF 10% 16V X7R 402
C5U1 .01UF 10% 16V X7R 402
C5U2 .01UF 10% 16V X7R 402
C5T3 .01UF 10% 16V X7R 402
C3E6 10.0UF 20% 6.3V X5R 1206
C4E5 .1UF 10% 6.3V X5R 402
C3T1 .1UF 10% 6.3V X5R 402
C3U1 .1UF 10% 6.3V X5R 402
C4E3 .1UF 10% 6.3V X5R 402
UNTOUCHED FROM XBLADE
SUPPOSED TO BE AT LAYER CHANGES
BUT ARE RANDOMLY PLACED AROUND NV2B
V_2P5 IN 26
C4R1 .01UF 10% 16V X7R 402
C5P3 .01UF 10% 16V X7R 402
C4N22 .01UF 10% 16V X7R 402
C5R1 .01UF 10% 16V X7R 402
C5P2 .01UF 10% 16V X7R 402
C3R1 .01UF 10% 16V X7R 402
26 IN V_2P5
C6C01 150UF+ 20% 2.5V POSCAP 3528
C6C1 150UF+ 20% 2V EMPTY 7343
DUAL FOOTPRINT
STUFF ONLY ONE
[PAGE_TITLE=MEMORY DECOUPLING]
DRAWING
TUSCANY_FABK
Mon Mar 15 14:30:26 2004
MICROSOFT CONFIDENTIAL
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TUSCANY
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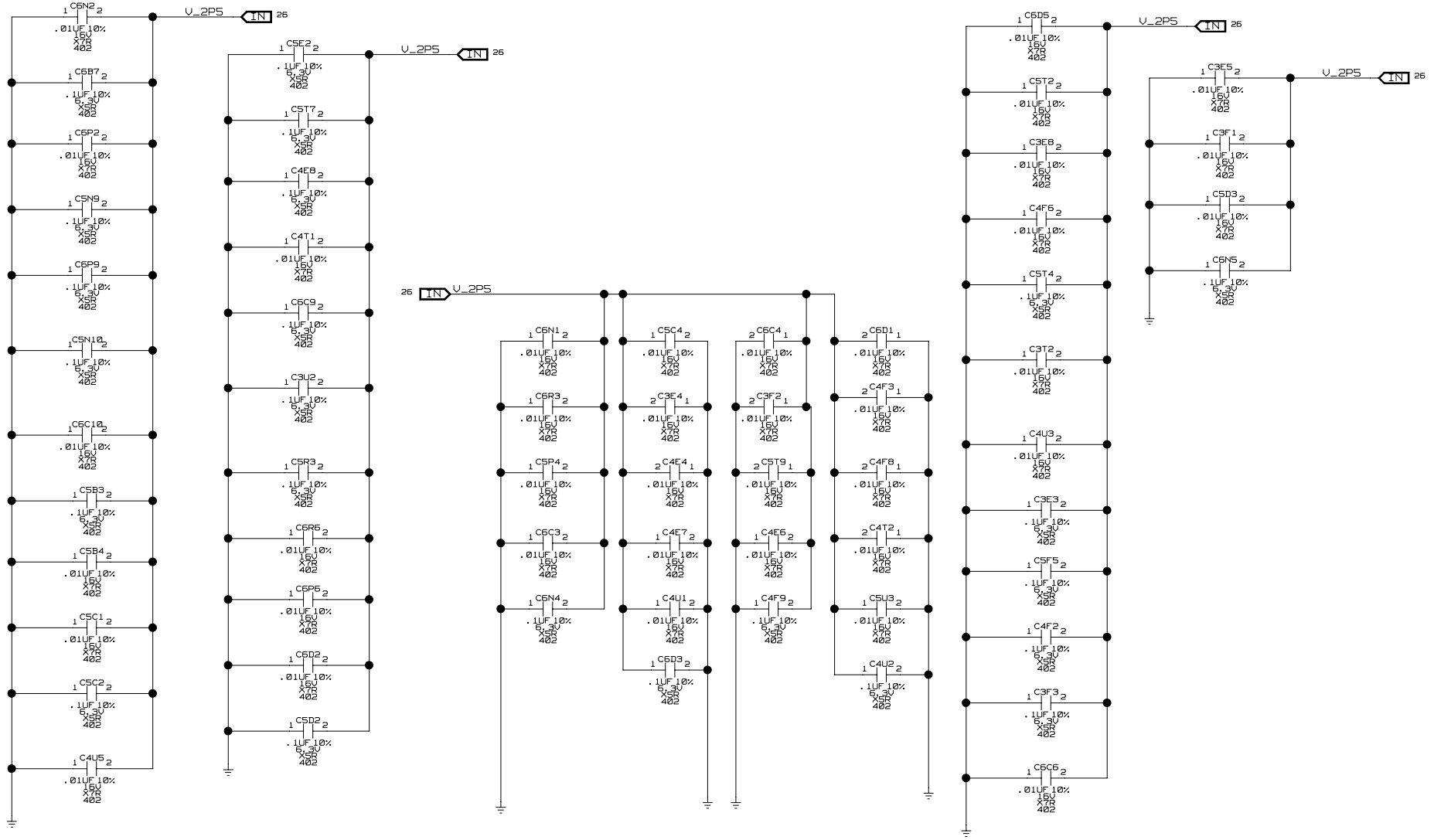
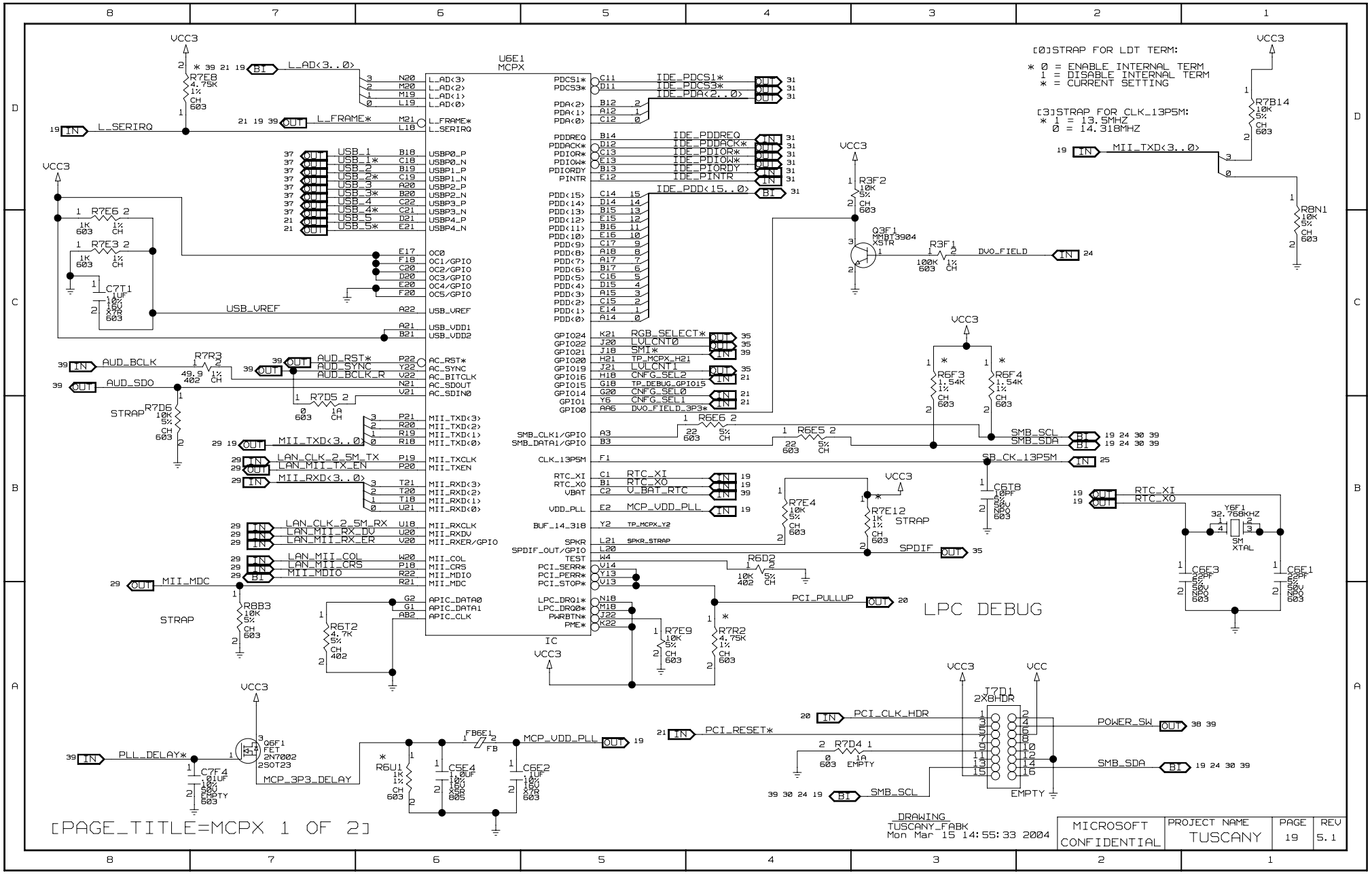
17
REV
5.1



[PAGE_TITLE=MEMORY DECOUPLING]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:30:42 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	18	5.1


U6E1
MCPX
[0]STRAP FOR LDT TERM:
* 0 = ENABLE INTERNAL TERM
1 = DISABLE INTERNAL TERM
* = CURRENT SETTING
[3]STRAP FOR CLK_13P5M:
* 1 = 13.5MHZ
0 = 14.318MHZ
L_AD<3..0>
L_FRAME*
L_SERIRQ
USB_1
USB_1*
USB_2
USB_2*
USB_3
USB_3*
USB_4
USB_4*
USB_5
USB_5*
USB_VREF
IDE_PDCS1*
IDE_PDCS3*
IDE_PDA<2..0>
IDE_PDDREQ
IDE_PDDACK*
IDE_PDIOR*
IDE_PDIOW*
IDE_PIORDY
IDE_PINTR
IDE_PDD<15..0>
RGB_SELECT*
LVL_CNT0
SMI*
LVL_CNT1
CNFG_SEL2
CNFG_SEL0
CNFG_SEL1
DVO_FIELD_3P3*
AUD_BCLK
AUD_SDO
AUD_RST*
AUD_SYNC
AUD_BCLK_R
MII_TXD<3..0>
MII_TXCLK
MII_TXEN
MII_RXD<3..0>
MII_RXCLK
MII_RXDV
MII_RXER/GPIO
MII_COL
MII_CRS
MII_MDIO
MII_MDC
SMB_CLK1/GPIO
SMB_DATA1/GPIO
SMB_SCL
SMB_SDA
CLK_13P5M
SB_CK_13P5M
RTC_XI
RTC_XO
V_BAT_RTC
MCP_VDD_PLL
SPKR_STRAP
SPDIF
PCI_PULLUP
LPC DEBUG
PCI_CLK_HDR
PCI_RESET*
POWER_SW
PLL_DELAY*
MCP_3P3_DELAY
DVO_FIELD
STRAP
EMPTY
IC
[PAGE_TITLE=MCPX 1 OF 2]
DRAWING
TUSCANY_FABK
Mon Mar 15 14:55:33 2004
MICROSOFT CONFIDENTIAL
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TUSCANY
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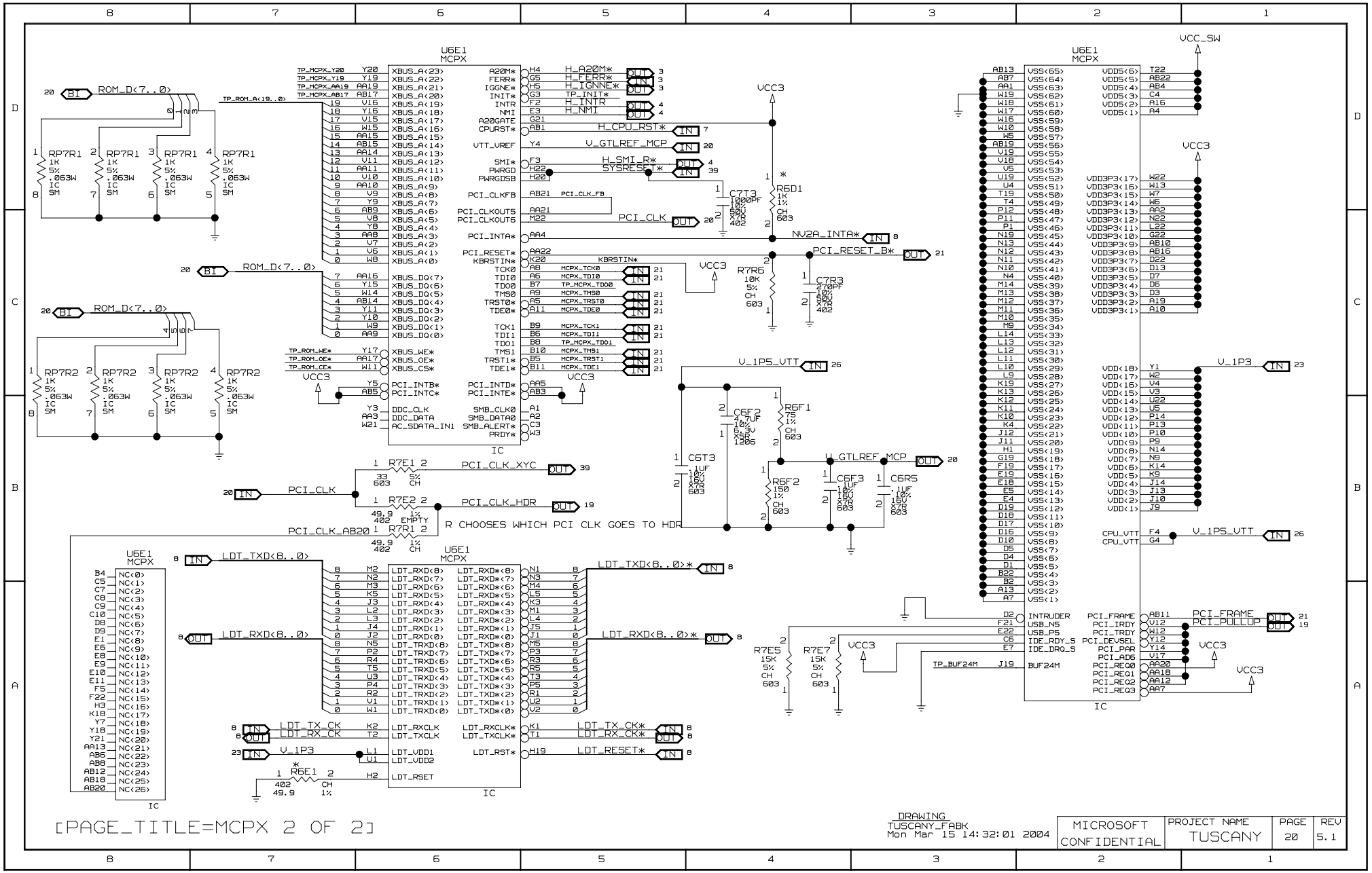
U6E1
MCPX
ROM_D<7..0>
RP7R1
RP7R2
TP_ROM_A<19..0>
XBUS_A<23>
XBUS_A<22>
XBUS_A<21>
XBUS_A<20>
XBUS_A<19>
XBUS_A<18>
XBUS_A<17>
XBUS_A<16>
XBUS_A<15>
XBUS_A<14>
XBUS_A<13>
XBUS_A<12>
XBUS_A<11>
XBUS_A<10>
XBUS_A<9>
XBUS_A<8>
XBUS_A<7>
XBUS_A<6>
XBUS_A<5>
XBUS_A<4>
XBUS_A<3>
XBUS_A<2>
XBUS_A<1>
XBUS_A<0>
XBUS_DQ<7>
XBUS_DQ<6>
XBUS_DQ<5>
XBUS_DQ<4>
XBUS_DQ<3>
XBUS_DQ<2>
XBUS_DQ<1>
XBUS_DQ<0>
XBUS_WE*
XBUS_OE*
XBUS_CS*
PCI_INTB*
PCI_INTC*
DDC_CLK
DDC_DATA
AC_SDATA_IN1
A20M*
FERR*
IGGNE*
INIT*
INTR
NMI
A20GATE
CPURST*
VTT_VREF
SMI*
PWRGD
PWRGDSB
PCI_CLKFB
PCI_CLKOUT5
PCI_CLKOUT6
PCI_INTA*
PCI_RESET*
KBRSTIN*
TCK0
TDI0
TDO0
TMS0
TRST0*
TDE0*
TCK1
TDI1
TDO1
TMS1
TRST1*
TDE1*
PCI_INTD*
PCI_INTE*
SMB_CLK0
SMB_DATA0
SMB_ALERT*
PRDY*
H_A20M*
H_FERR*
H_IGGNE*
TP_INIT*
H_INTR
H_NMI
H_CPU_RST*
V_GTLREF_MCP
H_SMI_R*
SYSRESET*
PCI_CLK
NV2A_INTA*
PCI_RESET_B*
MCPX_TCK0
MCPX_TDI0
TP_MCPX_TDO0
MCPX_TMS0
MCPX_TRST0
MCPX_TDE0
MCPX_TCK1
MCPX_TDI1
TP_MCPX_TDO1
MCPX_TMS1
MCPX_TRST1
MCPX_TDE1
PCI_CLK_XYC
PCI_CLK
PCI_CLK_HDR
PCI_CLK_AB20
R CHOOSES WHICH PCI CLK GOES TO HDR
V_1P5_VTT
V_GTLREF_MCP
LDT_TXD<8..0>
LDT_RXD<8..0>
LDT_TX_CK
LDT_RX_CK
V_1P3
LDT_RESET*
R6E1
IC
VCC_SW
VCC3
V_1P3
V_1P5_VTT
PCI_FRAME
PCI_PULLUP
INTRUDER
USB_N5
USB_P5
IDE_RDY_S
IDE_DRQ_S
BUF24M
PCI_IRDY
PCI_TRDY
PCI_DEVSEL
PCI_PAR
PCI_AD6
PCI_REQ0
PCI_REQ1
PCI_REQ2
PCI_REQ3
[PAGE_TITLE=MCPX 2 OF 2]
DRAWING
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Mon Mar 15 14:32:01 2004
MICROSOFT
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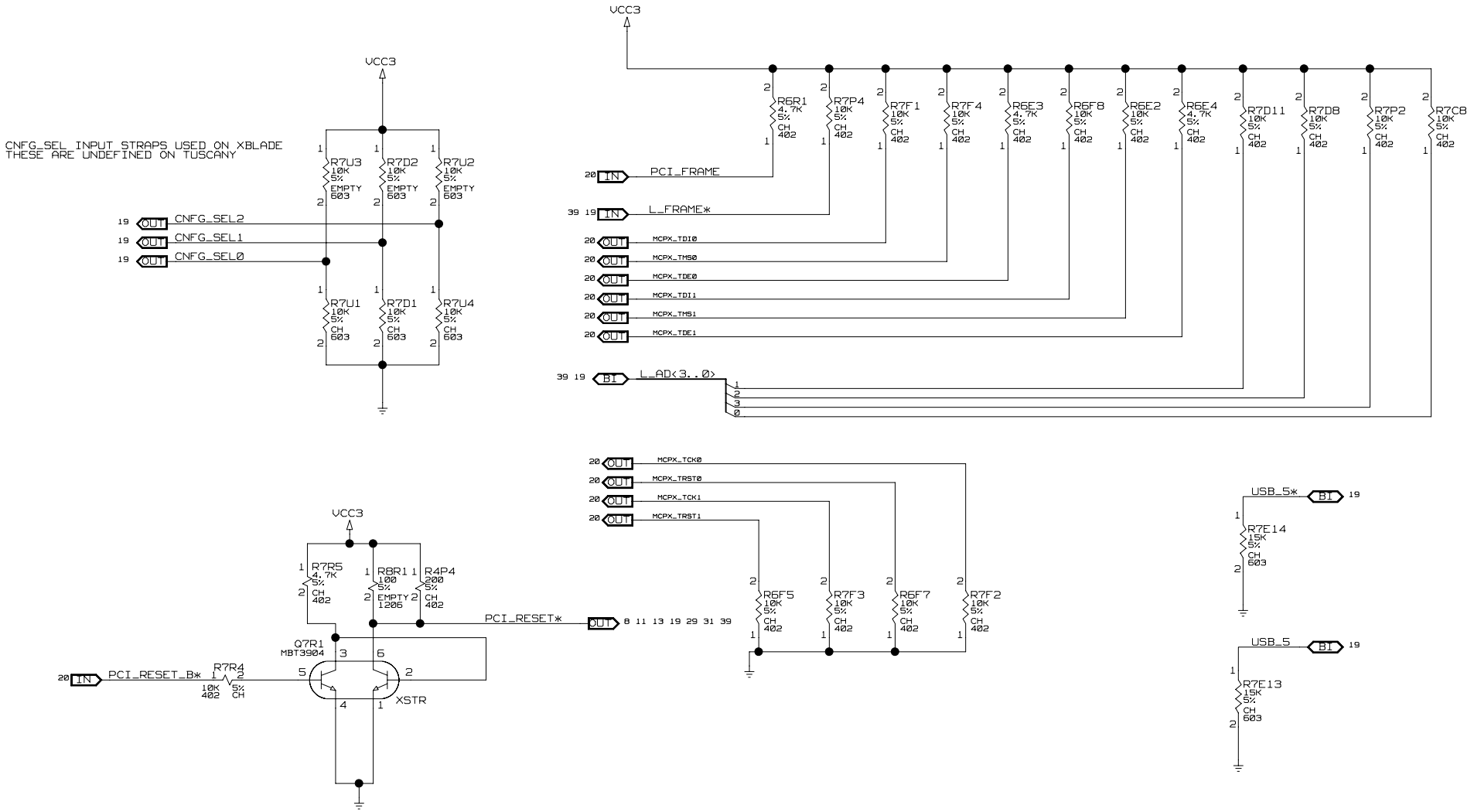

[PAGE_TITLE=MCPX INPUT STRAPS]

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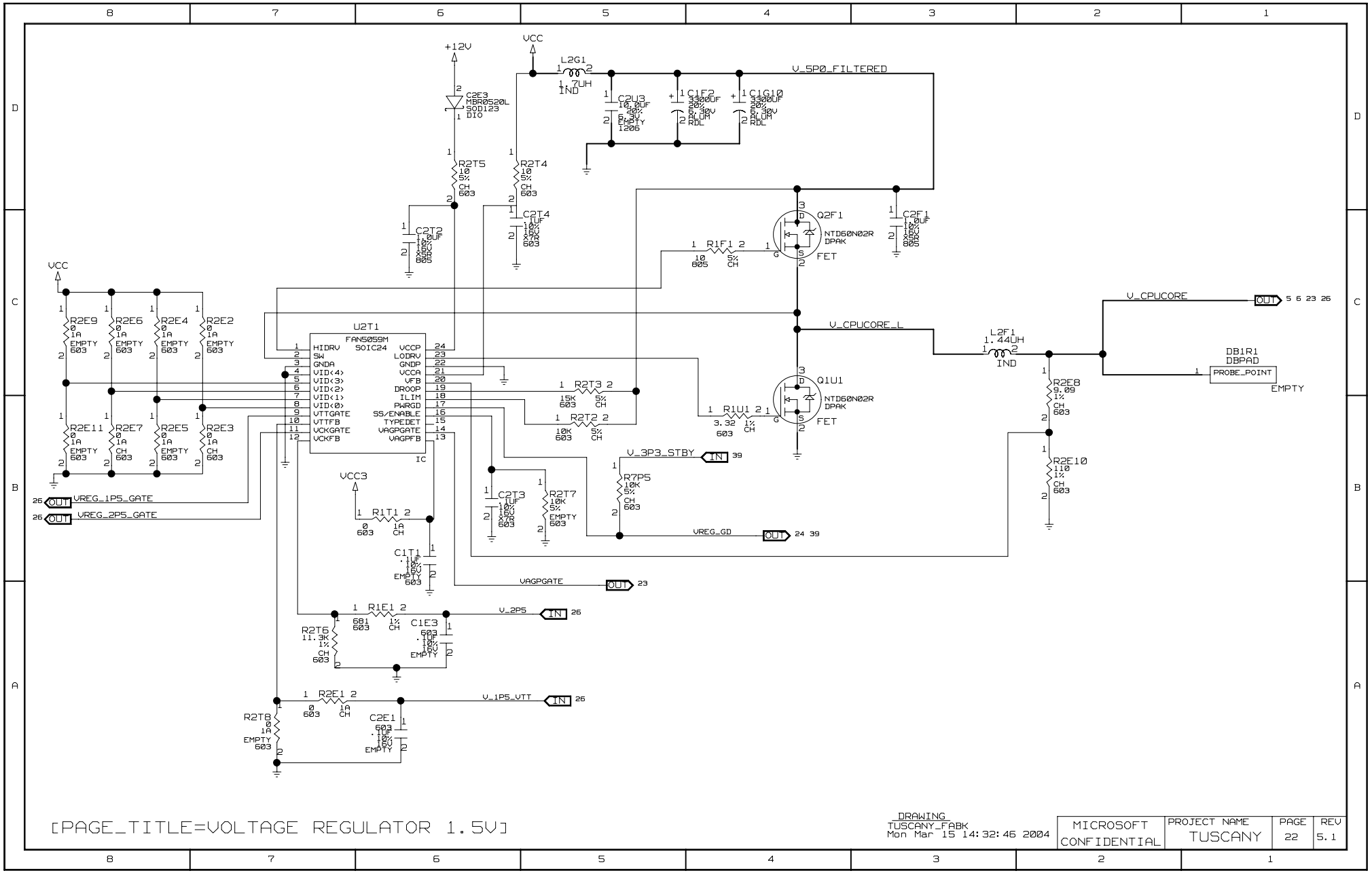
Mon Mar 15 14:32:27 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	21	5.1



[PAGE_TITLE=VOLTAGE REGULATOR 1.5V]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:32:46 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	22	5.1

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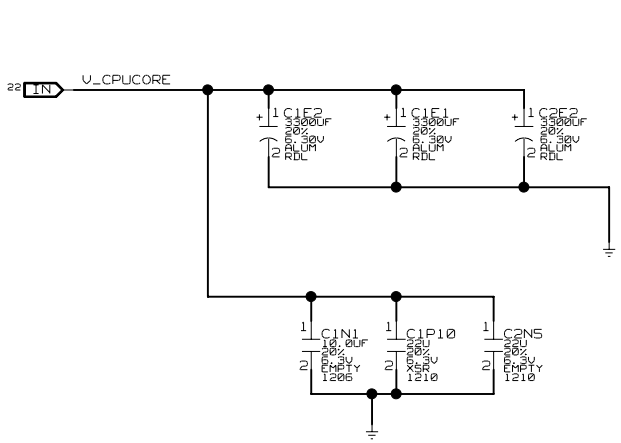

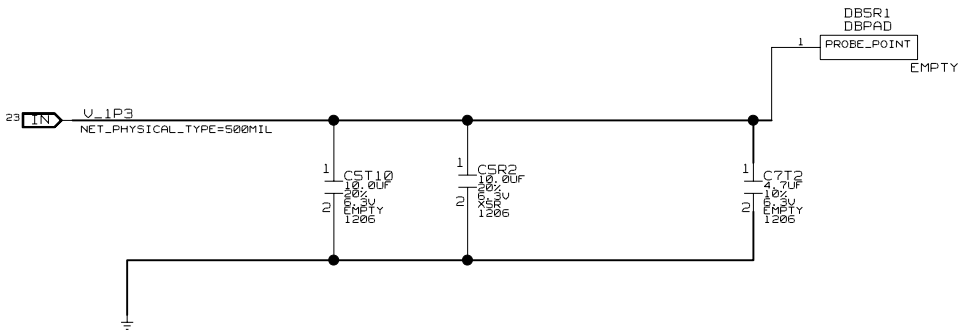

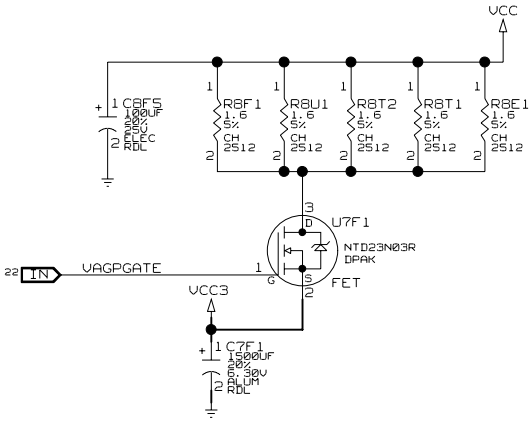

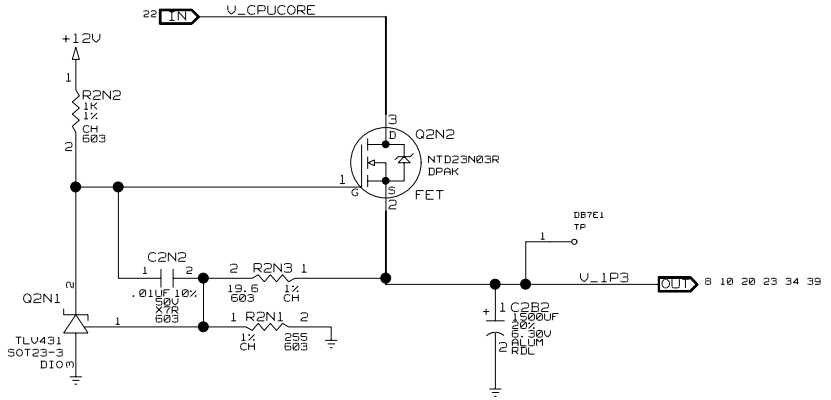

[PAGE_TITLE=1.5V OUTPUT FILTER/3.3V REGULATOR]

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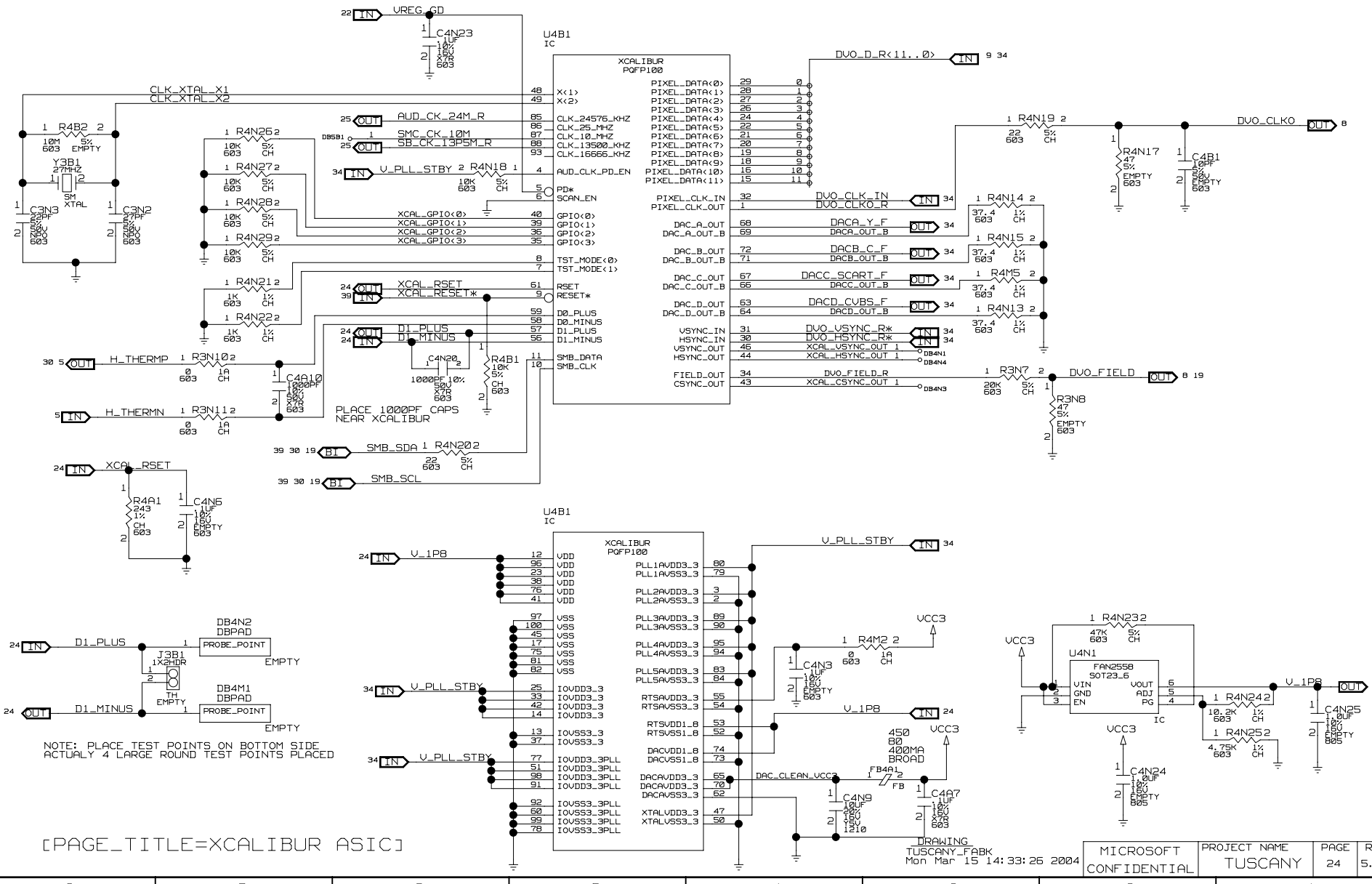
Mon Mar 15 14:33:06 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	23	5.1


U4B1
IC
XCALIBUR
PQFP100
VREG_CD
C4N23
CLK_XTAL_X1
CLK_XTAL_X2
R4B2
Y3B1
27MHZ
C3N3
C3N2
AUD_CK_24M_R
SMC_CK_10M
SB_CK_13P5M_R
V_PLL_STBY
R4N18
R4N26
R4N27
R4N28
R4N29
R4N21
R4N22
XCAL_GPIO<0>
XCAL_GPIO<1>
XCAL_GPIO<2>
XCAL_GPIO<3>
XCAL_RSET
XCAL_RESET*
D1_PLUS
D1_MINUS
C4N20
R4B1
H_THERMP
H_THERMN
R3N10
R3N11
C4A10
PLACE 1000PF CAPS
NEAR XCALIBUR
SMB_SDA
SMB_SCL
R4N20
DVO_D_R<11..0>
DVO_CLK_IN
DVO_CLKO_R
DACA_Y_F
DACA_OUT_B
DACB_C_F
DACB_OUT_B
DACC_SCART_F
DACC_OUT_B
DACD_CVBS_F
DACD_OUT_B
DVO_VSYNC_R*
DVO_HSYNC_R*
XCAL_VSYNC_OUT_1
XCAL_HSYNC_OUT_1
DVO_FIELD_R
XCAL_CSYNC_OUT_1
R4N19
R4N17
C4B1
DVO_CLKO
R4N14
R4N15
R4M5
R4N13
R3N7
R3N8
DVO_FIELD
R4A1
C4N6
V_1P8
V_PLL_STBY
DAC_CLEAN_VCC3
R4M2
C4N3
C4N9
C4A7
FB4A1
450
80
400MA
BROAD
VCC3
U4N1
FAN2558
SOT23_6
VIN
GND
EN
VOUT
ADJ
PG
R4N232
R4N242
R4N252
C4N24
C4N25
DB4N2
DBPAD
PROBE_POINT
J3B1
1X2HDR
DB4M1
DBPAD
PROBE_POINT
NOTE: PLACE TEST POINTS ON BOTTOM SIDE
ACTUALY 4 LARGE ROUND TEST POINTS PLACED
[PAGE_TITLE=XCALIBUR ASIC]
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Mon Mar 15 14:33:26 2004
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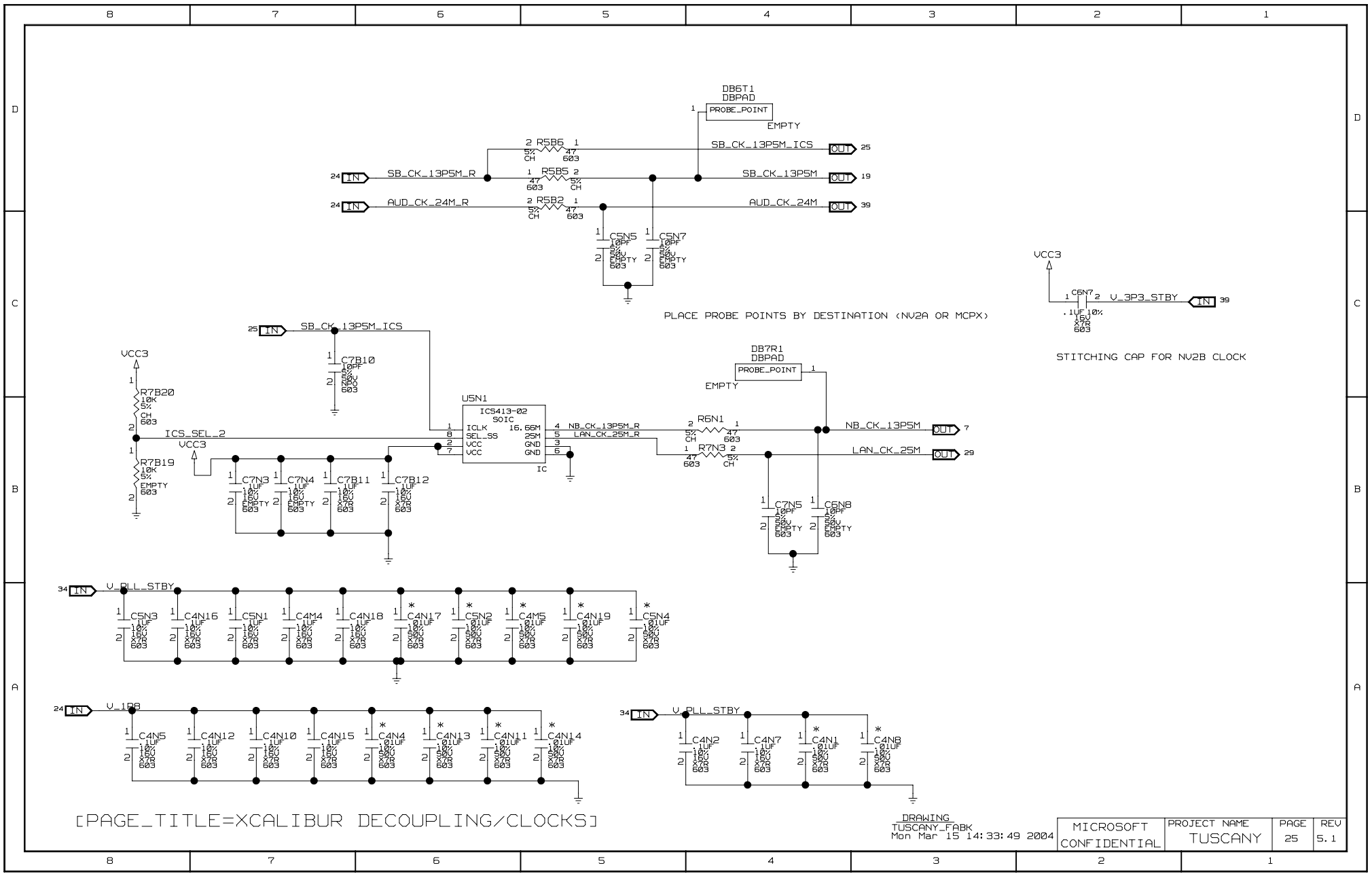
DB6T1
DBPAD
PROBE_POINT
EMPTY
SB_CK_13P5M_R
SB_CK_13P5M_ICS
SB_CK_13P5M
AUD_CK_24M_R
AUD_CK_24M
R5B6
R5B5
R5B2
C5N5
C5N7
PLACE PROBE POINTS BY DESTINATION (NV2A OR MCPX)
VCC3
C6N7
V_3P3_STBY
STITCHING CAP FOR NV2B CLOCK
SB_CK_13P5M_ICS
C7B10
R7B20
R7B19
ICS_SEL_2
U5N1
ICS413-02
SOIC
ICLK
SEL_SS
VCC
GND
16.66M
25M
NB_CK_13P5M_R
LAN_CK_25M_R
IC
DB7R1
DBPAD
PROBE_POINT
EMPTY
R6N1
R7N3
NB_CK_13P5M
LAN_CK_25M
C7N3
C7N4
C7B11
C7B12
C7N5
C6N8
V_PLL_STBY
C5N3
C4N16
C5N1
C4M4
C4N18
C4N17
C5N2
C4M5
C4N19
C5N4
V_1P8
C4N5
C4N12
C4N10
C4N15
C4N4
C4N13
C4N11
C4N14
C4N2
C4N7
C4N1
C4N8
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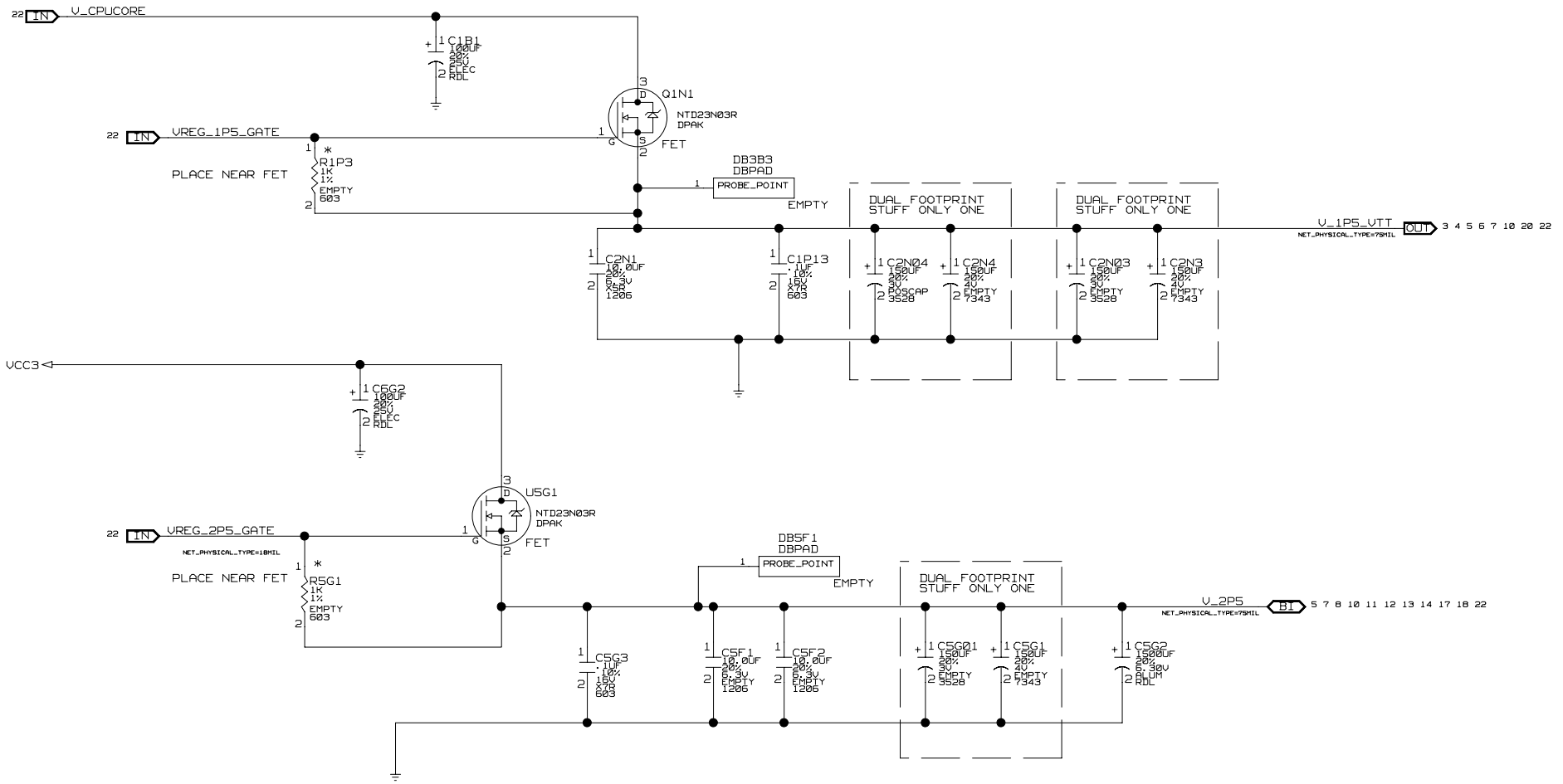

[PAGE_TITLE=1.5VTT/2.5V REGULATORS]

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TUSCANY_FABK
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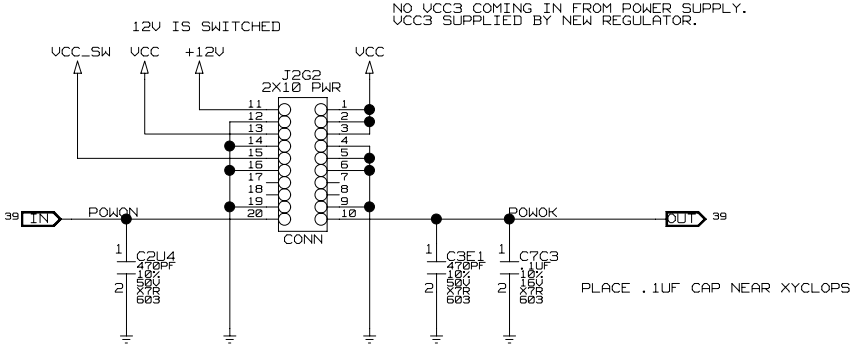
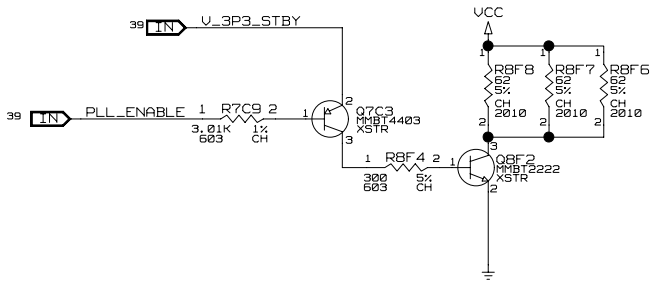
	TUSCANY	26	5.1

12V IS SWITCHED

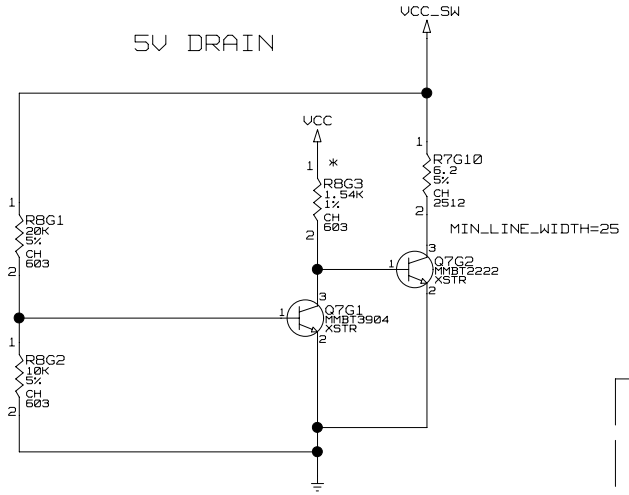
NO VCC3 COMING IN FROM POWER SUPPLY.
VCC3 SUPPLIED BY NEW REGULATOR.



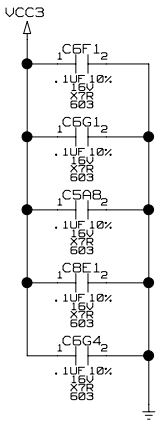
POWER SUPPLY MIN LOAD CIRCUIT



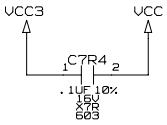
5V DRAIN



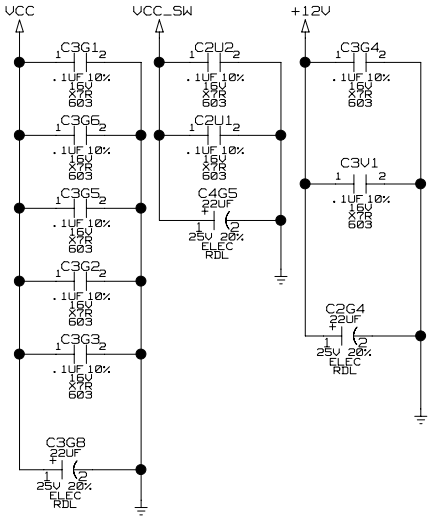
GENERAL BOARD DECOUPLING



STITCHING CAPS



POWER CONNECTOR DECOUPLING



[PAGE_TITLE=POWER CONNECTOR/5V DRAIN]

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TUSCANY_FABK
Mon Mar 15 14:34:34 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
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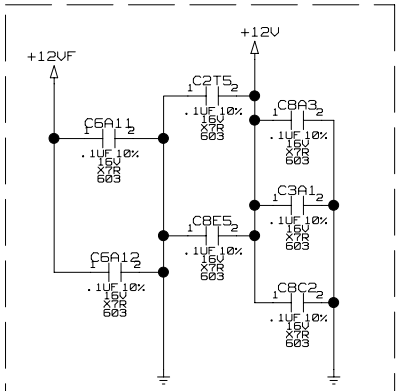

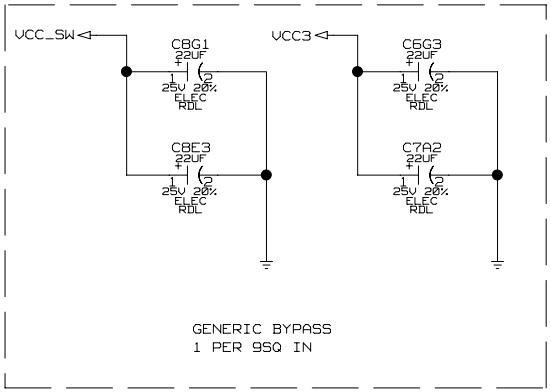

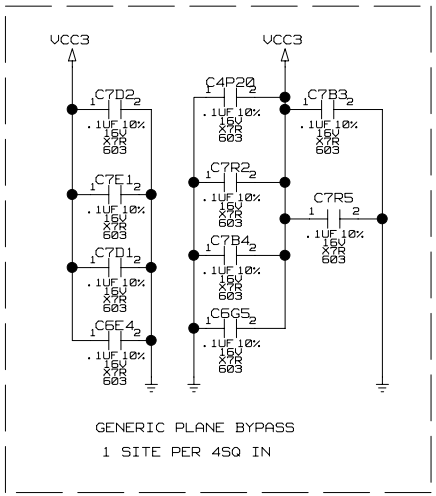

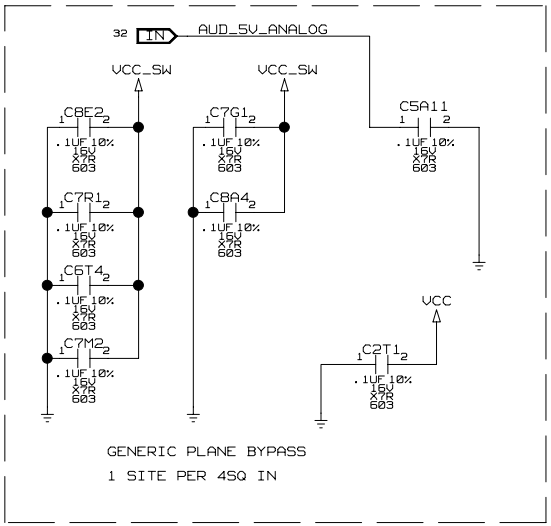

[PAGE_TITLE=BULK DECOUPLING]

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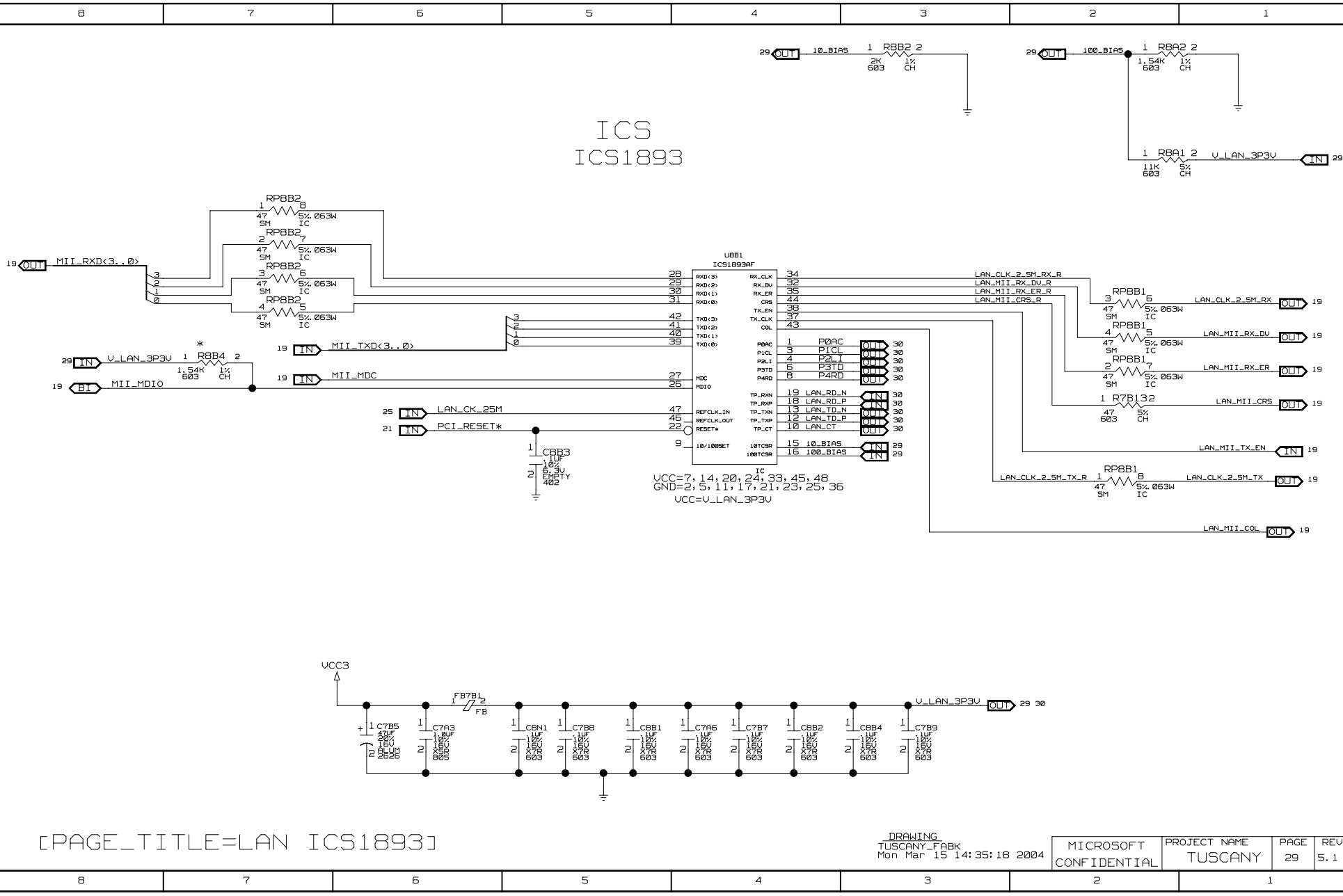
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	28	5.1


ICS
ICS1893
U8B1
ICS1893AF
10_BIAS
100_BIAS
V_LAN_3P3V
MII_RXD<3..0>
MII_TXD<3..0>
MII_MDC
MII_MDIO
LAN_CK_25M
PCI_RESET*
LAN_CLK_2_5M_RX_R
LAN_MII_RX_DV_R
LAN_MII_RX_ER_R
LAN_MII_CRS_R
LAN_CLK_2_5M_RX
LAN_MII_RX_DV
LAN_MII_RX_ER
LAN_MII_CRS
LAN_MII_TX_EN
LAN_CLK_2_5M_TX_R
LAN_CLK_2_5M_TX
LAN_MII_COL
VCC=7,14,20,24,33,45,48
GND=2,5,11,17,21,23,25,36
VCC=V_LAN_3P3V
VCC3
FB7B1
[PAGE_TITLE=LAN ICS1893]
DRAWING
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Mon Mar 15 14:35:18 2004
MICROSOFT
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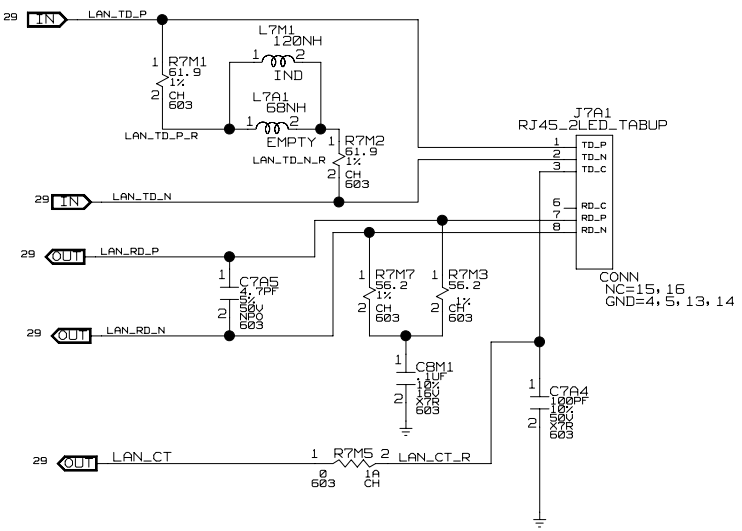
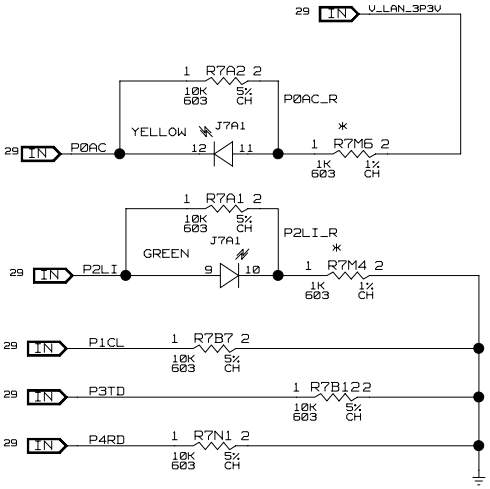
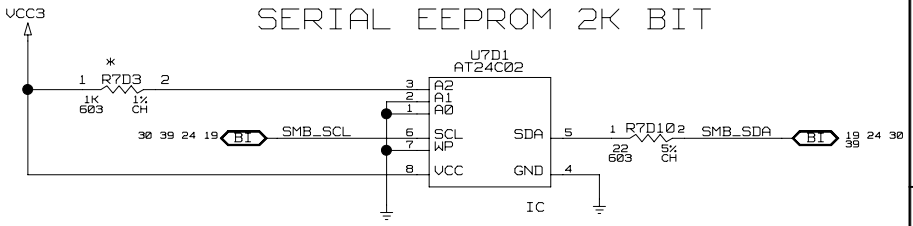
RJ45 SP JACK

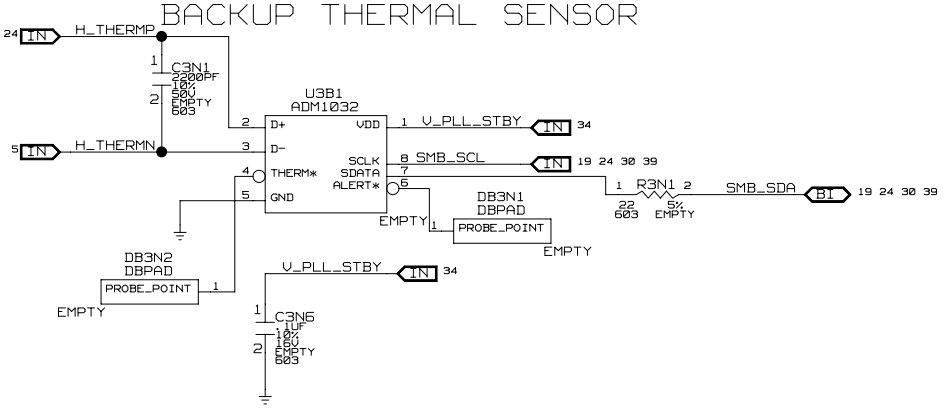




SERIAL EEPROM 2K BIT



BACKUP THERMAL SENSOR



[PAGE_TITLE=LAN JACK/EEPROM/THERMAL SENSOR]

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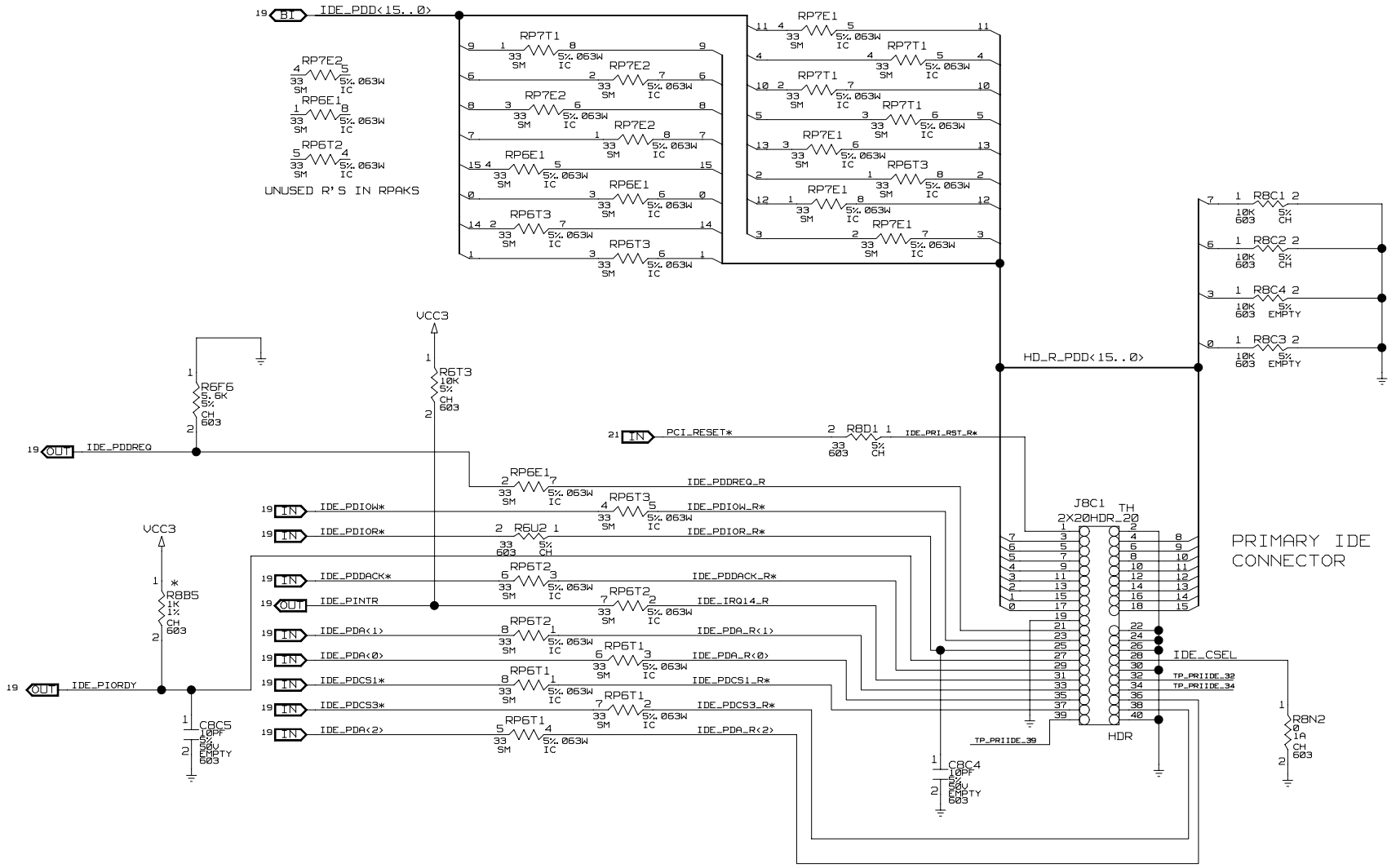
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	30	5.1


IDE_PDD<15..0>
UNUSED R'S IN RPAKS
HD_R_PDD<15..0>
PRIMARY IDE CONNECTOR
J8C1 TH 2X20HDR_20
HDR
IDE_PDDREQ
IDE_PDIOW*
IDE_PDIOR*
IDE_PDDACK*
IDE_PINTR
IDE_PDA<1>
IDE_PDA<0>
IDE_PDCS1*
IDE_PDCS3*
IDE_PDA<2>
IDE_PIORDY
PCI_RESET*
IDE_CSEL
VCC3
[PAGE_TITLE=IDE]
DRAWING
TUSCANY_FABK
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MICROSOFT CONFIDENTIAL
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TUSCANY
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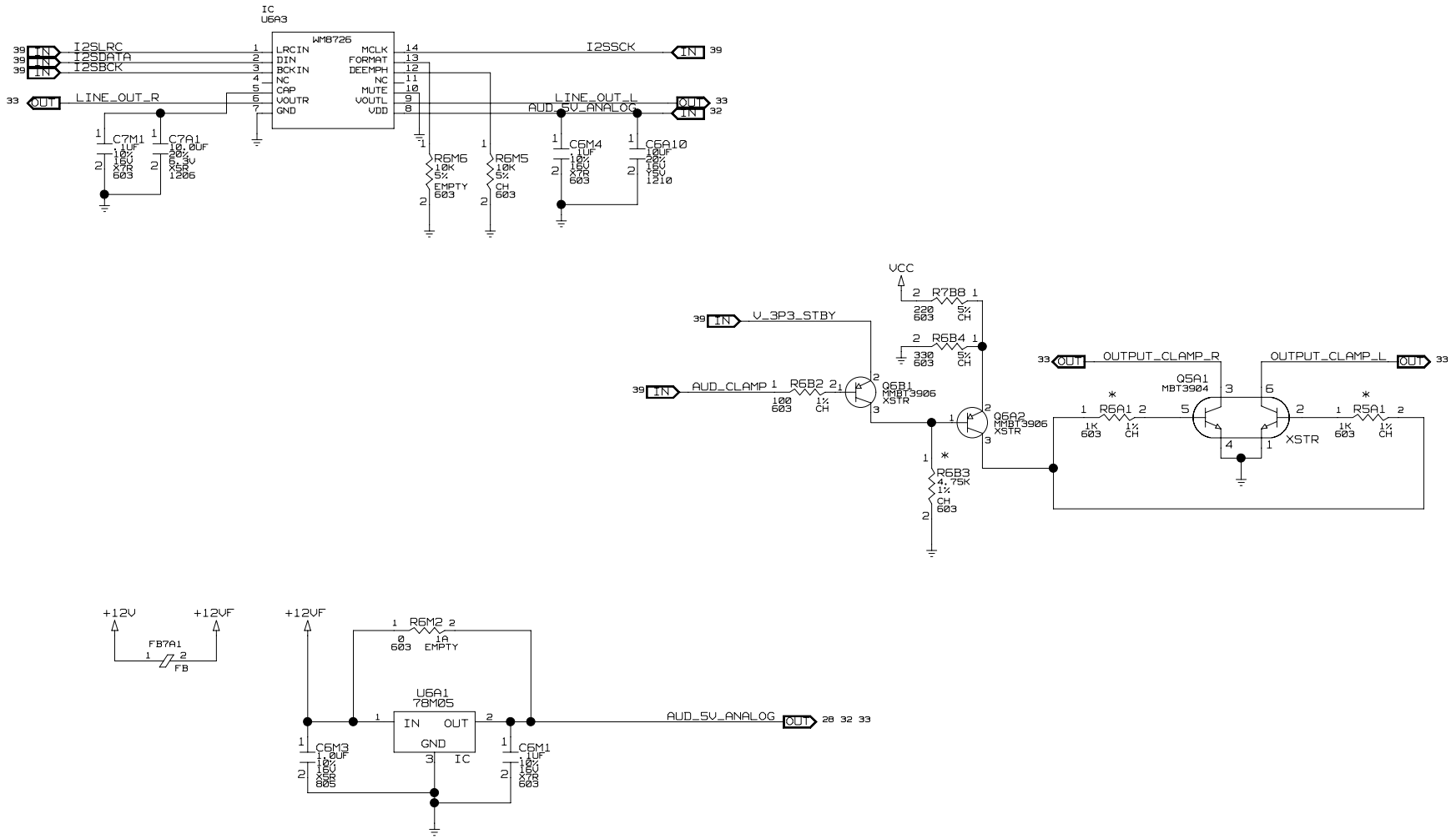
31
REV
5.1

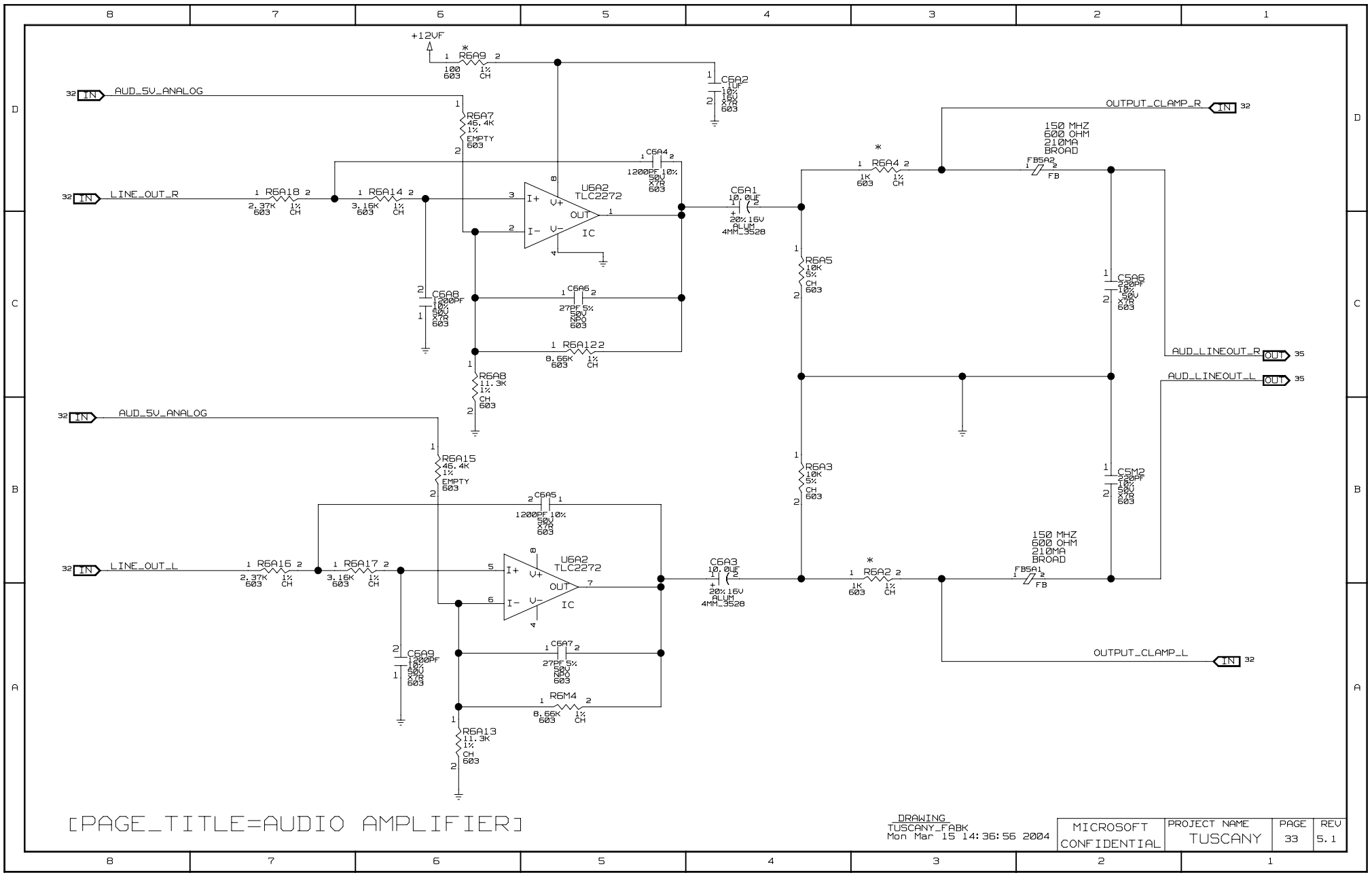


[PAGE_TITLE=AUDIO CODEC/AUDIO VREG]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:36:30 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	32	5.1

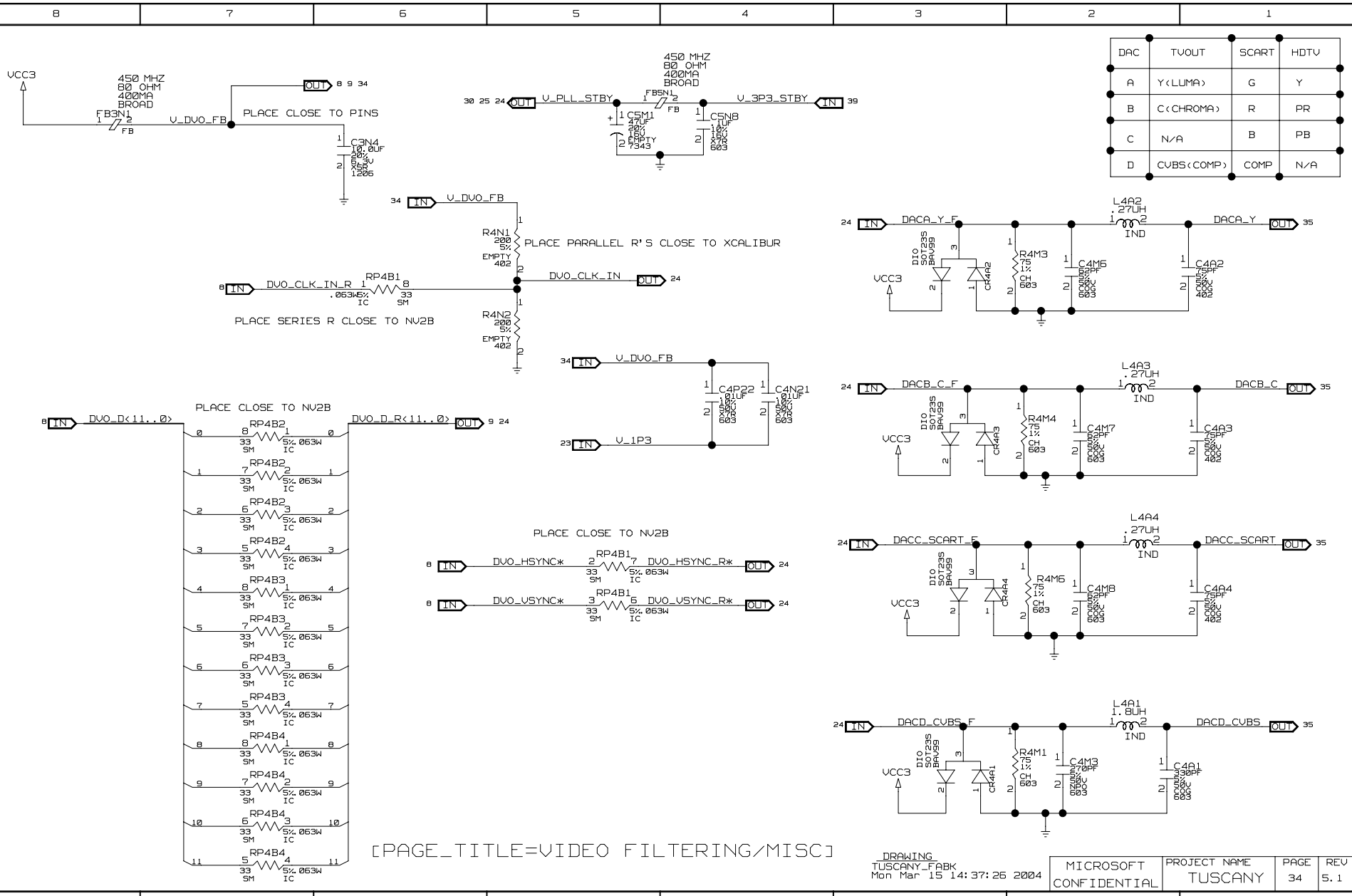
CR-33 : @TUSCANY_LIB.TUSCANY(SCH_1):PAGE33



[PAGE_TITLE=AUDIO AMPLIFIER]

DRAWING
TUSCANY_FABK
Mon Mar 15 14:36:56 2004

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	TUSCANY	33	5.1


VCC3
450 MHZ
80 OHM
400MA
BROAD
FB3N1
V_DVO_FB
OUT 8 9 34
PLACE CLOSE TO PINS
C3N4
10.0UF
20%
6.3V
X5R
1206
450 MHZ
80 OHM
400MA
BROAD
FB5N1
30 25 24 OUT V_PLL_STBY
V_3P3_STBY IN 39
C5M1
47UF
20%
16V
EMPTY
7343
C5N8
.1UF
10%
16V
X7R
603
DAC
TVOUT
SCART
HDTV
A
Y(LUMA)
G
Y
B
C(CHROMA)
R
PR
C
N/A
B
PB
D
CVBS(COMP)
COMP
N/A
34 IN V_DVO_FB
R4N1
200
5%
EMPTY
402
PLACE PARALLEL R'S CLOSE TO XCALIBUR
8 IN DVO_CLK_IN_R
RP4B1
.063W
5%
IC
33
SM
DVO_CLK_IN OUT 24
R4N2
200
5%
EMPTY
402
PLACE SERIES R CLOSE TO NV2B
34 IN V_DVO_FB
C4P22
.01UF
10%
50V
X7R
603
C4N21
.01UF
10%
50V
X7R
603
23 IN V_1P3
PLACE CLOSE TO NV2B
8 IN DVO_D<11..0>
DVO_D_R<11..0> OUT 9 24
RP4B2
RP4B3
RP4B4
PLACE CLOSE TO NV2B
8 IN DVO_HSYNC*
RP4B1
DVO_HSYNC_R* OUT 24
8 IN DVO_VSYNC*
RP4B1
DVO_VSYNC_R* OUT 24
24 IN DACA_Y_F
L4A2
.27UH
IND
DACA_Y OUT 35
DIO
SOT23S
BAV99
R4M3
75
1%
CH
603
C4M5
39PF
C4A2
75PF
24 IN DACB_C_F
L4A3
.27UH
IND
DACB_C OUT 35
R4M4
C4M7
C4A3
24 IN DACC_SCART_F
L4A4
.27UH
IND
DACC_SCART OUT 35
R4M6
C4M8
C4A4
24 IN DACD_CVBS_F
L4A1
1.8UH
IND
DACD_CVBS OUT 35
R4M1
C4M9
39PF
C4A1
[PAGE_TITLE=VIDEO FILTERING/MISC]
DRAWING
TUSCANY_FABK
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TUSCANY
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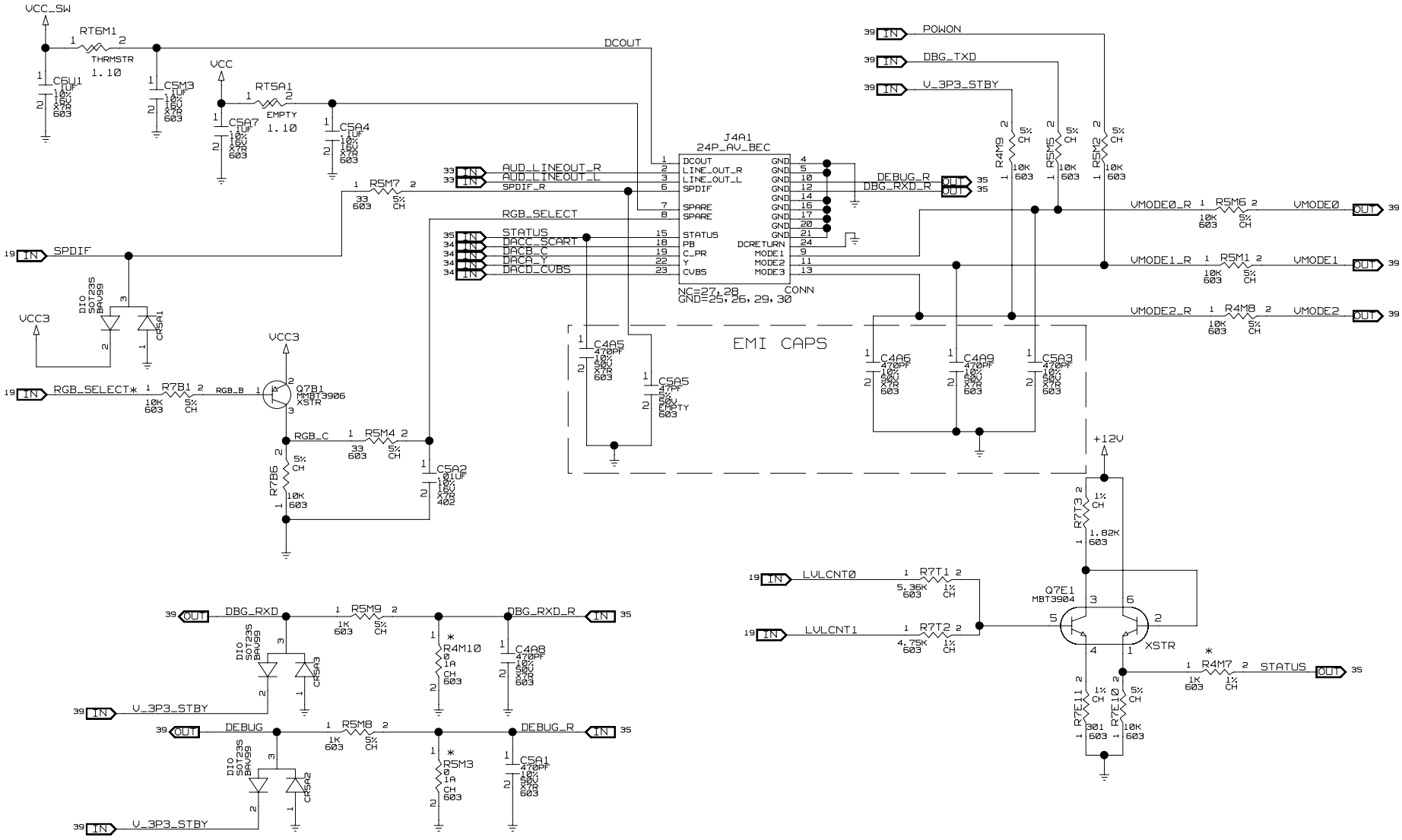
VCC_SW
RT6M1
THRMSTR
1.10
C6U1
C5M3
VCC
RT5A1
EMPTY
1.10
C5A7
C5A4
DCOUT
J4A1
24P_AV_BEC
AUD_LINEOUT_R
AUD_LINEOUT_L
SPDIF_R
RGB_SELECT
STATUS
DACC_SCART
DACB_C
DACA_Y
DACD_CVBS
R5M7
SPDIF
VCC3
DIO SOT23S BAV99
CR5A1
R7B1
Q7B1
MBT3906
XSTR
RGB_B
RGB_C
R5M4
R7B5
C5A2
EMI CAPS
C4A5
C5A5
C4A6
C4A9
C5A9
POWON
DBG_TXD
V_3P3_STBY
R4M9
R5M5
R5M2
DEBUG_R
DBG_RXD_R
VMODE0_R
VMODE1_R
VMODE2_R
R5M6
R5M1
R4M8
VMODE0
VMODE1
VMODE2
+12V
R7T3
1.82K
LVLCNT0
LVLCNT1
R7T1
5.36K
R7T2
4.75K
Q7E1
MBT3904
XSTR
R4M7
STATUS
R7E11
R7E10
DBG_RXD
R5M9
R4M10
C4A8
CR5A3
DEBUG
R5M8
R5M3
C5A1
CR5A2
[PAGE_TITLE=AV CONNECTOR]
DRAWING
TUSCANY_FABK
Mon Mar 15 14:56:01 2004
MICROSOFT CONFIDENTIAL
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TUSCANY
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5.1

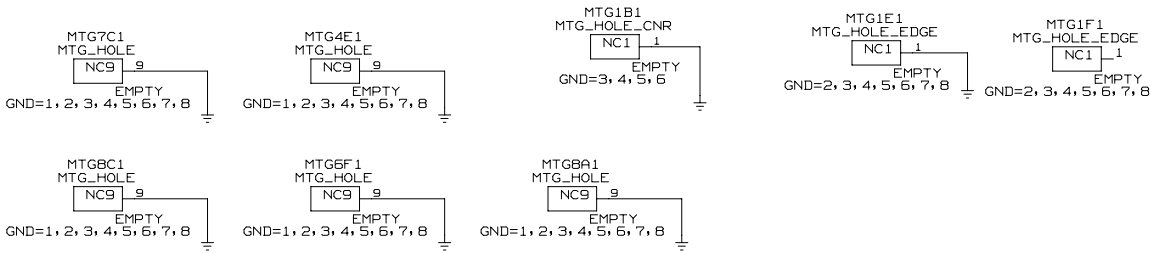
LABELS

XA19177-001
LBBD1
LABEL

1375X250_TARGET

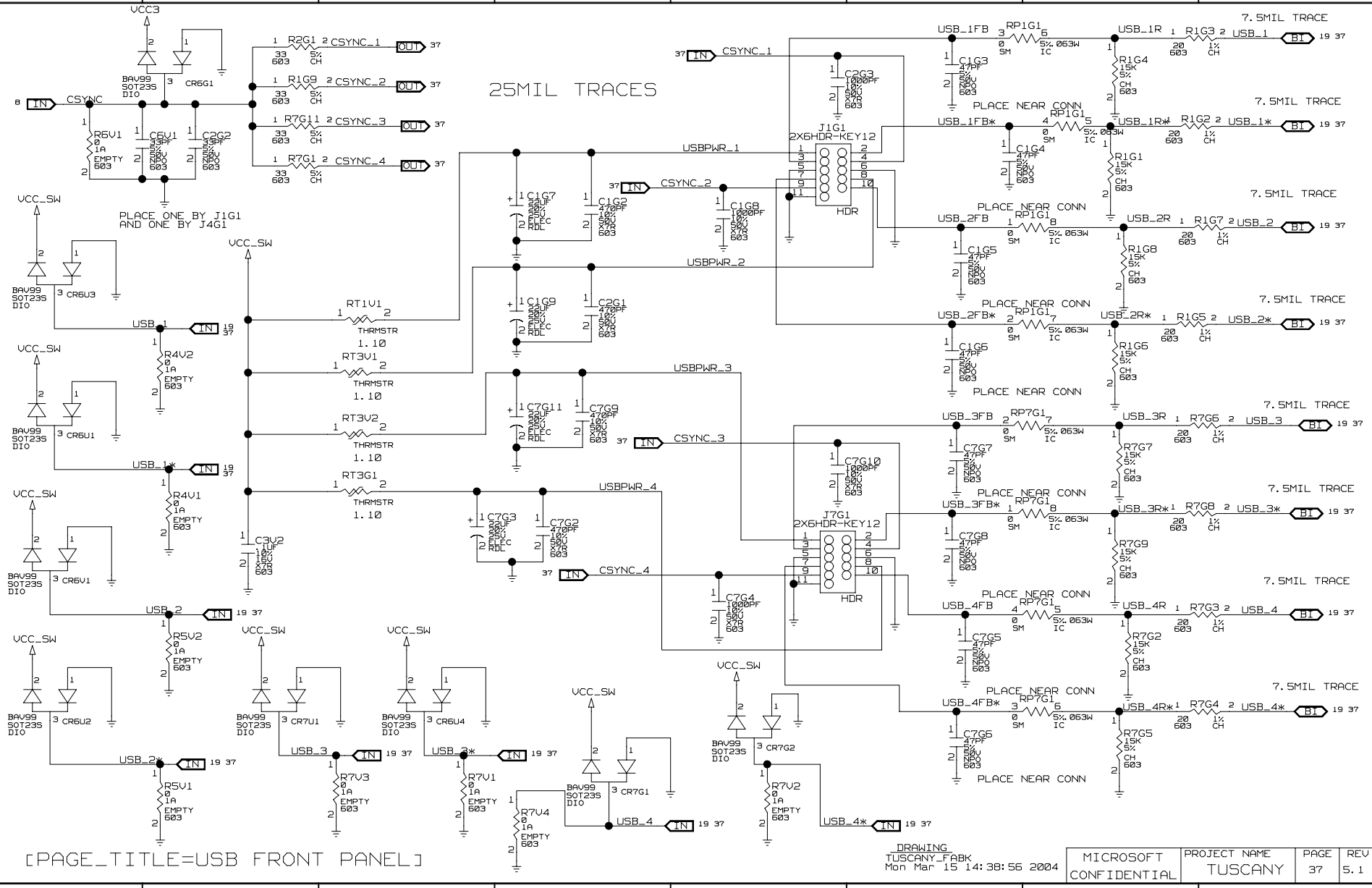
INTELLIGENT SERIAL NUMBER TARGET.

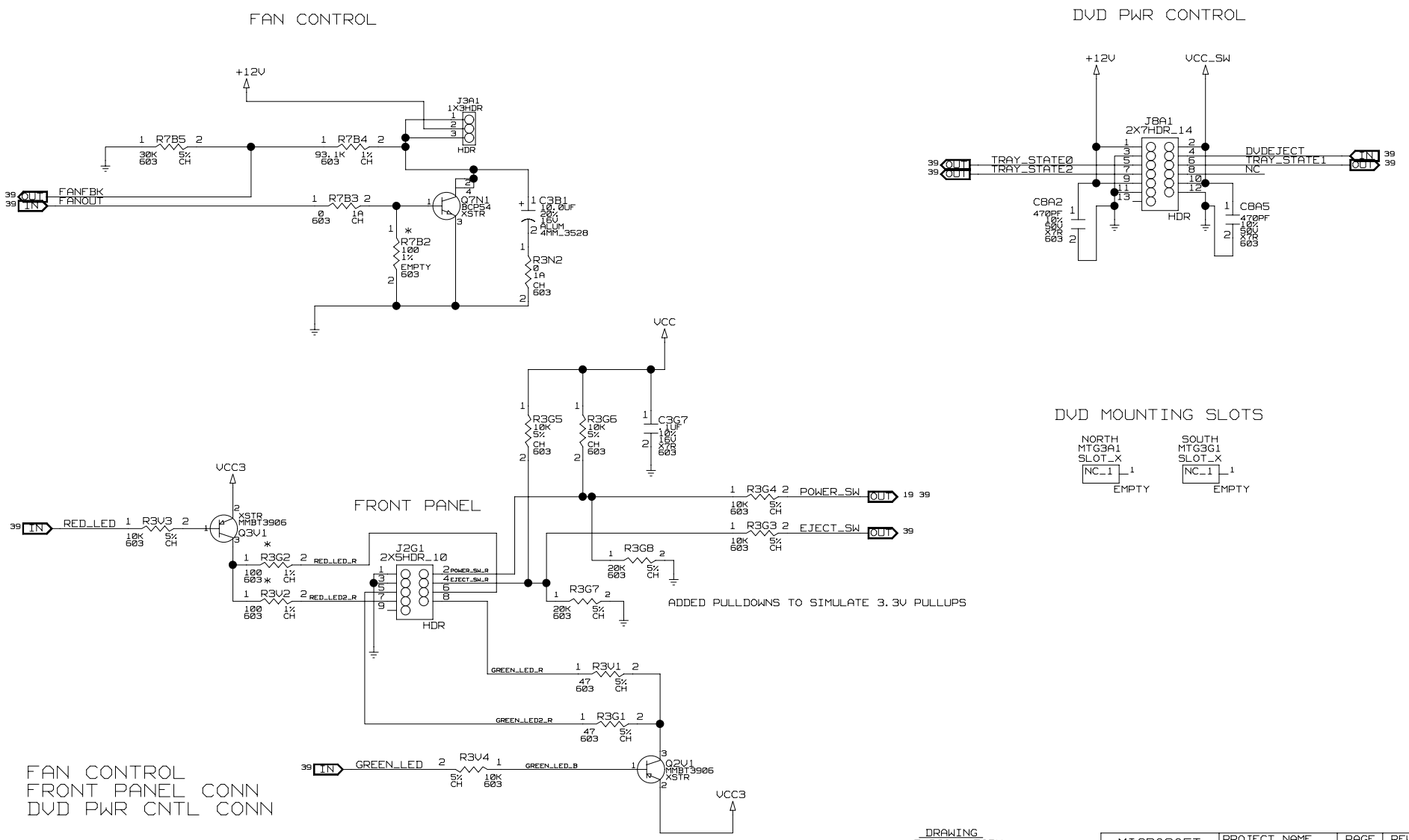
MOUNTING HOLES



[PAGE_TITLE=LABELS AND MOUNTING HOLES]

CR-37 : @TUSCANY_LIB.TUSCANY(SCH_1):PAGE37




FAN CONTROL
+12V
J3A1
1X3HDR
HDR
R7B5 2
30K
5%
CH
603
R7B4 2
93.1K
1%
CH
603
39 OUT FANFBK
39 IN FANOUT
R7B3 2
0
1A
CH
603
Q7N1
BCP54
XSTR
C3B1
10.0UF
20%
16V
ALUM
4MM_3528
R7B2
100
1%
EMPTY
603
R3N2
0
1A
CH
603
DVD PWR CONTROL
+12V
VCC_SW
J8A1
2X7HDR_14
HDR
39 OUT TRAY_STATE0
39 OUT TRAY_STATE2
DVDEJECT
TRAY_STATE1
NC
IN 39
OUT 39
C8A2
470PF
10%
50V
X7R
603
C8A5
470PF
10%
50V
X7R
603
VCC
R3G5
10K
5%
CH
603
R3G6
10K
5%
CH
603
C3G7
1UF
10%
16V
X7R
603
DVD MOUNTING SLOTS
NORTH
MTG3A1
SLOT_X
NC_1
EMPTY
SOUTH
MTG3G1
SLOT_X
NC_1
EMPTY
FRONT PANEL
VCC3
39 IN RED_LED
R3V3 2
10K
5%
CH
603
XSTR
MMBT3906
Q3V1
R3G2 2
RED_LED_R
100
1%
603
R3V2 2
RED_LED2_R
100
1%
603
J2G1
2X5HDR_10
HDR
POWER_SW_R
EJECT_SW_R
R3G4 2 POWER_SW OUT 19 39
10K
5%
603
R3G3 2 EJECT_SW OUT 39
10K
5%
603
R3G8 2
20K
5%
CH
603
R3G7 2
20K
5%
603
CH
ADDED PULLDOWNS TO SIMULATE 3.3V PULLUPS
GREEN_LED_R
R3V1 2
47
5%
603
CH
GREEN_LED2_R
R3G1 2
47
5%
603
CH
39 IN GREEN_LED
R3V4 2
5%
CH
10K
603
GREEN_LED_B
Q2V1
MMBT3906
XSTR
VCC3
FAN CONTROL
FRONT PANEL CONN
DVD PWR CNTL CONN
[PAGE_TITLE=FAN/DVD PWR/FRONT PANEL]
DRAWING
TUSCANY_FABK
Mon Mar 15 14:39:26 2004
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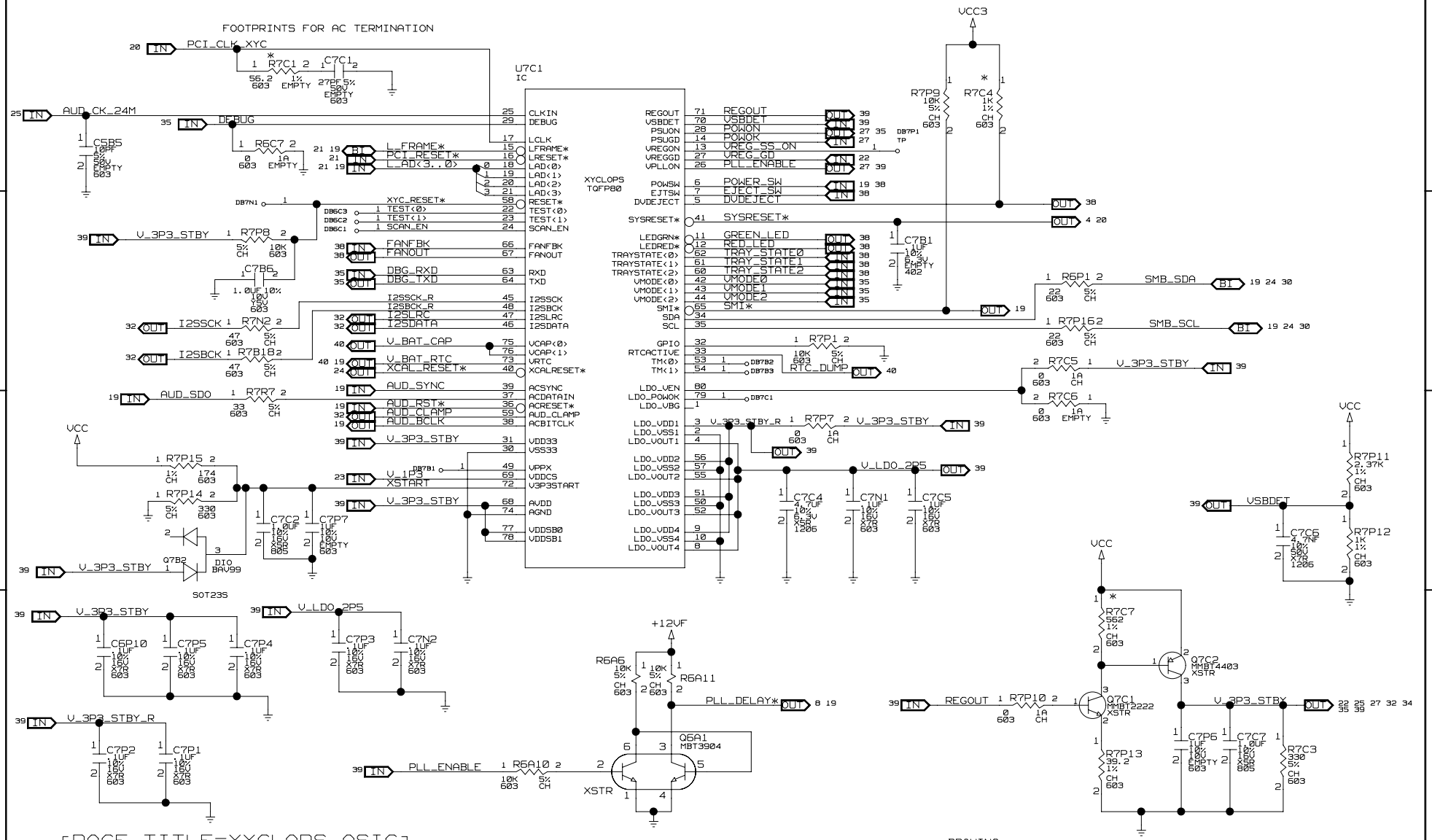
FOOTPRINTS FOR AC TERMINATION
U7C1
IC
XYCLOPS
TQFP80
PCI_CLK_XYC
AUD_CK_24M
DEBUG
L_FRAME*
PCI_RESET*
L_AD<3..0>
XYC_RESET*
V_3P3_STBY
FANFBK
FANOUT
DBG_RXD
DBG_TXD
I2SSCK
I2SBCK
I2SLRC
I2SDATA
V_BAT_CAP
V_BAT_RTC
XCAL_RESET*
AUD_SYNC
AUD_SDO
AUD_RST*
AUD_CLAMP
AUD_BCLK
V_1P3
XSTART
AVDD
AGND
VDDSB0
VDDSB1
REGOUT
VSBDET
PSUON
PSUGD
VREGON
VREGGD
VPLLON
POWSW
EJTSW
DVDEJECT
SYSRESET*
LEDGRN*
LEDRED*
TRAYSTATE<0>
TRAYSTATE<1>
TRAYSTATE<2>
VMODE<0>
VMODE<1>
VMODE<2>
SMI*
SDA
SCL
GPIO
RTCACTIVE
TM<0>
TM<1>
LDO_VEN
LDO_POWOK
LDO_VBG
LDO_VDD1
LDO_VSS1
LDO_VOUT1
LDO_VDD2
LDO_VSS2
LDO_VOUT2
LDO_VDD3
LDO_VSS3
LDO_VOUT3
LDO_VDD4
LDO_VSS4
LDO_VOUT4
V_3P3_STBY_R
V_LDO_2P5
VCC
VCC3
+12VF
SMB_SDA
SMB_SCL
RTC_DUMP
PLL_DELAY*
PLL_ENABLE
REGOUT
VSBDET
Q7B2
DIO
BAV99
SOT23S
Q6A1
MBT3904
Q7C1
MMBT2222
Q7C2
MMBT4403
XSTR
[PAGE_TITLE=XYCLOPS ASIC]
DRAWING
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TRACE WIDTH > 10MILS

39 IN V_BAT_CAP

NOTE: 2 VERSIONS OF THIS PCB EXIST.
X01053-12X HAS 2 FOOTPRINTS (5MM AND 3.5MM LEAD SPACING
5MM IS FOR TAPE-AND-REEL; 3.5MM IS FOR BULK PACKAGING
CBC1 IS 3.5MM; C8C3 IS 5MM
X01053-13X HAS 1 FOOTPRINT (3.5MM ONLY)

VOLTAGE ACROSS SUPERCAP	R7P3	R8P1
2.65V	EMPTY	0
2.5V	470	24

VCC

R7P3 470 5% CH 603

CBC1 1F 20% 5.5V ZERO RDL_RA

R7P5 22 5% CH 603

Q7F1 FET 2N7002

RTC_DUMP IN 39

R7U5 10K 5% CH 603

DB6F1 DBPAD

PROBE_POINT

EMPTY

V_BAT_RTC IN 39

C6F4 10.0UF 20% 5.5V X5R 1206

C6T2 .01UF 10% 50V X7R 603

PLACE NEAR U6E1

[PAGE_TITLE=SUPERCAP]

DRAWING
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	TUSCANY	40	5.1

*** Signal Cross-Reference for the entire design ***

10_BIAS	29D4> 29B3<
100_BIAS	29D2> 29B3<
AUD_5V_ANALOG	32A4> 28B4< 32D5< 33B8< 33D8<
AUD_BCLK	39B7> 19C8<
AUD_BCLK_R	19C7<
AUD_CK_24M	25C3> 39D8<
AUD_CK_24M_R	24D6> 25C7<
AUD_CLAMP	39B7> 32C5<
AUD_LINEOUT_L	33C1> 35D6<
AUD_LINEOUT_R	33C1> 35D6<
AUD_RST*	19C7> 39B7<
AUD_SDO	19C8> 39B8<
AUD_SYNC	19C7> 39B7<
BGA2_BREQ0_C6	4B4<>
CK_H_133M_CPU	7B5> 4A7<
CK_H_133M_CPU_BUF	4A5> 4B8<
CK_H_133M_CPU_R	4B6<
CK_H_133M_FB	7B6<>
CK_H_133M_FB_R	7B6<>
CK_H_PICCLK	7B5<>
CK_H_PICCLK_R	7B4> 4B5<
CLK_XTAL_X1	24D8<
CLK_XTAL_X2	24D8<
CNFG_SEL0	21C8> 19B4<
CNFG_SEL1	21C8> 19B4<
CNFG_SEL2	21C8> 19C4<
CSYNC	8B2> 37D8<
CSYNC_1	37D6> 37D4<
CSYNC_2	37D6> 37D5<
CSYNC_3	37D6> 37B5<
CSYNC_4	37D6> 37B5<
CTOB	35B2<
D1_MINUS	24A8> 24C6<
D1_PLUS	24C6> 24A8<
DACA_OUT_B	24C3<>
DACA_Y	34C1> 35C6<
DACA_Y_F	24C3> 34C3<
DACB_C	34C1> 35C6<
DACB_C_F	24C3> 34C3<
DACB_OUT_B	24C3<>
DACC_OUT_B	24C3<>
DACC_SCART	34B1> 35C6<
DACC_SCART_F	24C3> 34B3<
DACD_CVBS	34A1> 35C6<
DACD_CVBS_F	24C3> 34A3<
DACD_OUT_B	24C3<>
DAC_CLEAN_VCC3	24A4<
DBG_RXD	35B7> 39C7<
DBG_RXD_R	35D3> 35B5<
DBG_TXD	39C7> 35D4<
DCOUT	35D5<
DEBUG	35A7> 39D8<
DEBUG_R	35D3> 35A5<
DVDEJECT	39C2> 38D1<
DVO_CLKO	24D1> 8C2<
DVO_CLKO_R	24C3<>
DVO_CLK_IN	34C4> 24C3<
DVO_CLK_IN_R	8C2> 34C7<
DVO_D<11..0>	8C1> 34B8<
DVO_D_R<11..0>	9D7<> 34B5> 24D2<
DVO_FIELD	24C2> 8B2< 19C2<
DVO_FIELD_3P3*	19B5<
DVO_FIELD_R	24C3<>
DVO_HSYNC*	8C2> 34B6<
DVO_HSYNC_R*	34B4> 24C3<
DVO_VSYNC*	8C2> 34B6<
DVO_VSYNC_R*	34B4> 24C3<
EJECT_SW	38B3> 39C4<
EJECT_SW_R	38A6<
ETOGND	35A3<
FANFBK	38C8> 39C7<
FANOUT	39C7> 38C8<
GREEN_LED	39C4> 38A7<
GREEN_LED2_R	38A6<
GREEN_LED_B	38A5<
GREEN_LED_C	38A4<
GREEN_LED_R	38A6<
HD_R_PDD<15..0>	31C3
H_A#<31..3>	3D4<> 7D5<>
H_A20M#	20D5> 3B3<
H_A20M_R#	3B5<
H_ADS#	4C1<> 7C5<>
H_BNR#	4B5<> 7C5<>
H_BPRI#	7C5> 4B5<
H_CPU_RST#	7C5> 20D4<
H_CPU_RST_R#	7C4> 4C7<
H_D#<63..0>	3D8<> 7D8<>
H_DBSY#	4B1<> 7C5<>
H_DEFER#	7C5> 4B1<
H_DRDY#	4B1<> 7C5<>
H_FERR#	3B3> 20D5<
H_HIT#	4B1<> 7C5<>
H_HITM#	4B1<> 7B5<>
H_IGNNE#	20D5> 3B3<
H_INIT#	4C5<
H_INTR	20D5> 4B7<
H_INTR_R	4B5<
H_LOCK#	4B5<> 7B5>
H_NMI	20D5> 4B7<
H_NMI_R	4B5<
H_PREQ#	3B5<
H_REQ#<4..0>	4B5<> 7A8<>
H_RS#<2..0>	7B5<> 4B1<
H_SMI#	4A1> 4B6<
H_SMI_R#	20D4> 4A3<
H_TCK	3B5<
H_TDI	3B5<
H_THERMN	5C7> 24BB< 30B4<
H_THERMP	24C8> 5C7< 30B4<
H_TMS	3B5<
H_TRDY#	7B5<> 4B1<
H_TRST#	3B5<
I2SBCK	39C8> 32D8<
I2SBCK_R	39C6<>
I2SDATA	39C7> 32D8<
I2SLRC	39C7> 32D8<
I2SSCK	39C8> 32D5<
I2SSCK_R	39C6<>
ICS_SEL_2	25B8<
IDE_CSEL	31A2<
IDE_IRQ14_R	31B4<
IDE_PDA<0>	31A7<
IDE_PDA<2..0>	19D4>
IDE_PDA<1>	31B7<
IDE_PDA<2>	31A7<
IDE_PDA_R<0>	31A5<
IDE_PDA_R<1>	31B4<
IDE_PDA_R<2>	31A4<
IDE_PDCS1#	19D4> 31A7<
IDE_PDCS1_R#	31A5<
IDE_PDCS3#	19D4> 31A7<
IDE_PDCS3_R#	31A4<
IDE_PDD<15..0>	19D4<> 31D7<>
IDE_PDDACK#	19D4> 31B7<
IDE_PDDACK_R#	31B5<
IDE_PDDREQ	31B8> 19D4<
IDE_PDDREQ_R	31B5<
IDE_PDIOR#	19D4> 31B7<
IDE_PDIOR_R#	31B5<
IDE_PDIOW#	19D4> 31B7<
IDE_PDIOW_R#	31B5<
IDE_PINTR	31B7> 19D4<
IDE_PIORDY	31A8> 19D4<
IDE_PRI_RST_R#	31B3<
KBRSTIN#	20C5<
LAN_CK_25M	25B3> 29B6<
LAN_CK_25M_R	25B5<>
LAN_CLK_2_5M_RX	29C1> 19B7<
LAN_CLK_2_5M_RX_R	29C3<>
LAN_CLK_2_5M_TX	29B1> 19B7<
LAN_CLK_2_5M_TX_R	29B3<>
LAN_CT	29B3> 30B8>
LAN_CT_R	30B7<
LAN_MII_COL	29B1> 19B7<
LAN_MII_CRS	29B1> 19B7<
LAN_MII_CRS_R	29C3<>
LAN_MII_RX_DV	29C1> 19B7<
LAN_MII_RX_DV_R	29C3<>
LAN_MII_RX_ER	29C1> 19B7<
LAN_MII_RX_ER_R	29C3<>
LAN_MII_TX_EN	19B7> 29B1<
LAN_RD_N	30C8> 29C3<
LAN_RD_P	30C8> 29B3<
LAN_TD_N	29B3> 30C8<
LAN_TD_N_R	30D7<
LAN_TD_P	29B3> 30D8<
LAN_TD_P_R	30D8<
LDT_RESET*	8A4> 20A4<
LDT_RXD#<8..0>	20A4> 8B5<
LDT_RXD<8..0>	20A8> 8C5<
LDT_RX_CK	20A7> 8B2<
LDT_RX_CK*	20A4> 8B2<
LDT_TXD#<8..0>	8B4> 20B4<
LDT_TXD<8..0>	8C5> 20B8<
LDT_TX_CK	8B2> 20A7<
LDT_TX_CK*	8B2> 20A4<
LINE_OUT_L	32D5> 33B8<
LINE_OUT_R	32D8> 33D8<
LVLCNT	35B3<
LVLCNT0	19C4> 35B4<
LVLCNT1	19C4> 35A4<
L_AD<3..0>	19A4<> 19D7<> 21C5<> 39D7<
L_FRAME*	19D7> 39D7<> 19A4< 21C5<
L_SERIRQ	19A1> 19D8<
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MCPX_TCK1	21B5> 20C5<
MCPX_TDE0	21C5> 20C5<
MCPX_TDE1	21C5> 20C5<
MCPX_TDI0	21C5> 20C5<
MCPX_TDI1	21C5> 20C5<
MCPX_TMS0	21C5> 20C5<
MCPX_TMS1	21C5> 20C5<
MCPX_TRST0	21B5> 20C5<
MCPX_TRST1	21B5> 20C5<
MCP_3P3_DELAY	19A7<
MCP_VDD_PLL	19A5> 19B4<
MII_MDC	19B8> 29C7<
MII_MDIO	19B7<> 29C8<>
MII_RXD<3..0>	29C8> 19B7<
MII_TXD<3..0>	19B7> 19D2< 29C7<
M_AB_CKE	11A4> 12A4<
M_A_ADDR<13..0>	7D4> 11D7<
M_A_CAS*	7C4> 11B7<
M_A_CLK	7C4> 11A3<
M_A_CLK*	7C1> 11A3<
M_A_CS*<1..0>	7C5> 11B7<
M_A_DATA<31..0>	7D1<> 15D6< 15D8<
M_A_DATA_R<31..0>	11D7<> 15D4> 15D6>
M_A_DQM<3..0>	7D4> 15B6<
M_A_DQM_R<3..0>	15B4> 11C7<
M_A_DQS	7C4<> 15B3<
M_A_DQS_R	11A4<> 15C3<
M_A_RAS*	7C4> 11B7<
M_A_WE*	7C4> 11B7<
M_B_ADDR<13..0>	7B4> 12D7<
M_B_CAS*	7A4> 12B7<
M_B_CLK	7A4> 12A4<
M_B_CLK*	7A1> 12A4<
M_B_CS*<1..0>	7A5> 12B8<
M_B_DATA<31..0>	7B1<> 15C6< 15D3<
M_B_DATA_R<31..0>	12D7<> 15C4> 15D1>
M_B_DQM<3..0>	7B4> 15A6<
M_B_DQM_R<3..0>	15A4> 12C7<
M_B_DQS	7A4<> 15A3<
M_B_DQS_R	12A4<> 15A3<
M_B_RAS*	7A4> 12B7<
M_B_WE*	7A4> 12B7<
M_CD_CKE	13A4> 14A4<
M_C_ADDR<13..0>	8D8> 13D7<
M_C_CAS*	8C7> 13B7<
M_C_CLK	8C7> 13A4<
M_C_CLK*	8B5> 13A4<
M_C_CS*<1..0>	8C8> 13B7<
M_C_DATA<31..0>	8D5<> 16D6< 16D8<
M_C_DATA_R<31..0>	13D7<> 16D4> 16D6>
M_C_DQM<3..0>	8C8> 16B6<
M_C_DQM_R<3..0>	16B4> 13C7<
M_C_DQS	8C7<> 16B4<
M_C_DQS_R	13A4<> 16B4<
M_C_RAS*	8C7> 13B7<
M_C_WE*	8C7> 13B7<
M_D_ADDR<13..0>	8B8> 14D7<
M_D_CAS*	8A7> 14B7<
M_D_CLK	8A7> 14A3<
M_D_CLK*	8A5> 14A3<
M_D_CS*<1..0>	8A8> 14B8<
M_D_DATA<31..0>	8B4<> 16C6< 16D3<
M_D_DATA_R<31..0>	14D7<> 16C4> 16D1>
M_D_DQM<3..0>	8A8>
M_D_DQM<31..0>	16A6<
M_D_DQM_R<3..0>	16A4> 14C7<
M_D_DQS	8A7<> 16A4<
M_D_DQS_R	14A4<> 16A4<
M_D_RAS*	8A7> 14B7<
M_D_WE*	8A7> 14B7<
M_VREF_0	11A3> 11B7< 12A7<
M_VREF_1	13A4> 13B8< 14A7<
NB_CK_13P5M	25B3> 7B5<
NB_CK_13P5M_R	25B5<
NV2A_3P3_DELAY	8A2<
NV2A_INTA*	8B2> 20C3<
NV2A_TEST	8B2<>
NV2A_VREF_0	7C2<>
NV2A_VREF_1	8C6<>
OUTPUT_CLAMP_L	32C1> 33A1<
OUTPUT_CLAMP_R	32C3> 33D1<
P0AC	29C3> 30B8<
P0AC_R	30B7<
P1CL	29C3> 30A8<
P2LI	29C3> 30A8<
P2LI_R	30A7<
P3TD	29C3> 30A8<
P4RD	29C3> 30A8<
PCI_CLK	20C4> 20B7<
PCI_CLK_AB20	20B7<
PCI_CLK_FB	20D5<
PCI_CLK_HDR	20B5> 19A4<
PCI_CLK_XYC	20B5> 39D8<
PCI_FRAME	20A1> 21D5<
PCI_PULLUP	19A3> 20A1>
PCI_RESET*	21A5> 8B1< 11A7< 13A7< 19A5< 29B6< 31B5< 39D7<
PCI_RESET_B*	20C3> 21AB<
PICD0	4B7<>
PICD1	4B8<>
PLLVDD	8A2<>
PLL_C2B	39A5<
PLL_DELAY*	39A4> 8A4< 19A8<
PLL_ENABLE	39D4> 27D4< 39A7<
PLL_G2	39A5<
POWER_SW	19A1> 38B3> 39C4<
POWER_SW_R	38B6<
POWOK	27C5> 39D4<
POWON	39D4> 27C8< 35D4<
RED_LED	39C4> 38B8<
RED_LED2_R	38A7<
RED_LED_B	38B7<
RED_LED_C	38A8<
RED_LED_R	38B7<
REGOUT	39D4> 39A3<
RGB_B	35C7<
RGB_C	35B7<
RGB_SELECT	35C6<
RGB_SELECT*	19C4> 35C8<
ROM_D<7..0>	20C7<> 20C8<> 20D8<>
RSET_NV2A*	8A4<>

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RTC_DUMP          39C4> 40C2<
RTC_XI            19B2> 19B4<
RTC_XO            19B2> 19B4<
SB_CK_13P5M       25D3> 19B2<
SB_CK_13P5M_ICS   25D3> 25C7<
SB_CK_13P5M_R     24D6> 25D7<
SCAN_EN           39C6<
SMB_SCL           19A4<> 19B2<> 24B7<> 30D3<> 39C1<>
                  30B2<
SMB_SDA           19A1<> 19B2<> 24B7<> 30B1<> 30D1<>
                  39C1<>
SMC_CK_10M        24D6<>
SMI*              39C3> 19C4<
SPDIF             19B3> 35C8<
SPDIF_R           35D6<
SPKR_STRAP        19B5<
STATUS            35A1> 35C6<
SYSRESET*         39C2> 4C7< 20D4<
SYSRESET_R*       4C6<
TEST<0>           39C6<
TEST<1>           39C6<
TP_BGA2_A4        3C5<>
TP_BGA2_A5        3C5<>
TP_BGA2_AA1       4C3<>
TP_BGA2_AA17      5C7<>
TP_BGA2_AA21      3B5<>
TP_BGA2_AB1       4C3<>
TP_BGA2_AB19      5B7<>
TP_BGA2_AC17      5B7<
TP_BGA2_AD9       3B5>
TP_BGA2_AD20      5C7<>
TP_BGA2_B4        3C5<>
TP_BGA2_C5        3C5<
TP_BGA2_E6        3C5<>
TP_BGA2_G4        5C7<>
TP_BGA2_H4        5C7<>
TP_BGA2_P20       4B3<>
TP_BGA2_P21       4B3<>
TP_BGA2_R2        5B7<>
TP_BGA2_R21       4B3<>
TP_BGA2_T21       4B3<>
TP_BGA2_U19       4B3<>
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TP_BGA2_V18       4B3<>
TP_BGA2_V20       4B3<>
TP_BGA2_V21       3C5<>
TP_BGA2_W2        4C3<>
TP_BGA2_W19       3B5<>
TP_BGA2_W21       3B5<>
TP_BGA2_Y1        4B3<
TP_BGA2_Y2        4C3<>
TP_BGA2_Y21       3B5<>
TP_BUF24M         20A3<
TP_CPURSV0        7B6<>
TP_CPURSV1        7B6<>
TP_DEBUG_GPIO15   19C4<
TP_INIT*          20D5<
TP_MCPX_AA19      20D7<
TP_MCPX_AB17      20D7<
TP_MCPX_H21       19C4<
TP_MCPX_TDO0      20C5<
TP_MCPX_TDO1      20C5<
TP_MCPX_Y2        19B5<
TP_MCPX_Y19       20D7<
TP_MCPX_Y20       20D7<
TP_PRIIDE_32      31A2<
TP_PRIIDE_34      31A2<
TP_PRIIDE_39      31A3<
TP_ROM_A<19..0>   20D7<
TP_ROM_CE*        20C7<
TP_ROM_OE*        20C7<
TP_ROM_WE*        20C7<
TRAY_STATE0       38C3> 39C4<
TRAY_STATE1       38C1> 39C4<
TRAY_STATE2       38C3> 39C4<
USBPWR_1          37D4<
USBPWR_2          37C4<
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USBPWR_4          37B5<
USB_1             19D7> 37D1<> 37C7<
USB_1*            19D7> 37D1<> 37B7<
USB_1FB           37D3<
USB_1FB*          37D3<
USB_1R            37D2<
USB_1R*           37D2<
USB_2             19D7> 37C1<> 37A7<
USB_2*            19D7> 37C1<> 37A7<
USB_2FB           37C3<
USB_2FB*          37C3<
USB_2R            37C2<
USB_2R*           37C2<
USB_3             19D7> 37B1<> 37A5<
USB_3*            19D7> 37B1<> 37A5<
USB_3FB           37B3<
USB_3FB*          37B3<
USB_3R            37B2<
USB_3R*           37B2<
USB_4             19C7> 37A1<> 37A4<
USB_4*            19C7> 37A1<> 37A3<
USB_4FB           37A3<
USB_4FB*          37A3<
USB_4R            37A2<
USB_4R*           37A2<
USB_5             19C7> 21A1<>
USB_5*            19C7> 21B1<>
USB_VREF          19C7<
VAGPGATE          22B5> 23B8<
VMODE0            35C1> 39C4<
VMODE0_R          35C2<>
VMODE1            35C1> 39C4<
VMODE1_R          35C2<>
VMODE2            35C1> 39C4<
VMODE2_R          35C2<>
VREG_1P5_GATE     22B8> 26D8<
VREG_2P5_GATE     22B8> 26B8<
VREG_GD           22B4> 24D6< 39D4<
VREG_SS_ON        39D4<>
VSBDET            39B2> 39D4<
V_1P3             23A1> 8B2< 10B8< 10D8< 20A7< 20C1<
                  23D5< 34B5< 39B7<
V_1P5_VTT         26C1> 3B1< 3C3< 4D8< 5B6< 5D1<
                  5D4< 5D8< 6D4< 7A5< 7C5< 10D2< 20B1<
                  20C4< 22A5<
V_1P8             24A1> 24A3< 24B6< 25A8<
V_2P5             26B2<> 5B7< 7A4< 7A4< 7B4< 7C2<
                  7C4< 8A7< 8C7< 8D4< 10D5< 11A6<
                  11B2< 11B7< 12A7< 13A6< 13B2< 13B7<
                  14A7< 17B2< 17B6< 17B6< 17D3< 17D6<
                  17D8< 18C6< 18D1< 18D2< 18D6< 18D7<
                  22A5<
V_3P3_STBY        39A1> 22B4< 25C1< 27D3< 32C5<
                  34D3< 35A8< 35A8< 35D4< 39A8< 39B3<
                  39B7< 39B7< 39B8< 39C2< 39C8<
V_3P3_STBY_R      39B4> 39A8<
V_5P0_FILTERED    22D3<
V_BAT_CAP         39C7> 40D8<
V_BAT_RTC         39C7> 19B4< 40C2<
V_CLKREF          5A5> 5D8<
V_CPUCORE         22C1> 5C4< 6D6< 6D8< 23B4< 23D8<
                  26D8<
V_CPUCORE_L       22C4<
V_DVO_FB          34D6> 8C1< 9C8< 34C5< 34D6<
V_DVO_REF         8B2<>
V_GTLREF          5B4> 5B5< 5D8<
V_GTLREF_1P0      7A4> 7B5<
V_GTLREF_MCP      20B3> 20D4<
V_LAN_3P3V        29A2> 29C8< 29D1< 30B7<
V_LDO_2P5         39B3> 39A7<
V_PLL_STBY        34D5> 24A6< 24A6< 24B3< 24D6<
                  25A5< 25A8< 30A3< 30B2<
XCAL_CSYNC_OUT    24C3<>
XCAL_GPIO<0>      24C6<
XCAL_GPIO<1>      24C6<
XCAL_GPIO<2>      24C6<
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XCAL_GPIO<3>      24C6<
XCAL_HSYNC_OUT    24C3<>
XCAL_RESET*       39C7> 24C6<
XCAL_RSET         24C6> 24B8<
XCAL_VSYNC_OUT    24C3<>
XSTART            39B6<
XYC_RESET*        39C6<
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*** Part Cross-Reference for the entire design ***

C1B1	CAP_P	26
C1C1	CAPN	5
C1D1	CAPN	4
C1D2	CAPN	4
C1D3	CAPN	10
C1D4	CAPN	5
C1D5	CAPN	5
C1E1	CAP_P	23
C1E2	CAP_P	23
C1E3	CAPN	22
C1F2	CAP_P	22
C1G2	CAPN	37
C1G3	CAPN	37
C1G4	CAPN	37
C1G5	CAPN	37
C1G6	CAPN	37
C1G7	CAP_P	37
C1G8	CAPN	37
C1G9	CAP_P	37
C1G10	CAP_P	22
C1N1	CAPN	23
C1P1	CAPN	6
C1P2	CAPN	6
C1P3	CAPN	6
C1P4	CAPN	6
C1P5	CAPN	6
C1P6	CAPN	5
C1P7	CAPN	6
C1P8	CAPN	6
C1P9	CAPN	6
C1P10	CAPN	23
C1P11	CAPN	6
C1P12	CAPN	5
C1P13	CAPN	26
C1R1	CAPN	6
C1R2	CAPN	6
C1R3	CAPN	6
C1R4	CAPN	6
C1R5	CAPN	5
C1R6	CAPN	5
C1R7	CAPN	4
C1T1	CAPN	22
C2B2	CAP_P	23
C2E1	CAPN	22
C2E2	CAP_P	23
C2E3	MBR0520L	22
C2F1	CAPN	22
C2G1	CAPN	37
C2G2	CAPN	37
C2G3	CAPN	37
C2G4	CAP_P	27
C2N1	CAPN	26
C2N2	CAPN	23
C2N03	CAP_P	26
C2N3	CAP_P	26
C2N04	CAP_P	26
C2N4	CAP_P	26
C2N5	CAPN	23
C2P1	CAPN	6
C2P2	CAPN	6
C2P3	CAPN	6
C2P4	CAPN	6
C2P5	CAPN	6
C2P6	CAPN	6
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C2P21	CAPN	6
C2P22	CAPN	6
C2P23	CAPN	6
C2R1	CAPN	6
C2R2	CAPN	6
C2R3	CAPN	5
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C2R5	CAPN	6
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C2R8	CAPN	7
C2T1	CAPN	28
C2T2	CAPN	22
C2T3	CAPN	22
C2T4	CAPN	22
C2T5	CAPN	28
C2U1	CAPN	27
C2U2	CAPN	27
C2U3	CAPN	22
C2U4	CAPN	27
C3A1	CAPN	28
C3B1	CAP_P	38
C3B4	CAPN	10
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C3D2	CAPN	4
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C3E3	CAPN	18
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C3G2	CAPN	27
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C5C1	CAPN	18
C5C2	CAPN	18
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C5F7	CAPN	13
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C5G1	CAP_P	26
C5G2	CAP_P	26
C5G3	CAPN	26
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C5M2	CAPN	33
C5M3	CAPN	35
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RP6B1 RPAK4C_4R 15
RP6B2 RPAK4C_4R 15
RP6B3 RPAK4C_4R 15
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RP6C1 RPAK4C_4R 15
RP6C2 RPAK4C_4R 15
RP6C3 RPAK4C_4R 15
RP6E1 RPAK4C_4R 31
RP6P1 RPAK4C_4R 15
RP6P2 RPAK4C_4R 15
RP6P3 RPAK4C_4R 15
RP6P4 RPAK4C_4R 15
RP6R1 RPAK4C_4R 15
RP6R2 RPAK4C_4R 15
RP6R3 RPAK4C_4R 15
RP6R4 RPAK4C_4R 15
RP6T1 RPAK4C_4R 31
RP6T2 RPAK4C_4R 31
RP6T3 RPAK4C_4R 31
RP7E1 RPAK4C_4R 31
RP7E2 RPAK4C_4R 31
RP7G1 RPAK4C_4R 37
RP7R1 RPAK4C_4R 20
RP7R2 RPAK4C_4R 20
RP7T1 RPAK4C_4R 31
RP8B1 RPAK4C_4R 29
RP8B2 RPAK4C_4R 29
RT1V1 THERMISTOR 37
RT3G1 THERMISTOR 37
RT3V1 THERMISTOR 37
RT3V2 THERMISTOR 37
RT5A1 THERMISTOR 35
RT6M1 THERMISTOR 35
U2C1  PBGA2_495 3 4 5
U2T1  FAN5059M  22
U3B1  ADM1032   30
U3R1  CY2305    4
U3T1  DDR_SDRAM4MX32 14
U4B1  XCALIBUR  24
U4C1  NV2B      7 8
U4N1  FAN2558   24
U5F1  DDR_SDRAM4MX32 13
U5G1  FET_VREG  26
U5N1  ICS413_02 25
U6A1  78M05     32
U6A2  TLC2272   33
U6A3  WMB726    32
U6D1  DDR_SDRAM4MX32 12
U6E1  MCPX_2    19 20
U6N1  DDR_SDRAM4MX32 11
U7C1  XYCLOPS   39
U7D1  AT24C02   30
U7F1  FET_VREG  23
UBB1  ICS1893AF 29
Y3B1  CRYSTAL   24
Y6F1  XTAL4P    19
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