MSM5205

ADPCM SPEECH SYNTHESIS LSI

TO CUSTOMERS FOR NEW CIRCUIT DESIGN

For a new circuit design, it is recommended to use the MSM6585 as described later. The MSM5205 has a 10-bit DA converter and does not have a built-in low-pass filter. On the other hand, the MSM6585 has a 12-bit DA converter and includes a -40dB/oct low-pass filter. The sampling frequency can also be selected up to 32kHz. Therefore, the MSM6585 can realize a high quality voice.

GENERAL DESCRIPTION

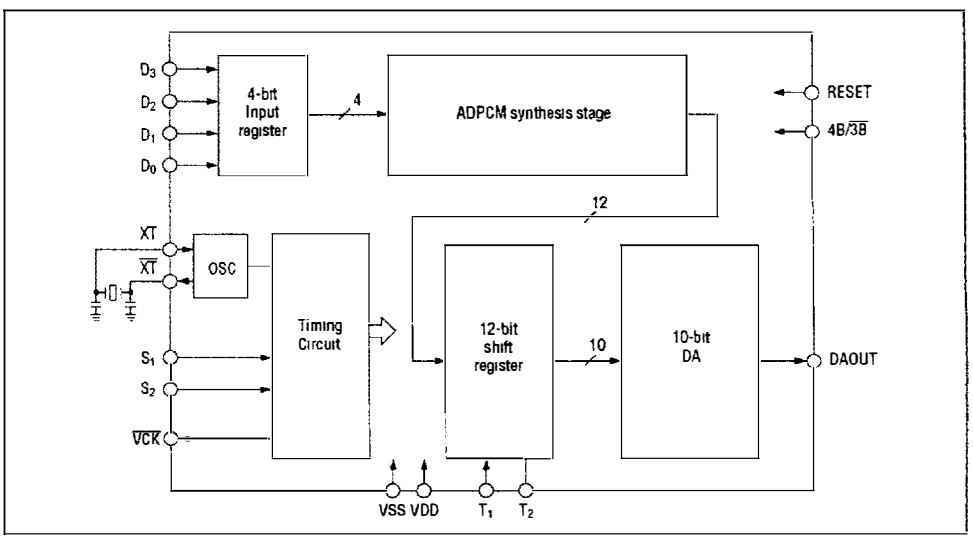
The MSM5205 is a speech synthesis integrated circuit which accepts Adaptive Differential Pulse Code Modulation (ADPCM) data. The circuit consists of synthesis stage which expands the 3- or 4-bit ADPCM data to 12-bit Pulse Code Modulation (PCM) data and a D/A stage which reproduces analog signals from the PCM data.

The MSM5205 is fabricated using Oki's advanced CMOS process which enables low-power consumption. The single power supply requirement and its availability in 18-pin molded DIP allow the MSM5205 to be ideally suited for various applications.

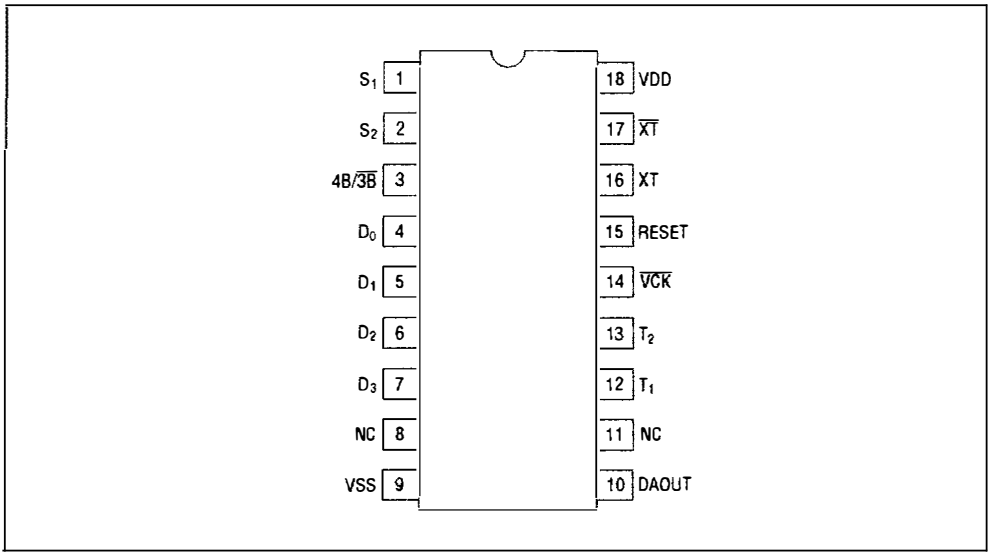
FEATURES

- 3 or 4-bit ADPCM system
- On-chip 10-bit D/A converter
- Low power consumption (10 mW typical)
- Single +5V supply
- Wide operating temperature (Ta = -30°C ~ +70°C)
- 18-pin Plastic DIP (DIP 18-P-300)

BLOCK DIAGRAM



PIN CINFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	T_a = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ VDD	V
Power dissipation	P_D	T_a = 25°C	200 max	mW
Storage temperature	T_{stg}	–	−55 ~ + 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	–	+3 ~ +6	V
Operating temperature	Top	–	−30 ~ +70	°C
Oscillator Frequency	f_{OSC}	Specified Oscillator	384 ~ 768	kHz

D.C./A.C. CHARACTERISTICS

(VDD = 5V±5%; Ta = –30°C ~ +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except T_1, T_2	4.2	–	VDD+0.3	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	V_{SS}–0.3	–	0.8	V
Input High Current	I_{IH}	V_{IN} = VDD	–	–	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V	–	–	–1	µA
Output High Current	I_{OH}	$\overline{VCK}$ pin: V_O = 4.2V	–50	–	–	µA
Output Low Current	I_{OL}	$\overline{VCK}$ pin: V_O = 0.4V	+50	–	–	µA
Operating Current	I_{DD}	f_{osc} = 384 kHz VDD = 5V	–	2	4	mA
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale; VDD = 5V	–	±4	–	LSB
DAOUT Output Impedance	V_{OR}	–	–	100	–	kΩ

PIN DESCRIPTION

Pin Name	Terminal Number	I/O
S_1	1	I
S_2	2	I
These inputs select the sampling data according to Figure 1.		
$4B/\overline{3B}$	3	I
Specifies whether 3-bit or 4-bit ADPCM data is to be processed. "H" level input is 4-bit (ADPCM). "L" level input is 3-bit (ADPCM).		
D_0	4	I
D_1	5	I
D_2	6	I
D_3	7	I
ADPCM data inputs. For 3-bit ADPCM data, D_0 input is not used and should be connected to ground.		
VSS	9	—
Ground (0 V)		
DAOUT	10	O
Output for synthesized analog signal. Peak-to-peak swing is proportional to VDD. Typical method of connection is shown Figure 2		
T_1	12	I
T_2	13	I
IC test pins used at the factory for testing purposes only. During normal operations, T_1 is grounded and T_2 is left open.		
$\overline{VCK}$	14	O
This pin outputs a signal whose frequency is equal to the sampling frequency selected by the S_1, S_2 inputs. See the figure1.		

PIN DESCRIPTION (continued)

Pin Name	Terminal Number	I/O
RESET	15	I

An active high input which initializes the internal circuitry. Internally, the reset pulse is synchronized with the $\overline{VCK}$ signal. To be effective, it must be true for at least twice $\overline{VCK}$ time.

XT	16	I
$\overline{XT}$	17	O

Oscillator input and output for a crystal or ceramic resonator (Figure 3).

VDD	18	—

Power supply pin (Typical +5V)

S1	S2	Sampling Frequency (f_{OSC}=384kHz)
L	L	4 kHz (f_{OSC}/96)
L	H	6 kHz (f_{OSC}/64)
H	L	8 kHz (f_{OSC}/48)
H	H	Prohibited See Note *1

Note: *1 A 384kHz oscillator can be used to select 4kHz, 6kHz or 8kHz. A 768kHz oscillator can be used to select 8kHz, 12kHz or 16kHz.

Figure 1

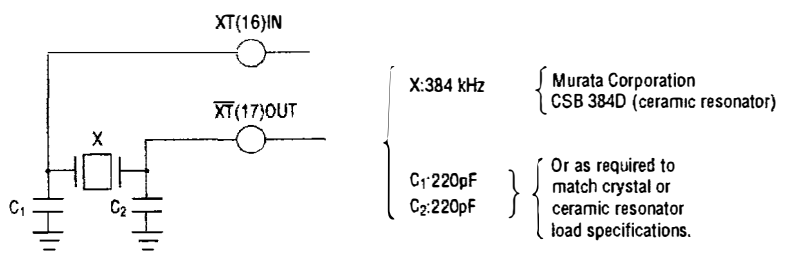
Cut off frequency (f_{CUT}) of LPF should be related to the selected sampling frequency (f sample) by,

$$(f_{CUT}) = f\ sample/2 \times 0.85$$

Sound quality is strongly dependent on the characteristic of the low pass filter.

* If the MSM5205 is sent a stream of ADPCM data that causes greater than full scale output, the D/A output will wrap around: from the most positive rail (+5V) to the most negative rail (0.0V)

Figure 2



XT and $\overline{XT}$ (Oscillator connector pins)

Figure 3

DA converter SN ratio improvement method

The accuracy near center of the voice waveform of this LSI may be worse due to the configuration of the DA converter. Therefore, the SN ratio can be improved by shifting the waveform center up or down. This is an extremely effective method for improving the SN ratio of a small signal or improving residual noise during silence (between 2 speech patterns.)

To put it concretely, by adding data before or after the current ADPCM data (voice data), the waveform center can be shifted as shown in Figure 4.

Adding data is as follows:

(A) section	(B) section	
0 0 0 0	1 0 0 0	
0 0 0 0	1 0 0 0	100 data
⋮	⋮	

(The ADPCM bit length is 4-bit.)

Since an offset of about 5 mV can be obtained for each 2 samples of data, it is recommended that about 100 samples of data be entered to shift the waveform center about 250 mV.

For 3-bit data, an offset of about 5 mV can be obtained for each data. Therefore, about 50 samples of data is required to be entered to shift the waveform center about 250 mV.

In the (A) section, the waveform center should be shifted up. In the (B) section, the waveform center should be shifted down. The number of data in the (A) section should be the same as that in the (B) section.

When (A) is added before voice data and (B) is added after the voice data, the output waveform is as shown in Figure 4.

Since the dynamic range is narrowed by the shifted area, some data may overflow, causing the voice to be distorted.

If this occurs, decrease the sound level about 20% and analyze the data once again. (For an overflow, see the precautions for ADPCM data creation on the next page.)

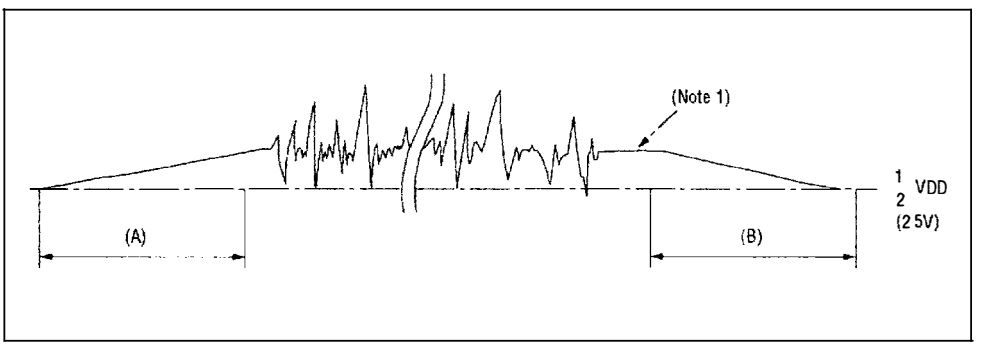


Figure 4 Waveform the DA Converter

Note 2: Voice data should be sufficiently small just prior to (B). For voice editing, insert a silence of about 10msec.

Precaution for ADPCM data creation

When voice is synthesized by the MSM5205 using ADPCM data analyzed by the MSM5218, noise may be generated in the synthesized voice.

The MSM5205 is not equipped with an overflow protection unit in the internal operation circuit even though the MSM5218 is. Therefore, although the MSM5218 produces normal voice, the MSM5205 may cause noise in the composite voice due to an overflow in the data. If this occurs, analyze and create the ADPCM data once again.

An example of a waveform when an overflow occurs and the overflow protection method is as follows :

(1) Waveform when an overflow occcurs

The observation of the output waveform from the DA converter of the MSM5205 on an oscilloscope shows that an overflowed waveform is looped as shown in Figure 5.

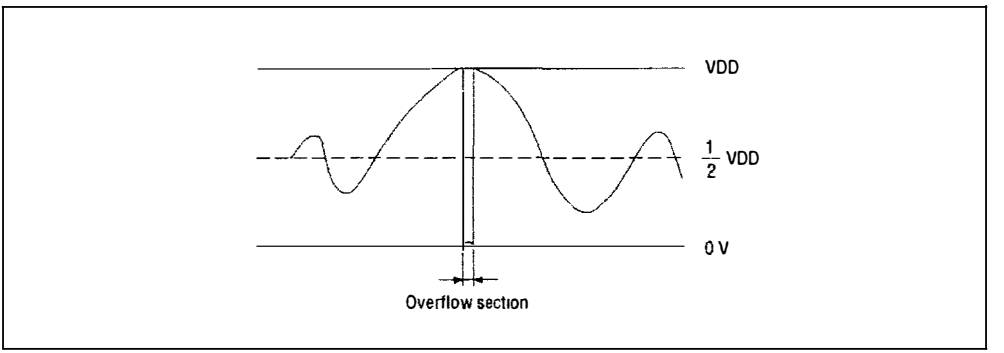


Figure 5 Output Waveform When an Overflow Occurs

(2) Overflow protection method

Even if an input waveform is not beyond the dynamic range when the ADPCM data is analyzed by the MSM5218, the output waveform may overflow due to an internal operation error.

Therefore, if the maximum amplitude level of the input waveform when the ADPCM data is analyzed by the MSM5218, is controlled to about 80% of the dynamic range or less (see Figure 6), the output waveform of the MSM5205 will not overflow, causing no noise in the composite voice.

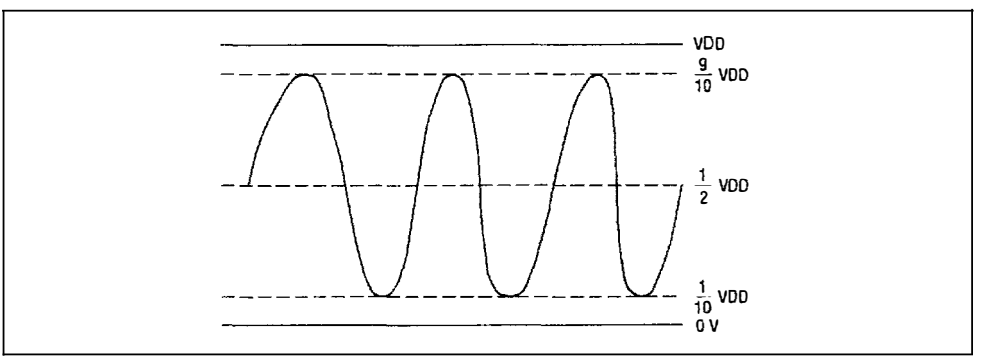
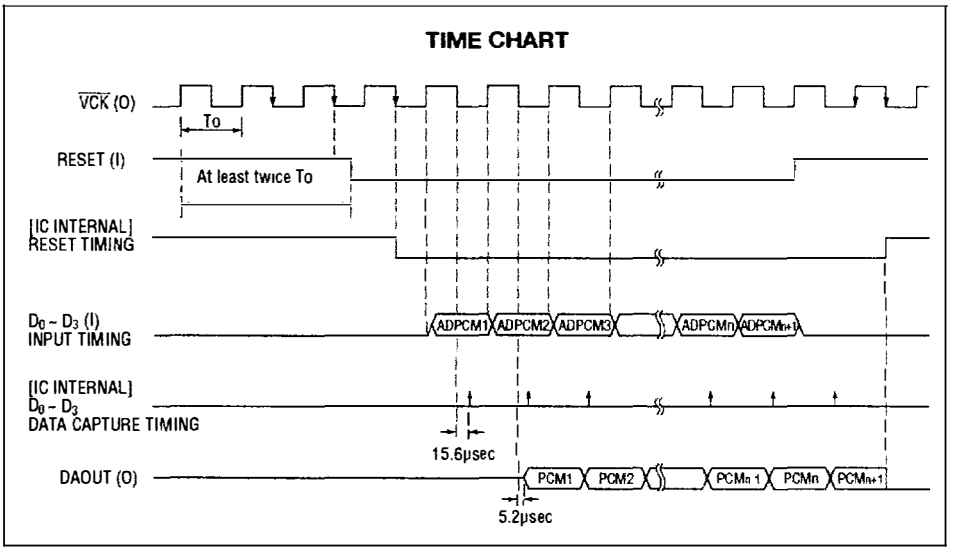


Figure 6 Waveform When the Maximum Amplitude Level of the Input Waveform is about 80% of the Dynamic Range.

Figure 7 shows the time chart for MSM5205.



Note 3: See the RESET pin description about RESET timing of the IC internal.

Figure 7

THE FOLLOWING TIMING SHOWS HOW TO APPLY THE RESET

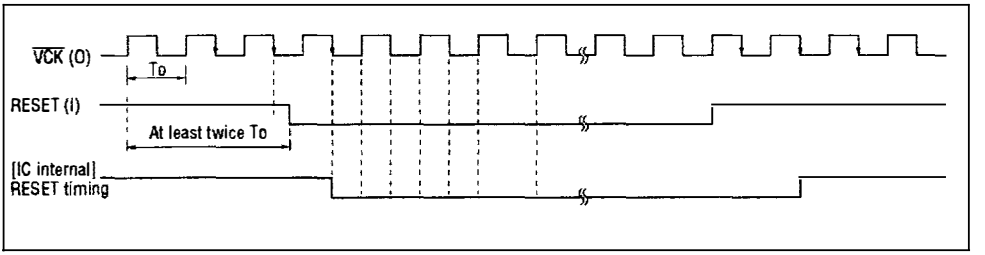


Figure 8 MSM5205 Reset Timing

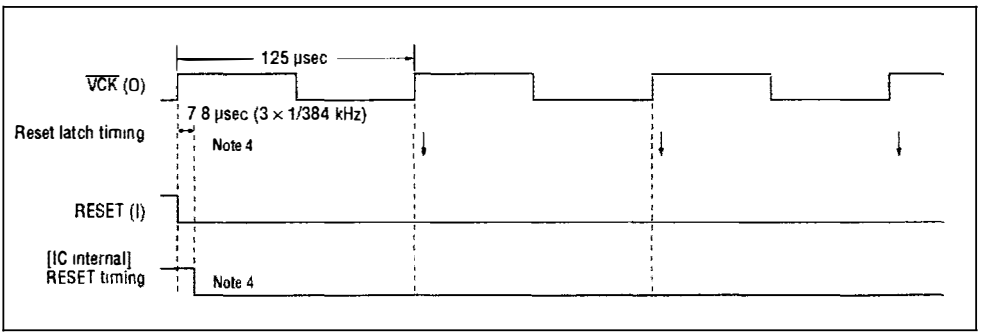


Figure 9 MSM5218 Reset Timing (8 kHz Sampling Example)

Note 4: The reset signal is latched within the LSI by the reset latch timing. Analysis is commenced by switching the external reset signal from H to L before this timing. Switching is probably best achieved by the leading edge of the VCK signal.

DISTINCTION BETWEEN MSM5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method, however, with the exception that MSM5218 is equipped with an overflow protection.

In other words, when all 12-bit PCM become '1' any further exceeding analog input would cause a data overflow which is caught and re-routed as the MSB in case of MSM5218.

MSM5205 returns to 'all bits zero' when a data overflow occurs.

Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the AD converter should be limited to 80% of the converters maximum input range.

The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

TYPICAL APPLICATION
MSM5205 TO CENTRONICS INTERFFACE CIRCUITS (f_{SAM} = 8kHz)

Figure 10 shows the MSM5205 to centronics interface circuit (f_{SAM} = 8kHz), and Figure 11 shows that timing chart.

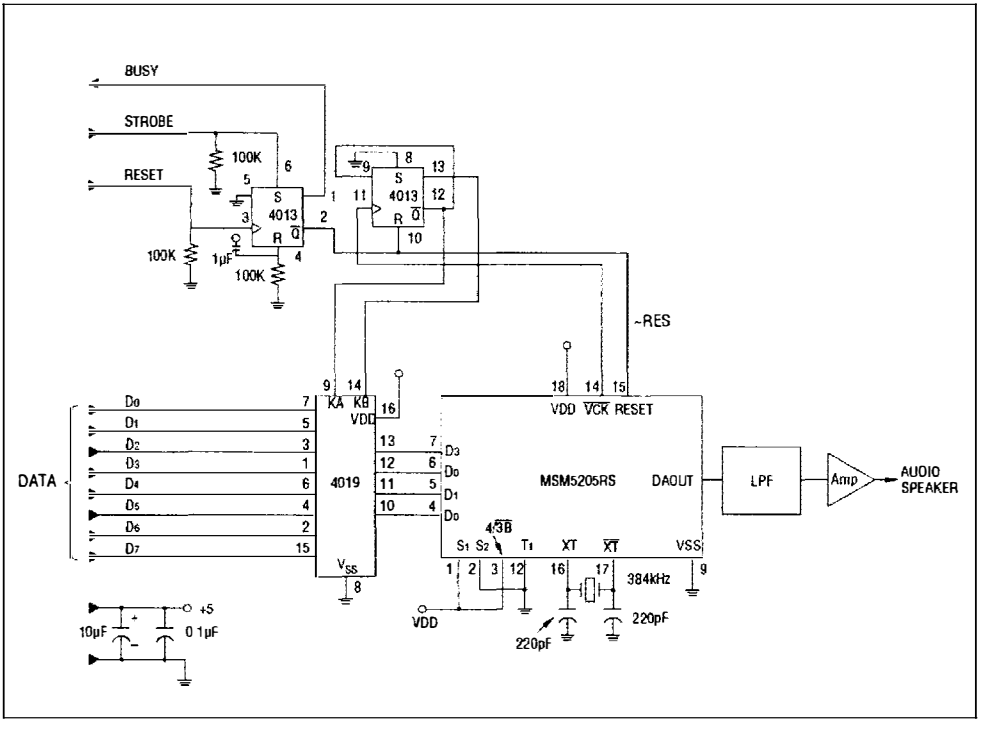


Figure 10

MSM5205 to Centronics Timing Diagram

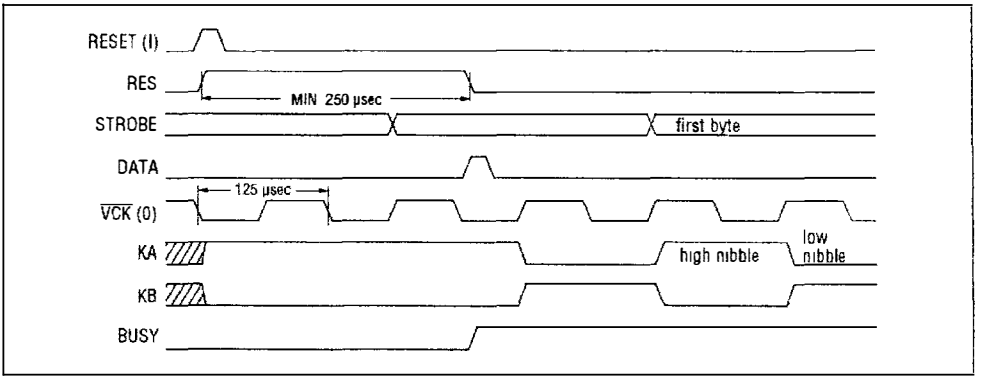


Figure 11

- **MSM5205 VOICE SYNTHESIS CIRCUIT EXAMPLE**

An example where 256k-bit EPROM are used linked together is shown in Figure 12. The timing chart for this example is provided in Figure 13.

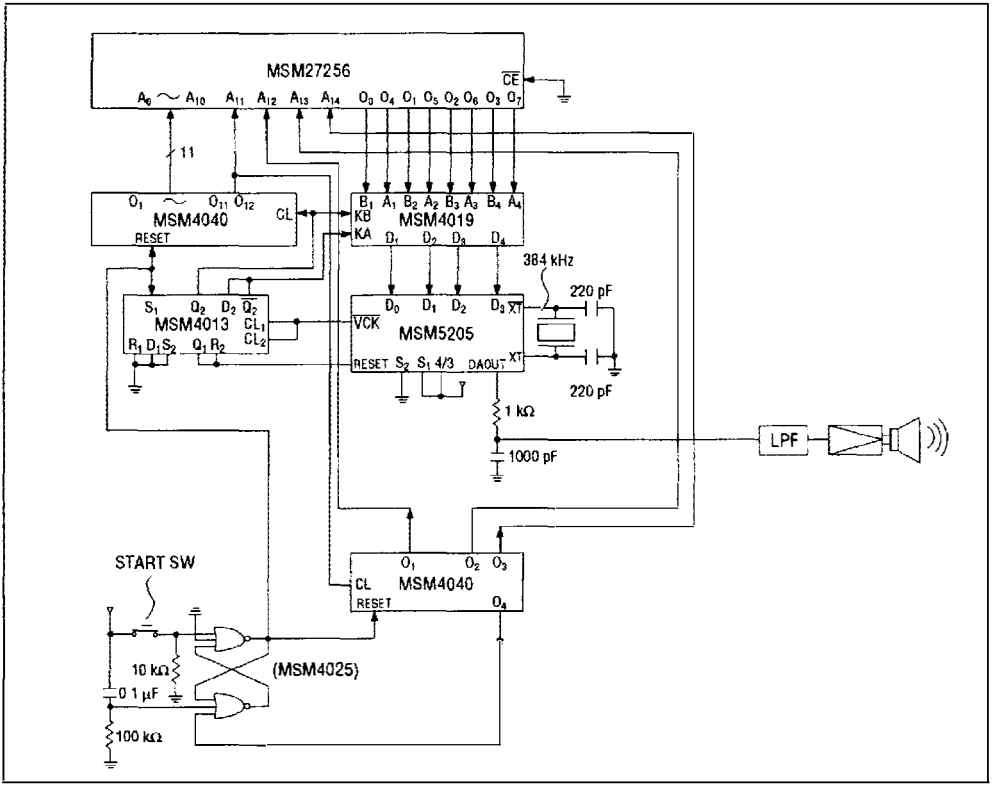


Figure 12

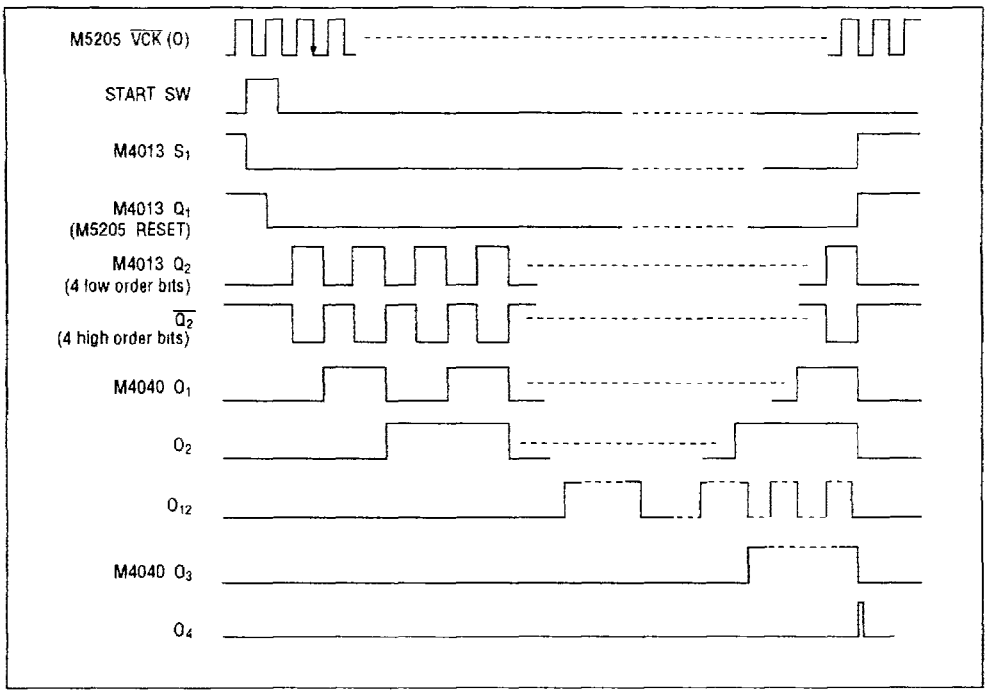

M5205 $\overline{VCK}$ (O)
START SW
M4013 S_1
M4013 Q_1
(M5205 RESET)
M4013 Q_2
(4 low order bits)
$\overline{Q_2}$
(4 high order bits)
M4040 O_1
O_2
O_{12}
M4040 O_3
O_4

Figure 13